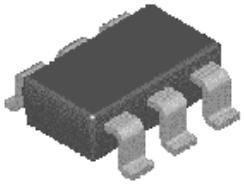
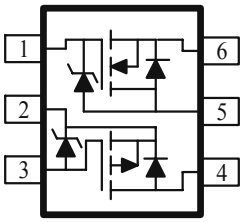
AM3850C

These miniature surface mount MOSFETs utilize High Cell Density process. Low $r_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are DC-DC converters, power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $r_{DS(on)}$ Provides Higher Efficiency
- and Extends Battery Life
- Miniature TSOP-6 Surface Mount Package Saves Board Space

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
25	0.45 @ V_{GS} = 4.5V	1.2
	0.72 @ V_{GS} = 2.5V	1.0
-25	1.09 @ V_{GS} = -4.5V	-0.85
	1.50 @ V_{GS} = -2.5V	-0.75





ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C UNLESS OTHERWISE NOTED)					
Parameter		**Symbol**	**N-Channel**	**P-Channel**	**Units**
Drain-Source Voltage		V_{DS}	25	-25	V
Gate-Source Voltage		V_{GS}	8	-8	
Continuous Drain Current[a]	T_A=25°C	I_D	1.2	-0.9	A
	T_A=70°C		0.95	-0.65	
Pulsed Drain Current[b]		I_{DM}	±3.5	±2.5	
Continuous Source Current (Diode Conduction)[a]		I_S	1	-1	A
Power Dissipation[a]	T_A=25°C	P_D	1.25		W
	T_A=70°C		0.8		
Operating Junction and Storage Temperature Range		T_J, T_{stg}		-55 to 150	°C

THERMAL RESISTANCE RATINGS				
Parameter		**Symbol**	**Maximum**	**Units**
Maximum Junction-to-Ambient[a]	t <= 5 sec	R_{THJA}	100	°C/W

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

b. Pulse width limited by maximum junction temperature

SPECIFICATIONS (T_A = 25°C UNLESS OTHERWISE NOTED)							
Parameter	**Symbol**	**Test Conditions**	**Limits**				**Unit**
			Ch	**Min**	**Typ**	**Max**	
Static							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 uA	N	25			V
		V_{GS} = 0 V, I_D = -250 uA	P	-25			
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250 uA	N	0.65	0.81	1.5	V
		V_{GS} = V_{DS}, I_D = -250 uA	P	-0.65	-0.83	-1.5	
Gate-Body Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 8 V	N			100	uA
		V_{DS} = 0 V, V_{GS} = -8 V	P			-100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V	N			1	uA
		V_{DS} = 20 V, V_{GS} = 0 V, T_J = 55°C				10	
On-State Drain Current[A]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 4.5 V	N	1			A
		V_{DS} = -5 V, V_{GS} = -4.5 V	P	-1			
Drain-Source On-Resistance[A]	$r_{DS(on)}$	V_{GS} = 4.5 V, I_D = 0.5 A	N		0.35	0.45	Ω
		V_{GS} = 2.5 V, I_D = 0.2 A			0.45	0.72	
		V_{GS} = -4.5 V, I_D = -0.41 A	P		0.860	1.09	
		V_{GS} = -2.5 V, I_D = -0.2 A			1.15	1.50	
Forward Tranconductance[A]	g_{fs}	V_{DS} = 5 V, I_D = 0.5 A	N		1.45		S
		V_{DS} = -5 V, I_D = 0.4 A	P		0.9		
Dynamic[b]							
Total Gate Charge	Q_g	N-Channel V_{DS}=5V, V_{GS}=4.5V, I_D=0.5A P-Channel V_{DS}=-5V, V_{GS}=-4.5V, I_D=-0.25A	N		1.64	2.3	nC
			P		1.1	1.5	
Gate-Source Charge	Q_{gs}		N		0.4		
			P		0.33		
Gate-Drain Charge	Q_{gd}		N		0.45		
			P		0.26		
Switching							
Turn-On Delay Time	$t_{d(on)}$	N-Chaneel V_{DD}=6V, V_{GS}=4.5V, I_D=0.5A , R_{GEN}=50Ω, P-Channel V_{DD}=-6V, V_{GS}=-4.5V, I_D=-0.41A R_{GEN}=50Ω	N		3	6	nS
			P		7	21	
Rise Time	t_r		N		8.5	18	
			P		9	19	
Turn-Off Delay Time	$t_{d(off)}$		N		17	30	
			P		55	112	
Fall-Time	t_f		N		13	25	
			P		35	71	

Notes

a. Pulse test: PW <= 300us duty cycle <= 2%.

b. Guaranteed by design, not subject to production testing.