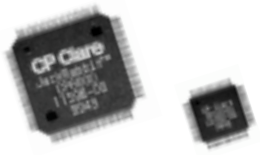
JackRabbit™
Phoneline Network PHY Transceiver Chipset
CPC6000 / CPC6100



Description

The CPC6000 physical layer (PHY) and CPC6100 analog front end (AFE) JackRabbit™ phoneline network transceiver chipset provides an economically robust solution for home and small business PC users to network their computer and Internet equipment together through ordinary copper telephone wires installed in their dwelling or office building. Operating simultaneously with ordinary telephone service (POTS) as well as analog and xDSL modems, the JackRabbit™ home phoneline network PHY chipset allows consumers to easily share high speed Internet services, play multi-player networked games and share peripheral equipment and files. The CPC6000 and CPC6100 JackRabbit™ transceiver chipset connects directly between an industry standard Ethernet Media Access Controller (MAC) over an industry standard MII (Media Independent Interface) or GPSI (General Purpose Serial Interface) interface and any RJ11 phone jack attached to the existing internal telephone wires. The JackRabbit™ chipset operates at speeds up to 10Mbps while in high speed "Turbo" mode in addition to providing a Home Phone Network Alliance (HomePNA) interoperability mode with a more robust 1Mbps technology. Consisting of the 80-pin TQFP packaged CPC6000 digital PHY device and the 48-pin TQFP packaged AFE, the JackRabbit™ chipset and available reference designs provide OEMs with a complete low cost home phoneline network interface card (NIC) solution.

Features

- Turbo mode data speed of up to 10Mbps, 5Mbps and 1Mbps within 4.5MHz – 24.5MHz band
- HomePNA interoperability mode at 1Mbps and 0.7Mbps within the 4.5MHz to 9.5MHz band
- Based upon patent and patent pending Dual Carrier Segment Modulation (DCSM)* and Adaptive Template Demodulation (ATCD)* technology
- Robust connectivity in severely impaired networks with bridged taps and other wire impairments
- Out of band spectral energy > -35dB without external filtering Superior S/N Error Performance – typically $<10^{-10}$ raw BER (without error correction) at an SNR of 8dB
- Direct connects with up to 500 feet of category "0" to category 5 twisted pair wire
- Low power consumption: <400mW
- Over 1500Vrms Isolation with external transformer
- Inexpensive 4 pole discrete filter provides proper termination
- Compatible with either 3V or 5V power supplies
- Onboard PLL's allowing inexpensive crystal for MAC and PHY clock source.
- Polarity insensitive
- Small 80-pin TQFP and 48-pin TQFP packaging

Applications

- Home phoneline network PCI NIC cards
- Home phoneline network USB NIC cards and adapters
- Home phoneline network PCMCIA NIC cards
- Phoneline adapter or dongle for standard Ethernet 10/100 NIC cards
- Network Printers and Scanners
- Residential gateway systems
- Set Top Boxes - shared entertainment
- xDSL Modems - shared Internet
- Cable Modems - shared Internet
- Voice Over IP Phones (Web-phones)
- Internet gaming systems
- Remote Metering
- Video Conferencing
- Home Monitoring and Security Systems
- Home Automation Systems

Approvals

- UL1950
- UL1459
- FCC PART 15B
- FCC PART 68
- HomePNA 1.0 Reference Design Certification

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Rev. 0A, 2/8/00

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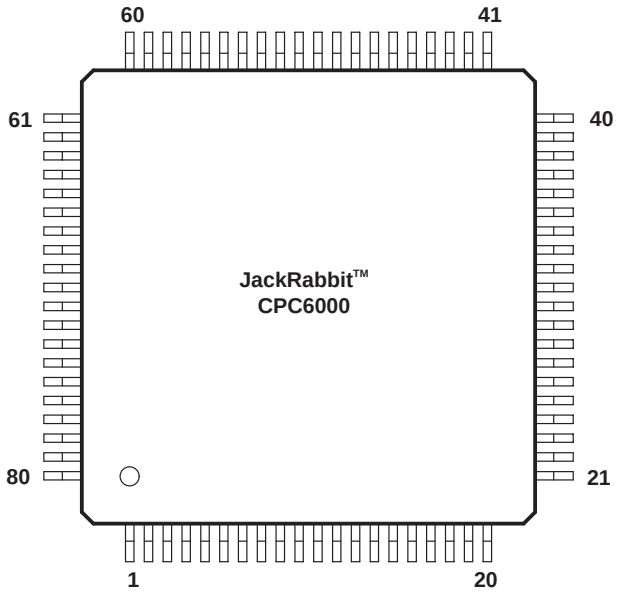
JackRabbit™ CHIPSET PIN DESCRIPTION

CPC6000 PHY PINOUT



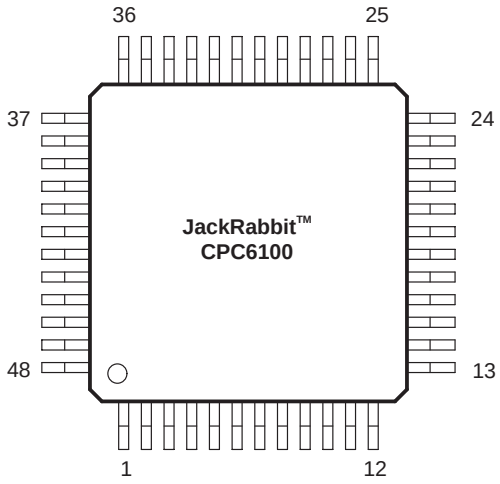
CPC6000 PHY PIN DESCRIPTION

Pin #	Name	Type	Description
1	SPI_DOUT	O	SPI port data out. Used in GPSI mode for communication with PHY.
2	TEST_XMIT1	NC	No connect. Leave pin floating. For production test.
3	Vcc	PWR	Digital power pin. 3.3V +/- 10%. Power to PLL.
4	PLL_60_LF	O	Pin for external filter to 60MHz PLL circuit. See Application schematic.
5	Vdd	GND	Ground Pin for 60MHz PLL circuit.
6	TEST_XMIT10	NC	No connect. Leave pin floating. For production test.
7	Vcc	PWR	Digital power pin. 3.3V +/- 10%. Connects to digital core.
8	Vdd	GND	Ground pin. Connects digital core to digital ground plane.
9	Vdd	GND	Digital ground to the MII interface.
10	SPI_CS	I	Chip select strobe for the SPI port. Leave pin as a NC.
11	RX_D3	O	Receive data for MII interface. Inactive in GPSI mode.
12	RX_D2	O	Receive data for MII interface. Inactive in GPSI mode.
13	RX_D1	O	Receive data for MII interface. Inactive in GPSI mode.
14	RX_D0	O	Receive data for MII interface. Used as RX_D in GPSI mode.
15	CRS	O	Carrier Sense for MII interface. On when TX or RX non-idle. Also used in GPSI mode.
16	COL	O	Collision detect for MII interface. Also used on GPSI interface.
17	MD_ADD4	I	Input on power-up. Sets MII physical address in MII register.
18	MD_ADD3	I	Input on power-up. Sets MII physical address in MII register.
19	MD_ADD2	I	Input on power-up. Sets MII physical address in MII register.
20	MD_ADD1	I	Input on power-up. Sets MII physical address in MII register.
21	MD_ADD0	I	Input on power-up. Sets MII physical address in MII register.
22	Vcc	PWR	Digital power pin. 3.3V +/- 10% Power to internal PADS.
23	Vcc	PWR	Digital power pin. 3.3V +/- 10%. For Oscillator section.

Pin #	Name	Type	Description
24	XTAL2	I	Crystal connection. Connect through 10pF cap.
25	XTAL1	O	Crystal connection.
26	Vdd	GND	Oscillator Ground pin. Connected to digital ground plane.
27	Vcc	PWR	Digital power pin. 3.3V +/- 10% Power to internal PADS.
28	LINK_ACT	O	Link activation LED driver. Outputs 16mA.
29	RX_MODE	O	For powering LED on card. Outputs HPNA / Turbo mode indication.
30	DAC_0	O	Output from modulator to DAC on CPC6100 AFE.
31	DAC_1	O	Output from modulator to DAC on CPC6100 AFE.
32	DAC_2	O	Output from modulator to DAC on CPC6100 AFE.
33	DAC_3	O	Output from modulator to DAC on CPC6100 AFE.
34	DAC_4	O	Output from modulator to DAC on CPC6100 AFE.
35	Vdd	GND	Connect to digital ground. Return for PADS.
36	Vcc	PWR	Digital power pin. 3.3V +/- 10% Power to internal PADS.
37	DAC_CLK	O	Clock from modulator to CPC6100 AFE. Drives sampling rate.
38	DAC_5	O	Output from modulator to DAC on CPC6100 AFE.
39	DAC_6	O	Output from modulator to DAC on CPC6100 AFE.
40	DAC_7	O	MSB Output from modulator to DAC on CPC6100 AFE.
41	DAC_SCAL	O	DAC scaling pin. Connects through resistor selection to AFE Vref pin.
42	G_COMP1	I	Input from comparator on CPC6100 AFE for phoneline network connections.
43	P_COMP1	I	Input from comparator on CPC6100 AFE for phoneline network connections.
44	N_COMP1	I	Input from comparator on CPC6100 AFE for phoneline network connections.
45	G_COMP2	I	Input from comparator on CPC6100 AFE for NIC card connections.
46	P_COMP2	I	Input from comparator on CPC6100 AFE for NIC card connections.
47	N_COMP2	I	Input from comparator on CPC6100 AFE for NIC card connections.
48	MANCH_CLK	O	Clock source for comparator bank #2 sampling.
49	Vcc	PWR	Digital power pin. 3.3V +/- 10%. Power to the PADS.
50	Vdd	GND	Ground connection to digital core. Connect to digital ground plane.
51	Vcc	PWR	Digital power pin. 3.3V +/- 10%. Power to 10BaseT core (endec block).
52	PLL_DISAB	I	PLL disable. Sampled on power up, active high. Has internal pull down.
53	Vdd	GND	Ground for 80MHz PLL circuit. Connect to digital ground plane.
54	PLL_80_lf2	I/O	Connection from 80MHz PLL to digital ground through filter.
55	Vcc	PWR	Digital power pin. 3.3V +/- 10%. Power for PLL.
56	Rref	I	Connect to digital ground through a 6.19K resistor to digital ground.
57	Vcc	PWR	Digital power pin. 3.3V +/- 10%. Power to the PADS.
58	CK_60_MON	I/O	Used to force 60MHz operation for testing. Leave as no connect.
59	60_CLK_IN	I/O	60MHz clock oscillator input.
60	80_CLK_IN	I/O	80MHz clock oscillator input.
61	GPSI_EN	I	Used to enter GPSI mode after reset. Must be pulled low with reset.
62	MANCH_N	O	Output to NIC card. Capacitively coupled to transformer – positive side.
63	MANCH_P	O	Output to NIC card. Capacitively coupled to transformer + positive side.
64	INT_A	O	Output to MAC or controller to signify interrupt condition. Open drain output.
65	CK_25	O	25MHz output to MAC for clock to MAC chip.
66	Vdd	GND	Connect to digital ground. Return for PADS.
67	RST	I	Reset. Will reset the device and all registers return to default values.
68	TX_CLK	O	Transmit clock for MII interface. 25% of data rate. Also used for GPSI.

Pin #	Name	Type	Description
69	TX_EN	I	Transmit enable for MII interface. Also used for GPSI interface.
70	TX_ER	I	Transmit error for MII interface. Valid only when TX_EN also set.
71	TX_D3	I	Transmit Data for MII interface. Inactive in GPSI mode.
72	TX_D2	I	Transmit data for MII interface. Inactive in GPSI mode.
73	TX_D1	I	Transmit data for MII interface. Inactive in GPSI mode.
74	TX_D0	I	Transmit data for MII interface. Used as TX_D in GPSI mode.
75	RX_CLK	O	Receive data clock for MII interface. Also used for GPSI interface.
76	RX_DV	O	Receive data valid for MII interface. Started at packet deliminator.
77	RX_ER	O	Receive error for MII interface. Any error detected by PHY.
78	Vcc	PWR	Power connection to digital core. 3.3V +/- 10%.
79	SPI_CLK/MDC	I/O	Mgt data clock for MII interface. Also, used for SPI port in GPSI mode.
80	SPI_DI/MDIO	I/O	Mgt data in/out for MII interface. Also, used for SPI port in GPSI mode for SPI data input. Muxed with SPI_DOUT to emulate MDIO for software compatibility.

CPC6100 AFE PINOUT



CPC6100 AFE PIN DESCRIPTION

Pin #	NAME	TYPE	DESCRIPTION
1	NC	NC	No connect. Leave floating.
2	DAC_7	I	Input from CPC6000 modulator to AFE DAC – transmit to twisted pair. (MSB)
3	DAC_6	I	Input from CPC6000 modulator to AFE DAC – transmit to twisted pair.
4	DAC_5	I	Input from CPC6000 modulator to AFE DAC – transmit to twisted pair.
5	Vdd	PWR	Digital power pin. 3.3V +/- 10%.
6	Vssa	GND	Ground. Connect to analog ground plane.
7	DAC_CLK	I	Input from modulator chip. Drives sampling rate.
8	DAC_4	I	Digital input from CPC6000 modulator to DAC – transmit to line.
9	DAC_3	I	Digital input from CPC6000 modulator to DAC – transmit to line.
10	DAC_2	I	Digital input from CPC6000 modulator to DAC – transmit to line.
11	Vdd	PWR	Digital power pin. 3.3V +/- 10%.

Pin #	Name	Type	Description
12	Vssa	GND	Ground. Connect to analog ground plane.
13	DAC_1	I	Input from CPC6000 modulator to AFE DAC – transmit to twisted pair.
14	DAC_0	I	Input from CPC6000 modulator to AFE DAC – transmit to twisted pair. (LSB)
15	Vssa	GND	Ground. Connect to analog plane.
16	Vssa	GND	Ground. Connect to analog plane.
17	Ref_G1	I	Ground reference to phoneline network signal input from twisted pair wire.
18	Ref_P1	I	Positive reference to phoneline network signal input from twisted pair wire.
19	SIG_IN1	I	Signal input from anti alias filter from the twisted pair input.
20	Ref_N1	I	Negative reference to phoneline network signal input from twisted pair wire.
21	Ref_G2	I	Ground reference for Manchester signal from NIC card.
22	Ref_P2	I	Positive reference to Manchester signal from NIC card.
23	SIG_IN2	I	Manchester signal input from NIC card.
24	Ref_N2	I	Negative reference to Manchester signal from NIC card.
25	NC	NC	No connect. Leave as float.
26	Vdd	PWR	Digital power pin. 3.3V +/- 10%.
27	Vdd	PWR	Digital power pin. 3.3V +/- 10%.
28	NC	NC	No connect. Leave as float.
29	NC	NC	No connect. Leave as float.
30	Vss	GND	Ground connection.
31	COMP2_CLK	I	Clock for Manchester comparators. Connect to Manch_Clk on digital chip.
32	N_COMP2	O	Output to CPC6000 modulator. Manchester receive data from NIC card.
33	P_COMP2	O	Output to CPC6000 modulator. Manchester receive data from NIC card.
34	G_COMP2	O	Output to CPC6000 modulator. Manchester receive data from NIC card.
35	N_COMP1	O	Output to CPC6000 modulator. Phoneline network receive data.
36	NC	NC	No connect. Leave floating.
37	P_COMP1	O	Output to CPC6000 modulator. Phoneline network receive data.
38	G_COMP1	O	Output to CPC6000 modulator. Phoneline network receive data.
39	Vdd	PWR	Digital power pin. 3.3V +/- 10%.
40	Vssa	GND	Analog ground pin. Connect to analog ground plane.
41	Vssd	GND	Digital ground. Connect to digital ground plane.
42	R_BIAS	I	Sets reference in DAC. Connected through 6.19K resistor.
43	Vdda	PWR	Power to analog section. 3.3V +/- 10%.
44	RB/DD	I	Connect to Vdd. Sets internal bias point.
45	I_NEG	I	Negative Current output source. 10mA max. To twisted pair line.
46	Vref	I	Sets reference for DAC. Connect through 0.1uF cap to ground.
47	I-POS	O	Positive current source Output. 10mA max, or 1Volt output.
48	Vdd	PWR	Digital power pin. 3.3V +/- 10% at current source.

System Configuration Block Diagrams

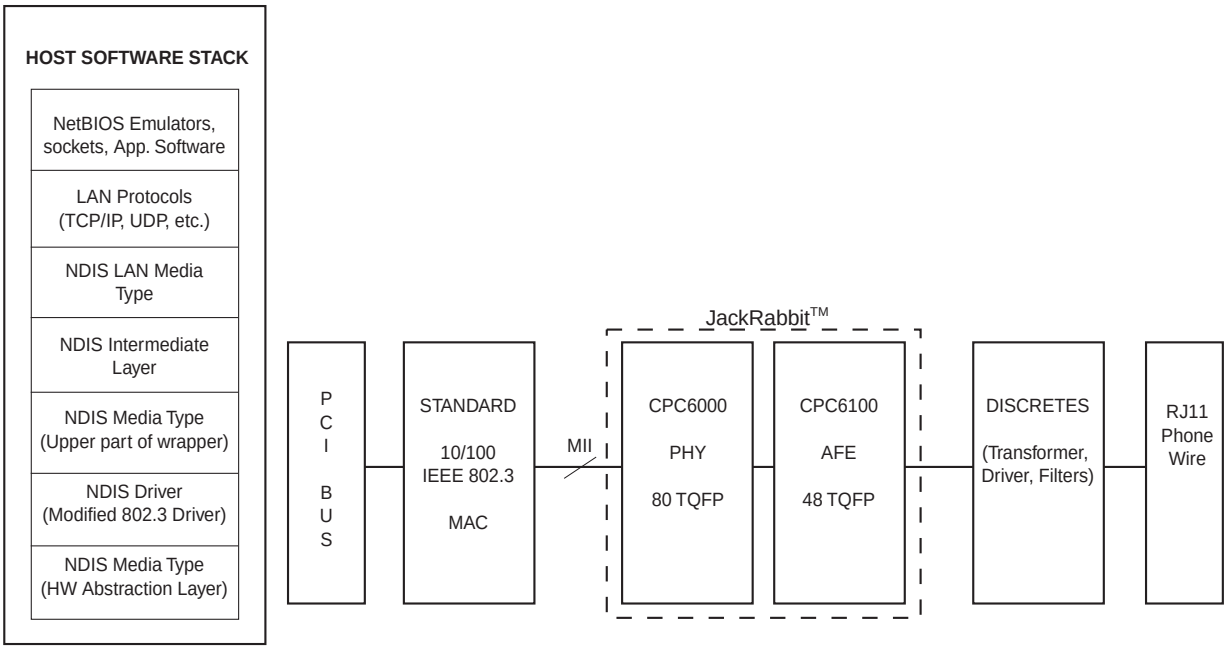


Figure 1. PCI Bus Half Card System Configuration

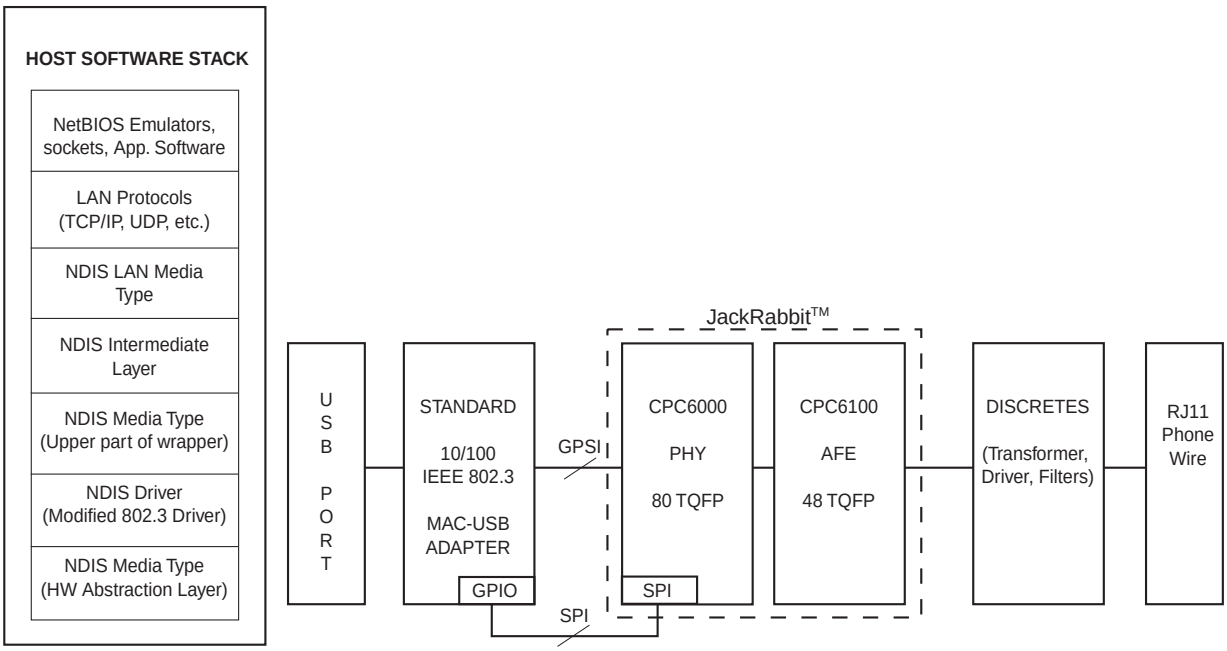


Figure 2. USB Port System Configuration

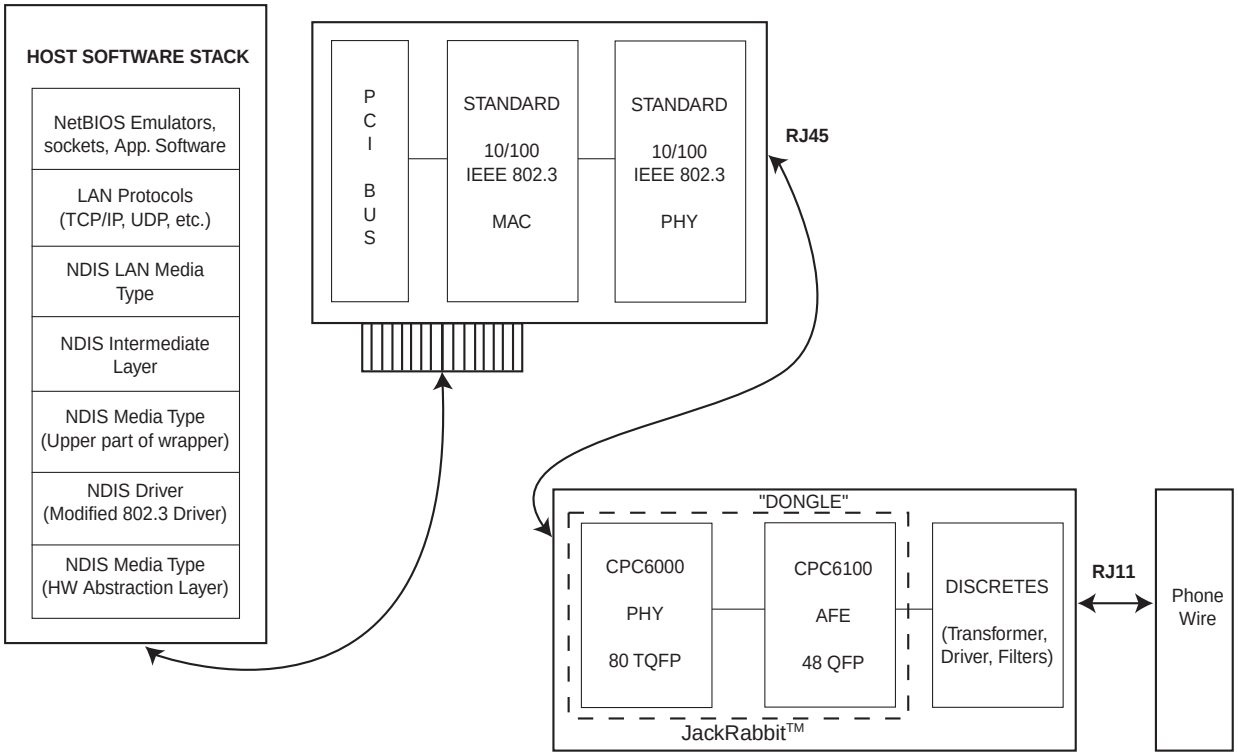


Figure 3. Adapter/Dongle System Configuration

INTRODUCTION

The personal computer has become a powerful platform in the home for work, communication, education, and entertainment. The Internet has exploded into an essential means of information access. Just as there is a critical need for high-speed connections to information and broadband entertainment outside the home, there is a growing need for this type of networking access inside the home as more and more homes have multiple PCs and users.

Until recently, however, Local Area Networks have not penetrated the home because of the poor quality of the in-home phone wiring installation and the high cost of running dedicated wiring in a finished home. In-home phone wires are frequently run to jacks that either have no telephone attached or have a phone that is not of high quality. Often wires have simply been cut leaving a "tap", or bridged tap, that does not affect voice communications but causes major problems for high speed data services. Bridged taps cause major problems in data transmission because they will actually reflect the transmitted signal and cause destructive interference with the data transmission as the time delay in the reflected signal is summed with the signal currently being sent.

In addition, most communication techniques have been constructed for an environment where there are many subscribers and precious copper resources. This historically resulted in modulation techniques such as (Quaternary Amplitude Modulation) QAM, which attempts to squeeze as many bits into as small a spectrum as was possible. 16, 32, 64, 128, and even 256 QAM have been proposed in the home telephone environment. This truly is a waste of resources – measured by processor cycles, silicon gates, or even system cost as QAM attempts to rebuild the original waveform through equalization, modulation, error correction and a host of other methods. The many taps and single customer residential wiring actually presents the exact inverse of central office plant which contains few taps and many subscribers.

To solve the problems encountered with phoneline networking, the JackRabbit™ chipset uses a much less complex modulation technique. The general consideration is to send a known data pattern into the channel, and to model the channel with all of its corruptive influences in a template that can be adaptive on a packet by packet basis. The resulting pattern is then correlated with future data transmissions within that same packet with a patented technique called Adaptive Template correlation. This results in a receiver that is little more than a simple state machine with much less demand on the analog to digital conversion process. To further this robust process, a patented Dual Carrier Segment Modulation* technique is used to create a bitstream from symbols. The carriers used are frequency diverse such that a reflection reacting destructively with one carrier constructively acts with the other carrier. Therefore, the technology used in the JackRabbit™ chipset does not require restoration of the carrier envelope through equalization and long training sequences but adapts within 24 data bits at the beginning of each packet.

FUNCTIONAL DESCRIPTION

The CPC6000 and CPC6100 chipset perform the same functions that a standard Ethernet 10/100Mbs PHY performs with the exception that category 5 Ethernet wiring is not required since the JackRabbit™ chipset operates over standard twisted pair telephone wire. From the perspective of a standard Ethernet MAC, the same protocols are used to communicate with other Ethernet cards. The only modification to any OSI layer above the PHY is a slight modification to the NDIS driver to allow for automatic speed negotiation during data transmission. This is a required change for home phone networking systems due to the fact that communication at a set speed (10/100) is not viable in an environment with rapidly changing characteristics. At the PHY layer, an Ethernet frame is stripped of its preamble and another preamble is appended to the frame. At the other end of the transmission channel, the reverse process is performed. Because all of the transmissions occur in Turbo mode at 4.5MHz - 24.5MHz or in the HomePNA interoperability mode band of 4.5MHz - 9.5MHz, all JackRabbit™ phoneline LAN communications are frequency division multiplexed with normal POTS, V.90 modem, ISDN, and ADSL services for coexistence inside the home.

The JackRabbit™ chipset and available reference design is interoperable with the HomePNA 1Mbps specification (Version 1.1) using robust DCSM* and ATCD* mod/demod technology. The HomePNA interoperability mode of operation allows transmission at 1Mb/s and 0.7Mb/s depending on the channel impairment characteristics, and provides a common platform upon which all current and future HomePNA certified home phoneline LAN cards can communicate with each other.

In addition, the JackRabbit™ chipset and available reference design will automatically Turbo up to communicate at the highest speed allowed by the channel (10Mbps, 5Mbps or 1Mbps) when communicating to another node on the network incorporating JackRabbit™ technology. When the chipset is powered up, software on the host system (NDIS driver) will poll all other nodes on the network. This is done exhaustively so that all nodes on the network will build a speed look up table that will combine each card's Ethernet address with the fastest speed that each node can be communicated with over the existing channel. This polling technique is performed at regular programmable multiples of 2-second intervals so that if the channel

characteristics change, communications with each node will continue to be optimized for its maximum performance capabilities. The home or small office network is dynamic and significant changes in the channel characteristics are common. For example if a phone is removed from a wall socket during transmission, the attenuation characteristics of the channel are greatly affected. Additionally, the polling algorithm feature of the JackRabbit™ allows random entry by additional stations as in the case of a laptop plugging into a wall jack to use a remote networked printer. The CPC6000 and CPC6100 chipset and associated MAC software driver therefore provides automatic speed negotiation from HomePNA interoperable 0.7Mbps up a Turbo mode of 10Mbs without any user intervention.

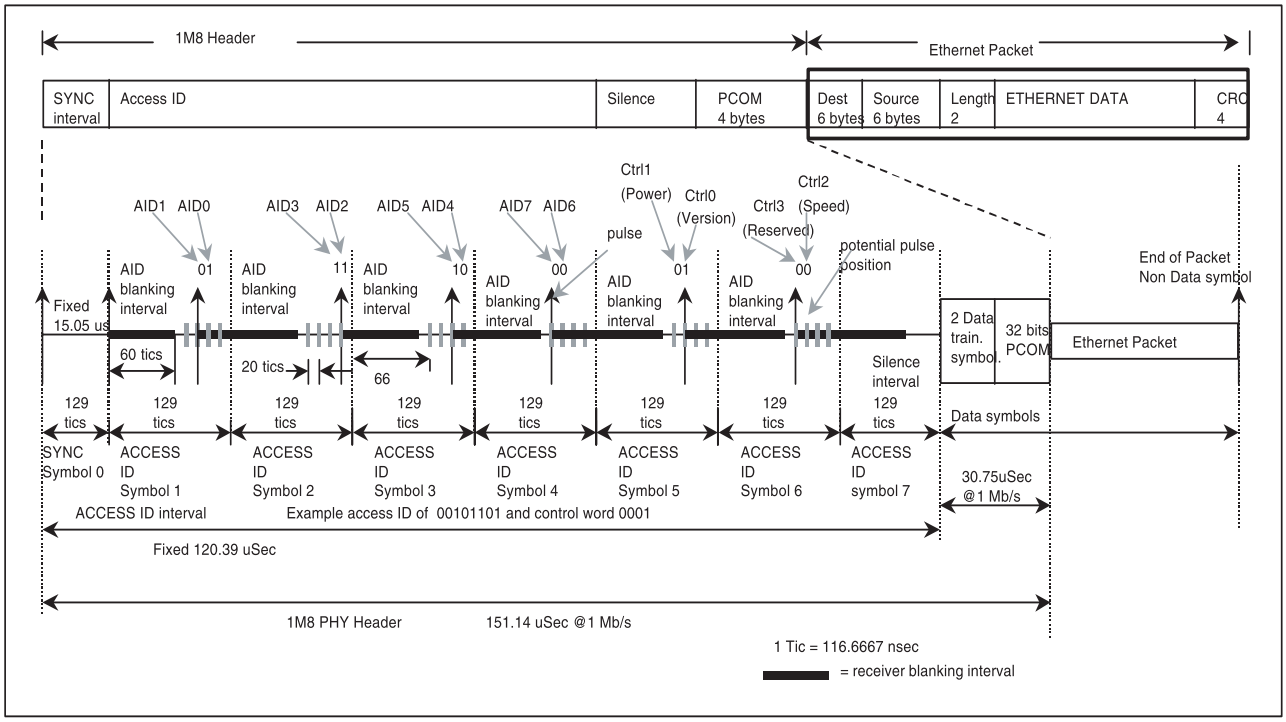


Figure 4. HomePNA 1Mb/s Frame Structure

PHY CORE DESCRIPTION

Overview

In both HomePNA interoperability mode (1Mbps) and high speed Turbo mode (10Mbps) mode, the JackRabbit™ phoneline chipset along with an Ethernet MAC essentially perform the same function as a typical Ethernet MAC/PHY NIC configuration with only a slight modification to the host based NDIS driver for rate adaptation functions. The reason standard Ethernet PHYs cannot be connected to standard twisted pair wire is that those devices require a tightly controlled termination whereby reflected emissions are reduced to a minimum. The home phoneline wire network is exactly the opposite situation where terminations are multiple and incalculable as to the effect on any particular signal. The PHY design goal is therefore to get a signal through a multitude of channel types as efficiently as possible.

The JackRabbit™ chipset accomplishes this goal as it overcomes the difficulties of the phoneline network through advanced DSCM* modulation and ATCD* demodulation technologies. The CPC6000 utilizes these new technologies in both the high speed Turbo (10Mbps) mode of operation and the HomePNA interoperability (1Mbps) mode of operation so that reuse of the chip's architecture is maximized. There are parallel front-end pulse detectors that are required to be working at the same time to determine which type of waveform has been received and transmitted. These receivers send data to the MII interface registers so that the host software can build its speed-address look up tables correctly as further described below.

A scrambler is also used to randomize the data pattern so that voltage skews cannot be built up on the wire pairs. The maximum voltage output to the twisted pair is below the FCC authorized limit of 560mV.

A simplified block diagram of the modem is shown in figure 5, and the AFE is shown in figure 6 below.

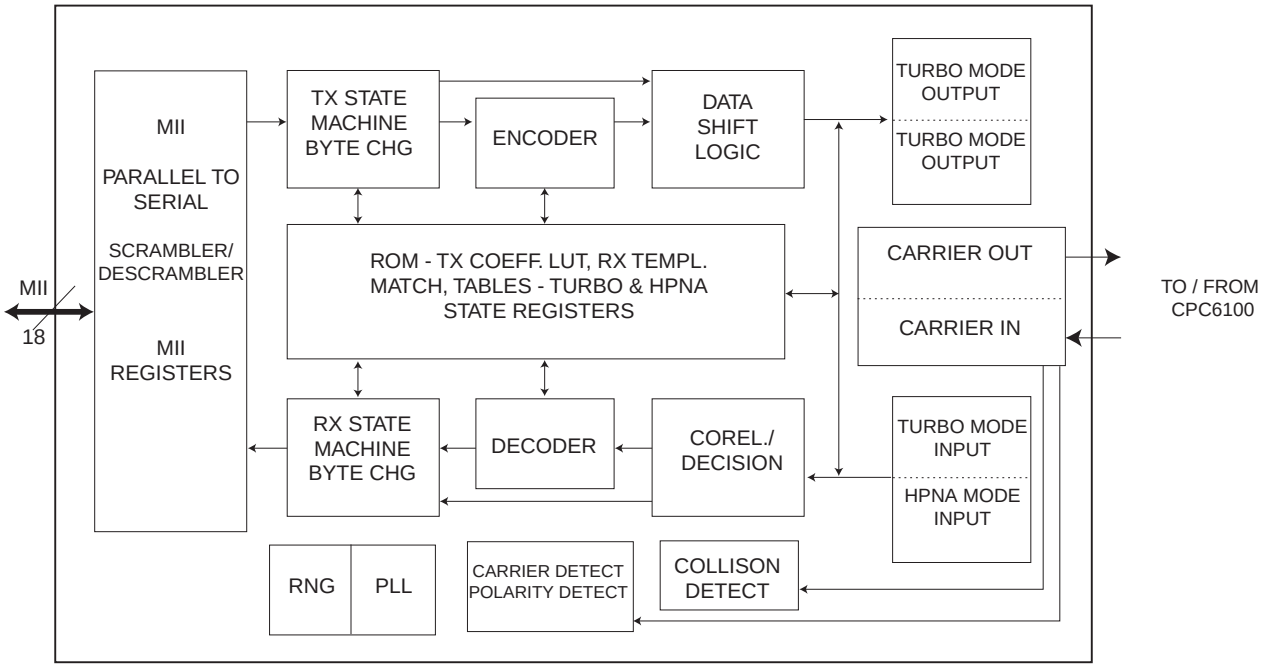


Figure 5. Simplified CPC6000 PHY Block Diagram

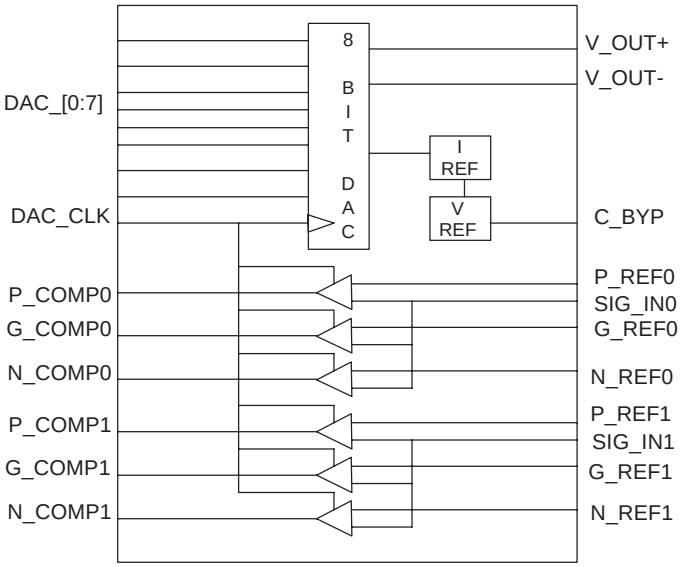


Figure 6. Simplified CPC6100 AFE Block Diagram

MAC Interface

The interface to the MAC is shown in Figure 5. In the case of the MII interface, data is received in nibble wide blocks and feeds a parallel to serial conversion process before entering the transmit scrambler. The GPSI interface is inherently serial in nature, and bypasses the parallel to serial conversion process before entering the transmit scrambler. The scrambler itself uses a 2^{11} - 1 polynomial to scramble the incoming data. The exact reverse process takes place when receiving data from the demodulator block.

The transmit control block sends speed information to the core modulator after receiving that information from either the MII management port or 4-wire serial management interface that is host based driver directed. In the receive direction, the modem core will send the sampling clock to the receive control block. This clock is used to transmit data over either the MII or GPSI interface to the MAC. Therefore, in the receive direction, data speed will be directed by the receive clock rate over the interface.

The receive control block also inputs pulses from both the carrier sense and collision detect logic and relays that to the output pins directly.

Turbo Mode Data Transmitter

Scrambled data is passed from the MII/GPSI interface block to the transmit state machine logic. This logic strips the first 64 bits off of the standard Ethernet frame, which includes both the preamble and SFD (start of frame delimiter). These bits are replaced with a DCSM preamble as defined below in figure 7. Because of this, the DCSM preamble is not scrambled when sent over the twisted pair medium, but has been carefully selected to fit a pseudo-random sequence.

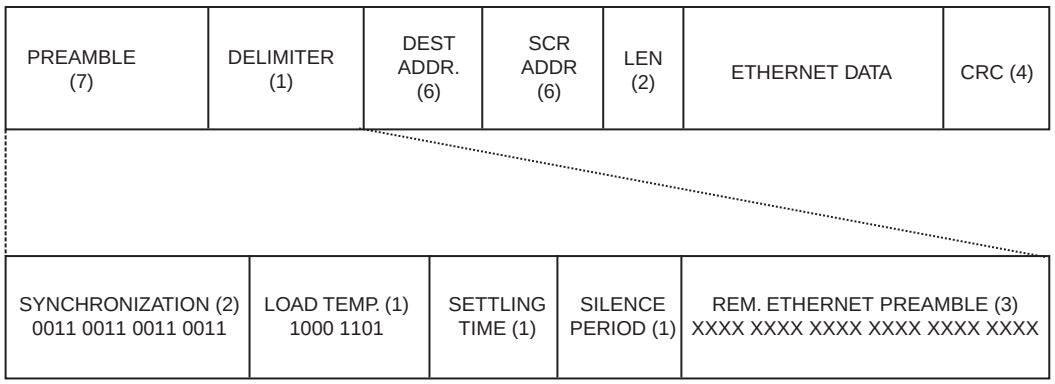


Figure 7. Turbo Mode Preamble

The preamble shown above allows for synchronization between the transmitter and other receivers on the network, correlator template loading, and an 8 bit settling period followed by an 8 bit silence period. The settling and silence period is used to determine if collisions have occurred on the network over the maximum length of twisted pair wire.

The remaining 24 bits of preamble are used for warming up the transmitter, turning on the data valid signal, and sending serial data out. Essentially this represents a setup time to present the data to the RLL encoder in the case of HomePNA interoperability (1Mbps) mode transmissions or to the phase accumulator in the case of Turbo mode (10Mbps) transmissions. The remainder of the transmitter is the actual modulator that transforms the scrambled bit stream into symbols. This is the phase accumulator state machine logic that decides which value is output from the DAC to the twisted pair wire. These coefficients are cosine segments that represent the magnitude from a maximum to a minimum slope point on a sinusoidal wave pattern. These coefficients are actually an address into a static LUT holding binary values to be sent directly into the DAC. The phase accumulator also holds a comparator that notifies the state machine if a zero slope point has been reached which indicates the bit edge.

The resultant output waveform is precise, requiring only a filter for cleaning DAC noise effects on its output. The remaining blocks of the Turbo mode (10Mbps) transmitter portion of the modem are shown in figure 8 below.

HomePNA Interoperability (1Mbps) Transmitter

In HomePNA interoperability operation, data is passed to the transmit state machine logic in the same fashion as is performed on the high speed Turbo mode (10Mbps) data stream. The logic will also strip the first 64 bits of the Ethernet preamble as specified by the HomePNA version 1.1 document. The logic attaches the specified HomePNA 1.1 frame structure as shown in figure 4. Therefore, just like Turbo mode operation, the preamble is not scrambled. In HomePNA interoperability mode, however, the 1 Mbps transmit frame is passed to an encoder which encodes the data pattern for the time based transmission scheme. The information is then sent to the same coefficient look up table state machine as described in Turbo mode for transmission to the DAC where the HomePNA interoperability mode (1Mbps) waveform is built. A block diagram of the HomePNA interoperability mode transmit block is shown below in figure 9.

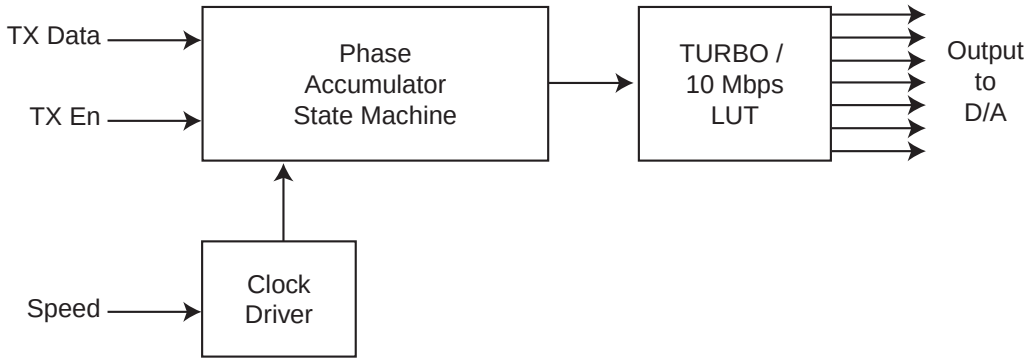


Figure 8. Post State Machine Transmitter Logic

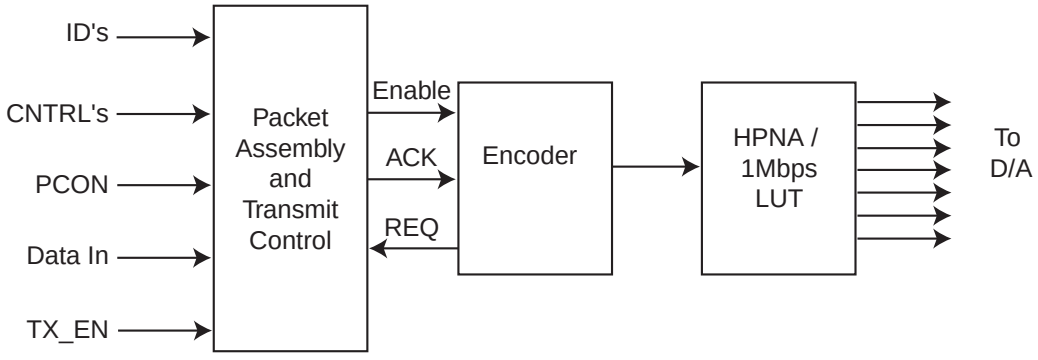


Figure 9. HomePNA 1Mbps Transmitter Logic

Turbo Mode Receive Path

There is a limiter circuit that will limit the incoming voltage and magnitude templates as the variance in voltage will be from a minimum of 10mV at the farthest nodes to a 2.5V maximum for a node placed close to the receiver. Once data has passed through the comparators, it is presented to a carrier detect mechanism that makes determinations based on the three input slice thresholds and the digital input level. The receiver is polarity insensitive and can determine both positive and negative pulses coming in. This is performed in the carrier detect and polarity detect logic and is done on a continuing basis while the receiver synchronizes on the first 24 bits of known preamble. The receiver will lock within the first 16 bits, but may require up to 24 on severely impaired channels. When the receiver is locked (or "framed-up"), it begins to load templates that will hold the incoming data stream. This is done with a known data pattern so that known binary levels with channel impairment conditions are stored in the reference templates. Future bit values are shifted into registers, compared to the reference templates, and sent to a majority voting state machine. Because the bits (grouped 3 at a time) are shifted exhaustedly, high correlation values are scored for the voting process. This is done in parallel with a correlation process on the raw data stream, so that two different scoring methods are engaged to produce the final data stream robustly. The output from the majority voting logic is the data recovered from the input symbol pattern. Note that each symbol is over-sampled either 8 or 16 times so that the final score summation of the 8/16 template matching scores for greater accuracy in determining the bit value.

This data stream is then fed to state machine logic that strips the first 64bits of the frame and attaches the Ethernet preamble and delimiter before being sent to the $2^{11} - 1$ descrambler in the MII interface (see figures 5 and 6). A block diagram of the Turbo mode (10Mbps) receiver is shown below in figure 10.

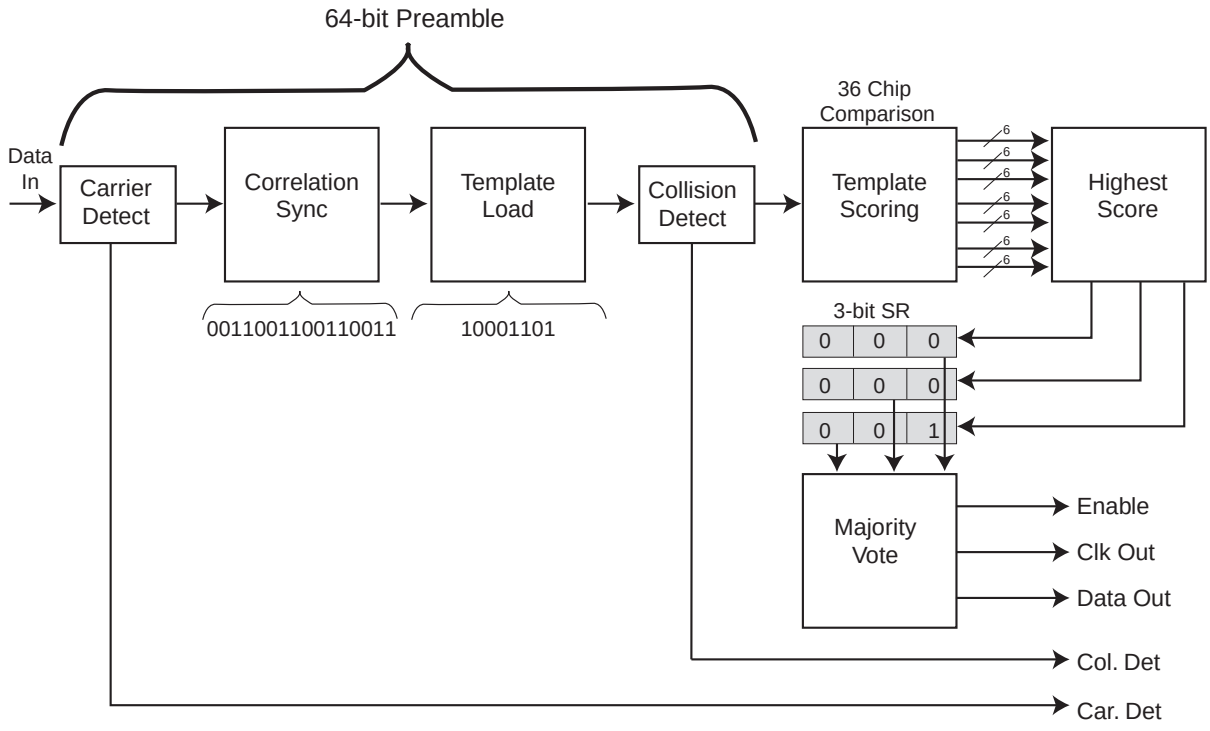


Figure 10. Turbo Mode Receiver

HomePNA INTEROPERABILITY (1Mbps) RECEIVER

The front end of the receiver for HomePNA interoperability (1Mbps) mode operates completely in parallel with the Turbo mode (10Mbps) receiver. Therefore, upper layer software can have information about which receiver is active so that no latency needs to be built into the receive path even though most of the circuitry is redundant. The HomePNA 1.1 specification calls for an energy detect voltage threshold slicer for determining the presence of a valid pulse. The JackRabbit™ chipset implements additional decision state logic to improve the 1Mbps receiver robustness beyond the specification by correlating total energy over the pulse wave. Each pulse is over-sampled by 8X or 16X that provides more consistent detection of timer tic locations. These timer tic locations are related to the actual data stream as shown in figure 4. Note that the same carrier sense and polarity detect circuitry is active during HomePNA interoperability mode reception as in Turbo mode (10Mbps) and eventually only one of the two receivers will remain active. In fact, the Turbo mode (10Mbps) receiver will lock onto the data pattern well before the second tic of a HomePNA 1Mbps frame has been decoded as it will lock within 16BT or bit times. By the time a HomePNA 1Mbps receiver begins to receive valid AID symbols, the 10Mbps Turbo mode receiver will have "turned off". The HomePNA 1Mbps receiver will then send the resultant data stream into the RLL25 decode state machine logic before the data is then sent to the main receive state machine logic to strip the HomePNA 1Mbps header and attach a standard Ethernet preamble and frame delimiter. This state machine then feeds the $2^{11} - 1$ descrambler within the MII or GPSI interface. A block diagram of the HomePNA interoperability mode receiver is shown below in figure 11.

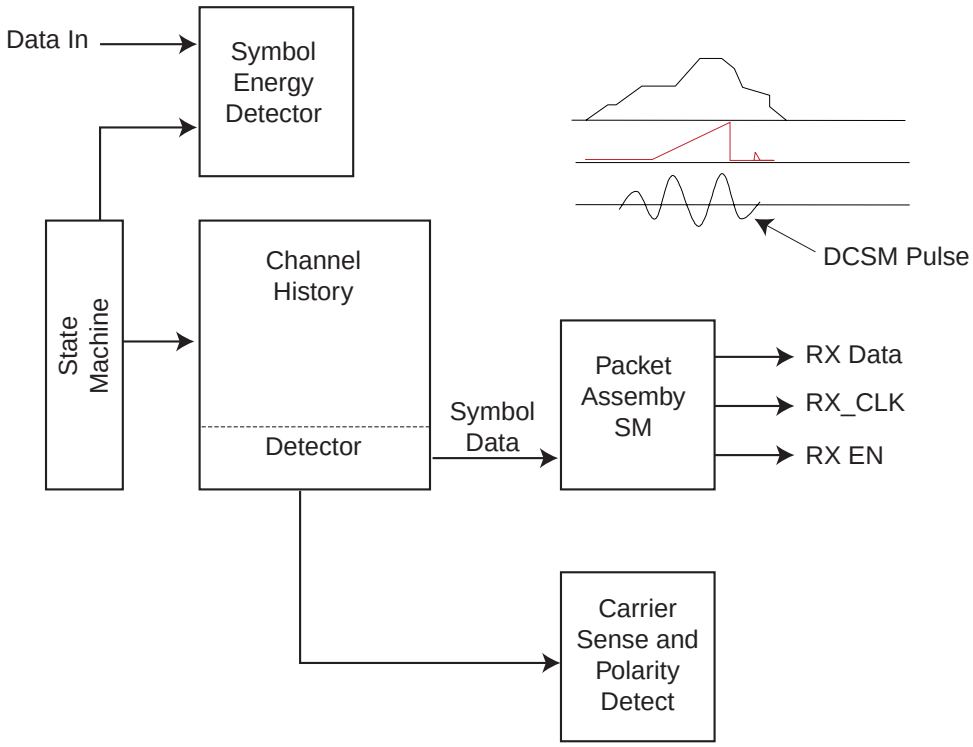


Figure 11. HomePNA Interoperability (1Mbps) Pulse Detector

INTERFACES

MII Interface

TX_D0:TX_D3, RX_D0:RX_D3, TX_EN, TX_CLK, TX_ER, RX_DV, RX_CLK, RX_ER, COL, CRS, MDC, MDIO, MD_ADD0:MD_ADD4

The MII interface implemented in the CPC6000 device is compatible with the IEEE 802.3u specification, and constitutes 18 pins. In that specification, MII interface registers are defined such that the first 16 registers must have defined or reserved values in them. These registers constitute the basic and part of the enhanced register set. Registers 16 – 32 are defined as extended AND "vendor specific" by the IEEE. Note that registers 2 and 3 expect to be filled in with the OUI (Organizationally Unique Identifier, which for CP CLARE is 0x00-30-15), the manufacturers model number, and the revision number. This allows the host software (NDIS driver) the option of booting with vendor specific code that can drive the vendor specific registers correctly.

The CPC6000 uses this vendor specific register area to manage the interaction between a standard 802.3 MAC and the phoneline PHY. As per the 802.3u specification, these registers are read and written to over the MII management interface, which has its protocol, pins, and timing, specified. The registers are updated by data transmitted on the MDIO pin and clocked in and out of the registers by the MDC pin. The registers and definitions are defined in the following section.

On boot-up, the system software driver will poll the status of the MD_ADD0:MD_ADD4 pins to determine the MII hardware address. The 802.3 specification allows for 32 independent devices to be attached to the MAC any one of which can be operational at one time. The user can use pull up or pull down resistors externally to force the appropriate address desired to be read by the MAC.

MII Vendor Specific Register Definitions

Note - the TYPE field has the following meanings:

RW = read/write bit

RW/SC = read/write self clearing

RO = read only

RO/LL = read only latch low, cleared on read

RO/LH = read only latch high, cleared on read

Register 0 – Control Register

This is a basic register that must be included in every MII interface. The register is set for 100 Mb/s operation, and defaults by tri-stating the MII interface at boot-up. Bits 9, 8, 6, 5, 4, 3, 2 and 1 are ignored by the CPC6000 PHY.

BIT #	DEFAULT	NAME	DESCRIPTION	TYPE
15	0	Reset	Sets PHY in Reset state	RW/SC
14	0	Loopback	Loopback disabled	RW
13	1	Speed select	Combined with bit 6	RW
12	0	Auto-Negotiate	0 = Disable Auto-Negotiation	RW
11	0	Power Down	1 = Enable Power Down	RW
10	1	Isolate	1 = Electrically Isolate PHY from MII	RW
9	0	Restart Auto-Neg	1 = Restart, 0 = Normal Operation	RW/SC
8	0	Duplex Mode	Set in half duplex mode	RW
7	0	COL Test	1 = Enable COL signal test	RW
6	0	Speed select	MSB. Sets PHY in 100Mb/s mode	RW
[5:0]	0	Reserved	Write as 0	RW

Register 1 – Status Register

This is also a basic register and must be included with every MII interface. Bits 6, 5, 4, 3 and 1 are ignored by the CPC6000 PHY.

BIT #	DEFAULT	NAME	DESCRIPTION	TYPE
15	0	100 BaseT4	Set to unable to perform 100BaseT4	RO
14	0	100BaseX FD	Set to unable to perform 100BaseX Full Duplex	RO
13	0	100BaseX HD	Set to unable to perform 100BaseX Half Duplex	RO
12	0	10Mb/s FD	Set to unable to perform 10Mb/s Full Duplex	RO
11	1	10Mb/s HD	Set to ABLE to perform 10Mb/s Half Duplex	RO
10	0	100BaseT2 FD	Set to unable to perform 100baseT2 Full Duplex	RO
9	0	100BaseT2 HD	Set to unable to perform 100baseT2 Half Duplex	RO
8	0	Extended Status	No extended status in register 15	RO
7	0	Ignore	Ignore this when read	RO
6	0	MF Preamble	Set to force management frames with preamble	RO
5	0	Auto-neg Complete	Set to Auto-negotiation NOT complete/Not capable	RO
4	0	Remote Fault	Default is no remote fault condition detected	RO/LH
3	0	Auto-negotiate	Set to unable to Auto-negotiate	RO
2	1	Link status	Default is set to Link status up	RO/LL
1	0	Jabber Detect	Set to No Jabber condition detected	RO/LH
0	1	Extended Registers	Set to use upper 16 registers for JackRabbit?	RO

Register 2 – PHY Identifier Register

This register contains bits 3 to 18 of the Organizationally unique Identifier, where bit 3 of the OUI is mapped to the MSB of register 2. This register is “hard-wired” and Read Only.

BIT #	DEFAULT	NAME	DESCRIPTION	TYPE
[15:0]	0000 0000 0011 0010	OUI	OUI is mapped per IEEE specification	RO

Register 3 – PHY Identifier Register

This register holds the remaining bits of the OUI (bits 19 to 24, with bit 19 of the OUI mapped to the MSB of register 3), the manufacturer’s model number, and the revision number.

BIT #	DEFAULT	NAME	DESCRIPTION	TYPE
[15:10]	10 1000	OUI	Upper 6 bits of the OUI	RO
[9:4]	00 0000	Mfr. Model #	Read CP Clare Model number	RO
[3:0]	0	Mfr. Rev. #	Read CP Clare Revision number	RO

Registers 4 – 8: Auto-negotiation Registers

These registers will be set to all 0’s since Auto-negotiation is turned off since it has no meaning in phoneline PHY silicon. These are read only as they are never used and should not be changed.

BIT #	DEFAULT	NAME	DESCRIPTION	TYPE
[15:0]	0000 0000 0000 0000	Auto-Neg. Regs.	Auto-negotiation registers	RO

Registers 9 & 10: 100 BaseT2 Control and Status Registers

The 100 BaseT2 control register is a RO register with defaults at 0. This will be set to all 0's. The status register is RO, and will be set to all 0's.

BIT #	DEFAULT	NAME	DESCRIPTION	TYPE
[15:0]	0000 0000 0000 0000	100BaseT2	100BaseT2 control and status registers	RO

Registers 11 to 14: Reserved Registers

These registers are reserved by the IEEE, and are all set to 0's and are read only.

BIT #	DEFAULT	NAME	DESCRIPTION	TYPE
[15:0]	0000 0000 0000 0000	Reserved	Reserved by the IEEE	RO

Register 15 – Extended Status Register

This register is implemented only for PHY's capable of speeds over 100Mb/s, and as such, will be set to all 0's and be read only.

BIT #	DEFAULT	NAME	DESCRIPTION	TYPE
[15:0]	0000 0000 0000 0000	Ext. Status	Used for 1Gb/s LAN's status	RO

Register 16 - CPC6000 PHY Control Register

This register prevents non-JackRabbit™ PHY aware MACs from inadvertently writing into the JackRabbit™ PHY specific registers.

BIT #	DEFAULT	NAME	DESCRIPTION	TYPE
10	0	Reserved	Bit reserved for future use	R/W
9	0	Turbo Status	Turbo link status. 1=turbo packet detached	R/W
8	1	1M8 Sense	Identifies 1M8 packet source. 0=legacy detect only	R/W
4	1			
2	0	Legacy 1M8	Set if legacy 1M8 source detected. Invalid if Bit 8=0	R/W
1	0	CPC6000 1M8	Set if CPC6000 1M8 source detected. Invalid if Bit 8=0	R/W

Registers 17 – 23: Unused Registers

These registers are not being used by the CPC6000 PHY, and will be read back as all 0's.

BIT #	DEFAULT	NAME	DESCRIPTION	TYPE
[15:0]	0000 0000 0000 0000	Unused	Unused registers	RO

Register 24: CPC6000 Clock Control Register

The register is used to set the internal clock registers.

BIT #	DEFAULT	NAME	DESCRIPTION	TYPE
[15:13]	101	Reserved	Reserved for PHY	
[12:9]	1 110	PLL 60 count	Sets PLL counter for 60MHz internal clock	R/W
8	0	Reserved	Reserved	R/W
7	0	Forced Turbo	Sets PHY to Turbo Mode Only. 1=Forced Turbo	R/W
6	0	Forced 1M8	Sets PHY to 1M8 Mode Only. 1=Forced 1M8	R/W
5	0	Reserved	Reserved for PHY	
[4:0]	1 1111	PLL 80 count	Sets PLL counter for 80MHz internal clock	R/W

Register 25-26: CPC6000 PHY Scratch Pad Registers

These registers are used internally by the PHY. Do not read or write to these registers. A read to these registers will return undefined values.

BIT #	DEFAULT	NAME	DESCRIPTION	TYPE
[15:0]	Random-undetermined	Reserved	Reserved for PHY	RO

Registers 27 – 29: Unused Registers

These registers are not being used by the CPC6000 PHY, and will be read back as all 0's.

BIT #	DEFAULT	NAME	DESCRIPTION	TYPE
[15:0]	0000 0000 0000 0000	Unused	Unused registers	RO

Register 30: User Data Channel

BIT #	DEFAULT	NAME	DESCRIPTION	TYPE
[15:12]	Random	Reserved	Bit reserved for future use	RO
[11:10]	11	Turbo Speed	Rx packet speed. 11=10Mbps, 10=5Mbps, 01=2Mbps, 00=1Mbps	RO
9	0	1M8 Packet	Rx 1M8 packet	RO
8	0	New Data	Set to 1 if user data is new since last read	RO
[7:0]	Random	User Data	User data byte. Remains valid until register is read	RO
9	0	Data Enable	Enable for interrupt on new user data	WO
[7:0]	Random	User Data	Sets new bit on receiving PHY when written	WO

Register 31: R16 Alias

This register uses the lower bits as an alias to register 16 for programming convenience, other bits are unused and should be read as 0's.

BIT #	DEFAULT	NAME	DESCRIPTION	TYPE
[15:4]	0000 0000 0000	Unused	Unused registers	RO
[3:0]	R16 [15:12]	R16 Alias	Alias for Register 16 bits [15:12]	RO

The MII interface receives nibble wide data from an industry standard 802.3 MAC, performs parallel to serial conversion, and shifts the data into a transmit scrambler. The data is clocked in on the rising edge of TX_CLK when TX_EN is enabled (driven high) on the first nibble of the preamble. There is no buffering of data between the MII and scrambler so that no measurable delay is inserted into the transmission path.

The MII also transmits nibbles received from the descrambler to an industry standard 802.3 MAC by performing serial to parallel conversion on a nibble of data. The data is clocked out on the rising edge of RX_CLK when RX_EN is enabled (driven high) beginning with the SFD (Start of Frame Delimiter).

In the present implementation, neither TX_ER nor RX_ER is connected to any logic inside the CPC6000.

Collision detect is determined and the COL signal is asserted if a collision is detected on the twisted wire medium during the silence period of the Ethernet preamble (see fig 4 for the HomePNA Version 1.1 silence period). Back-off timing is determined by the 802.3 standard BEB algorithm.

Carrier sense is asserted when either the transmit or the receive silicon blocks are active. As per the HomePNA version 1.1 specification, carrier will be asserted within 815nS after the detection of a valid pulse. It will also be turned off after the receiver has sensed no voltage above the squelch limit for 29.8uS (if it has been 120uS since carrier asserted), or 16uS if longer than 120uS since carrier asserted. In Turbo mode, the CRS is turned off 2BT (bit times) after the conclusion of the frame reception.

A block diagram of the MII interface is shown in Figure 12.

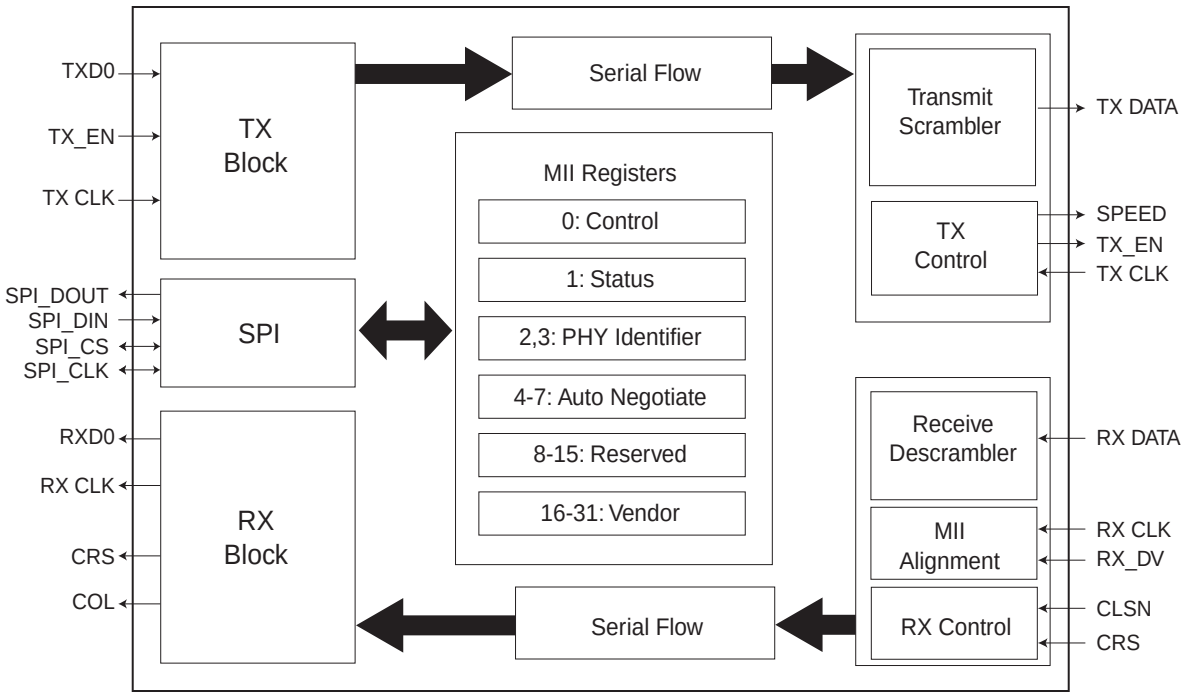


Figure 12. MII Interface Block Diagram

Seven Wire Serial (GPSI) Interface

Note: The GPSI interface mode will not be active in first version (CPC6000A) silicon.

TX_D0, RX_D0, TX_EN, TX_CLK, RX_CLK, COL, CRS, GPSI_EN

Typically used as the digital interface in a USB MAC or a PCMCIA MAC application, the GPSI interface is an industry standard 7-wire interface used in many 10BaseT Ethernet designs. The seven signals (TX_D0, RX_D0, TX_EN, TX_CLK, RX_CLK, COL, and CRS) that comprise the GPSI interface also serve the same function in the MII interface. The major difference between this interface and the MII interface is that the TX_CLK and RX_CLK are continuous in MII mode, but are gapped in GPSI mode. The GPSI interface is enabled in the PHY by holding the GPSI_EN pin low during the reset pulse.

Table 1 – GPSI Interface Signals

Signal	Description
TX_CLK	Transmit clock
TX_EN	Transmit enable
TX_D0	Transmit data
RX_CLK	Receive clock
RX_D0	Receive data
CRS	Receive carrier sense
COL	Collision (active high)

Serial Peripheral Interface

SPI_DI/MDIO, SPI_DOUT, SPI_CLK/MDC, SPI_CS

This is a simple 4-trace interface – SPI_DIN, SPI_DOUT, SPI_CS, and SPI_CLK. This interface is used in conjunction with the GPSI port to commute speed change information to the modulator from the MAC. Since there are neither registers nor any management interface, the SPI port acts like an MII management interface when used with a GPSI port. This port is double buffered and serial so that as data is shifted in serially on the rising edge of SPI_CLK, it is also shifted in parallel into the second buffer when SPI_CS goes high. In effect, SPI_CS acts like a load strobe to shift data from the serial buffer into the parallel buffer. Figure 13 shows the second-generation PHY silicon (CPC6000B) to MAC interface when configured in GPSI mode (and thereby also configuring the SPI interface).

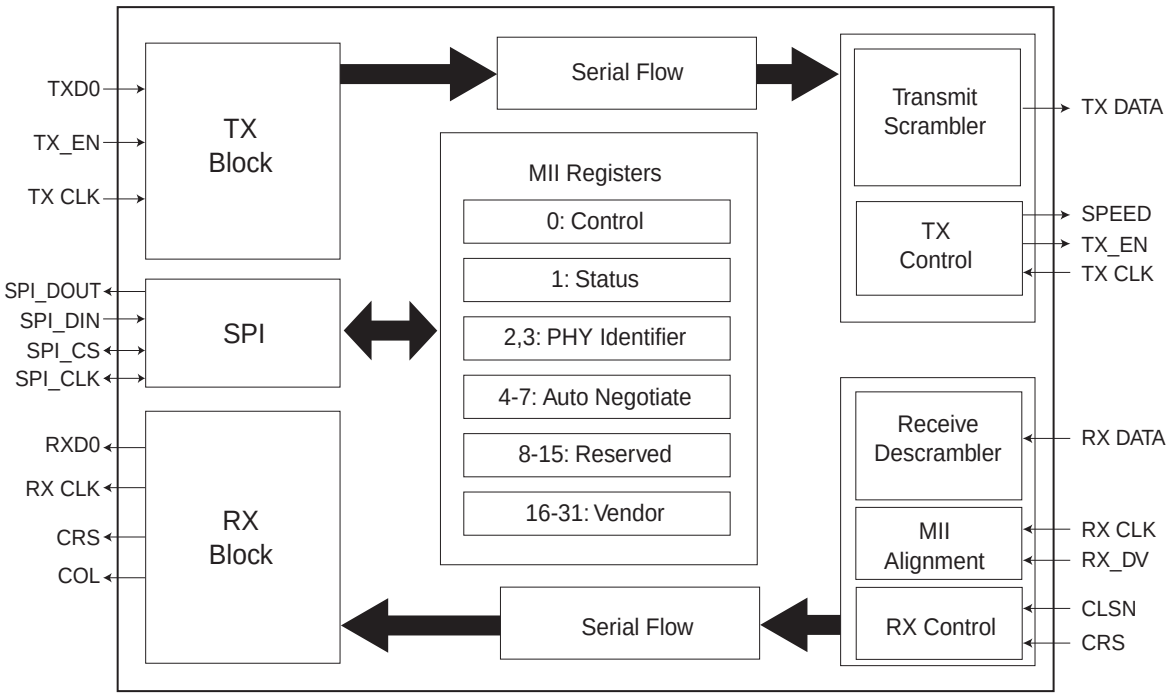


Figure 13. GPSI and SPI Port Interfaces

COMPARATOR (ADC) INTERFACE

N_COMP, G_COMP, P_COMP PINS, MANCH_CLK

These pins connect the demodulator inside the modem to comparators inside the AFE. The pins ending with 1 are those in the main receive path from the twisted pair wire for HomePNA transmissions. The second set, those ending with a 2, are used to receive transmissions from an Ethernet NIC card in the "dongle" mode from a second set of comparators inside the AFE. In this dongle mode, transmissions received from the Ethernet NIC are demodulated through the endec and routed through the CPC6000 modulator for the DAC to twisted pair wire in the transmit path. Conversely, signals received from the twisted pair wire are received through the "1" set of comparators, demodulated, and sent through the Manchester transmit pins (MANCH_P, MANCH_N) to the Ethernet NIC card. The voltages on these wires are compatible with either 3.3V or 5V interface logic. These traces are directly connected between the two chips, and no external components are required (pull-ups, etc.). The sampling rate on comparator set number 1 is driven by the DAC_CLK, and the second set of comparators is clocked by the MANCH_CLK pin on the 80 pin device.

N_REF1,2 G_REF1,2 PREF1,2 SIG_IN1,2

These are analog inputs to the AFE comparators from the twisted pair wire. All inputs ending with a 2 are inputs from an Ethernet NIC card for use in a dongle application previously described where one end communicates with an Ethernet NIC card and the other with standard twisted pair wire. All inputs ending with a 1 are directly connected

with the twisted pair wire. The N_REF, G_REF, AND P_REF signals are connected to the inverting end of the comparator, and the SIG_IN signal represents the input from the wire through an anti-aliasing filter. All of the positive inputs to the comparators are connected to the SIG_IN trace.

DAC INTERFACE

DAC0:DAC7, DAC_CLK, DAC_SCAL

These pins directly connect the modulator and 8 bit DAC inside the AFE. These traces require no external discrete devices between chips such as pull-ups, etc. Inside the AFE, digital inputs are latched on the rising edge of DAC_CLK, which drives the update rate up to 125mS/S. DAC_CLK is an output from the modem and is either directly connected through the modem to the modem's input clock, or is fed from a divided down modem clock. The data inputs are compatible with either 3.3V or 5V logic. The DAC_SCAL output from the modem to the AFE determines which set of coefficients to use from the internal LUT to be sent to the DAC so as to adjust the drive current for either HPNA interoperability or Turbo mode operation. This is accomplished by setting the bias inside the AFE through a FET which switches in a resistor in parallel thereby setting the reference voltage inside the AFE.

I_POS, I_NEG

These signals represent a differential analog output signal and are directly connected from the DAC output on the AFE to a center-tapped transformer through a bandpass filter and an amplifier. These are current outputs, and can be adjusted from 2mA to 10mA which represents the full swing output without any degradation of signal quality. An external drive circuit is all that is required to connect to the twisted pair wire. The output capacitance is less than 5pF.

ETHERNET NIC DONGLE INTERFACE

Note: The Dongle interface will not be active in first generation (CPC6000A) silicon.

MANCH_P AND MANCH_N

These pins are capacitively coupled to an AUI transformer on an industry standard 802.3 compliant Ethernet NIC card. These pins provide a Manchester encoded pulse that emulates the analog pulses required for connection to a RX+ and RX- connection from a twisted pair wire to a standard NIC card. As described above, the flow of this data connection is actually from the twister pair through the COMP2 section of the AFE (see the comparator section above), through the demodulator circuit in the digital chip, and then out the MANCH_P AND MANCH_N pins to the NIC card. The voltage swing on these pins is from (TBD)V to (TBD)V.

CLOCKS

INPUT CLOCK OPTIONS

OPTION 1: CLK_IN_80, CLK_IN_60 SIGNALS

These signals are inputs from standard crystal oscillators that provide the master clock to both the CPC6000 digital PHY and CPC6100 AFE. They provide the sampling rate on the DAC for data transmission and the oversampling rate in the modem. A .1uF bypass capacitor is connected between the OE and GND pins of the oscillator. In addition, a 10-Ohm resistor is placed in series between the Vcc pin and the +5V power plane. The output of the oscillator is connected directly to the clock inputs. The tolerance on the oscillators shall be +/- 50ppm with an allowable jitter of <1nS max.

OPTION 2: XTAL1, XTAL2, PLL_80_If2, PLL_60_If2:

These are the inputs for the 25MHz crystal that drives the internal PLL's incorporated in the CPC6000. The crystal shall be of fundamental frequency with a tolerance of +/- 50ppm. The PLL will be connected to an external filter for each frequency (80MHz and 60MHz) and then connected to digital ground. The internal PLL will output the fundamental clocks for all internal functions with the 80MHz clock driving all Turbo mode (10Mbps) operations and the 60MHz clock used for all HomePNA interoperability (1Mbps) operations.

OUTPUT CLOCK

CK_25

This is a 25MHz output clock used to drive the MAC so that no external clocking source is required for that device. This clock will also have a tolerance of +/-50ppm with an allowable jitter of <1nS.

PINS FOR DEVICE TESTING

TEST_XMIT1, TEST_XMIT10, CK_60_MON

These pins are used to test the silicon. They should be treated as a no connect and left floating. Essentially, the pins will force either HomePNA interoperability mode or 10Mbps Turbo mode only; not both or either.

MISCELLANEOUS PINS

LEDS: LINK_ACT, RX_MODE:

The LINK_ACT pin will output a 16mA source current to drive an LED when the Link is considered active; if there has been receive activity within the last 4 seconds.

The RX_MODE pin will be an indicator for the mode of operation (HomePNA interoperability or Turbo) chip is currently operating. It

will source a 16mA current if the chip is operating in Turbo mode.

INTA PIN

This pin provides a standard logic signal from the CPC6000 to signal the host to read both the MII status register and the JackRabbit™ status register. This is provided for software drivers that would prefer an interrupt driven MII interface rather than a standard 802.3 polled interface. If this pin is not connected, it should be left floating as a NC signal.

RESET PIN

This pin, when activated, will reset the CPC6000 device and return all MII register settings to their default state. This pin is active high, and should have a pull down resistor on the trace for normal operation. Pulling the pin high for a period of (TBD)mS will activate the reset signal. Note that reset of the device can also be effectuated by the host software driver. A 0 is written to bit 15 in the MII control register to begin the reset process.

Rref:

This pin is used for setting a reference for the PLL incorporated in the CPC6000 and should be tied through a 6.19K resistor to digital ground.

R_BIAS

This pin is used to set a reference inside the CPC6100 AFE and should be tied through a 4K resistor to digital ground. Note that this pin is also connected through a FET in parallel through another 4K resistor to the DAC_SCAL pin on the CPC6000 digital PHY.

RB/DD

This pin acts as a voltage divider inside the CPC6100 AFE and should be connected through a 2K resistor to digital power.

PHONELINE INTERFACE EXTERNAL COMPONENTS

LINE DRIVER

The line driver is a high speed voltage feedback amplifier with 160MHz bandwidth and 160V/uS slew rate for fast settling time and high speed data transfer rates that peak at 10Mb/s. It is capable of driving 50mA from a single +5V supply. It takes a differential signal from the DAC and outputs a single trace output to the transformer. The driver provides > -85dB of harmonic distortion at 1MHz.

RECEIVE PATH

The receive path contains an active/passive bandpass 4-pole filter with amplifiers that provide (TBD)dB of gain to the incoming signal. The gained signal is further sent to a limiting section which soft-limits the signal to +/- 500mV max through 5GHz transistors. The limiting section also provides a further gain of (TBD)dB. This provides enough of a gain to correlate 10mVp signals as well as limit 2.5V signals from closely spaced HomePNA 1Mbps nodes so as not to saturate the receiver section.

ISOLATION

This is a 1:1 ferrite transformer that provides 1500Vrms of isolation from line transients or power crosses that might occur due to the fact that home telephone wires are connected directly to the PSTN. The signal rise time is 3.5nS maximum, and the leakage inductance is less than .2uH. In addition, the DCR is .200hms max, and the inductance at 100KHz and .01Vrms is 100uH.

TRANSMIT FILTER

A fourth order bandpass filter is utilized to pass JackRabbit™ standard frequencies while removing noise and other carrier frequencies from interfering with the demodulation process. The output of the filter is a 5.5MHz to 24.5MHz frequency band that is sent to the line driver.

FRONT END PROTECTION

The circuitry from the transformer to the twisted pair wire is known as the front-end circuitry. Since it is connected in parallel with POTS telephone service, protection must be provided from central office supervisory signaling such as ringing. Therefore, two .001uF, 250V DC blocking capacitors are required as well as two ferrite beads and a sidactor for voltage surges such as lightening strikes. These discrete devices are typically found on most voice band modems for the same reasons as those mentioned above.

ELECTRICAL CHARACTERISTICS

OPERATING CONDITIONS (CPC6000 and CPC6100)

Maximum Guaranteed Ratings:

Operating Temperature: 0°C – 70°C

Storage Temperature: -40°C – 125°C

Soldering Temperature: 225°C for 10sec.

Positive Voltage on any pin: Vdd +.5V

Negative Voltage on any pin: Vdd - .5V

Maximum: Vdd: 7V

CPC6000 DC ELECTRICAL CHARACTERISTICS

(Ta = 0°C – 70°C, Vdd = 3.3V +/- 5%)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNITS	CONDITIONS
Input						
Voltage level high	Vih	Vdd-.75		Vdd+.75	V	
Voltage level low	Vil	0		0.75	V	
Current level High	Iih		5		uA	
Current level low	Iil		-5		uA	No pull up
Pin cap to GND			10		pF	Includes package
Output						
Voltage level high	Voh	Vdd-.5		Vdd+.5	V	-7mA
Voltage level low	Vol	0		0.5	V	+7mA
Current level high	Ioh	-				Measured on AFE
Current level low	Iol	-				Measured on AFE
Rise time			4		nS	.4V to 2.5V into 20pF load
Fall time			4		nS	2.5V to .4V into 20pF load
Pin cap to GND			10		pF	
Supply Current						
HomePNA mode active			TBD		mA	suspect below 100mA
Turbo mode active			TBD		mA	
Low power mode			TBD		mA	

CPC6000 AC ELECTRICAL CHARACTERISTICS

(Ta = 0°C – 70°C, Vdd = 3.3V +/- 5%)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNITS	CONDITIONS
CLK_IN_80		+/- 50ppm			MHz	
Duty cycle		40		60	%	
CLK_IN_60		+/- 50ppm			MHz	
Duty Cycle		40		60	%	
RX_CLK						
TX_CLK						
MDC						

CPC6100 DC ELECTRICAL CHARACTERISTICS

(Ta = 25decC, Vdd = 3.3V +/-5%)

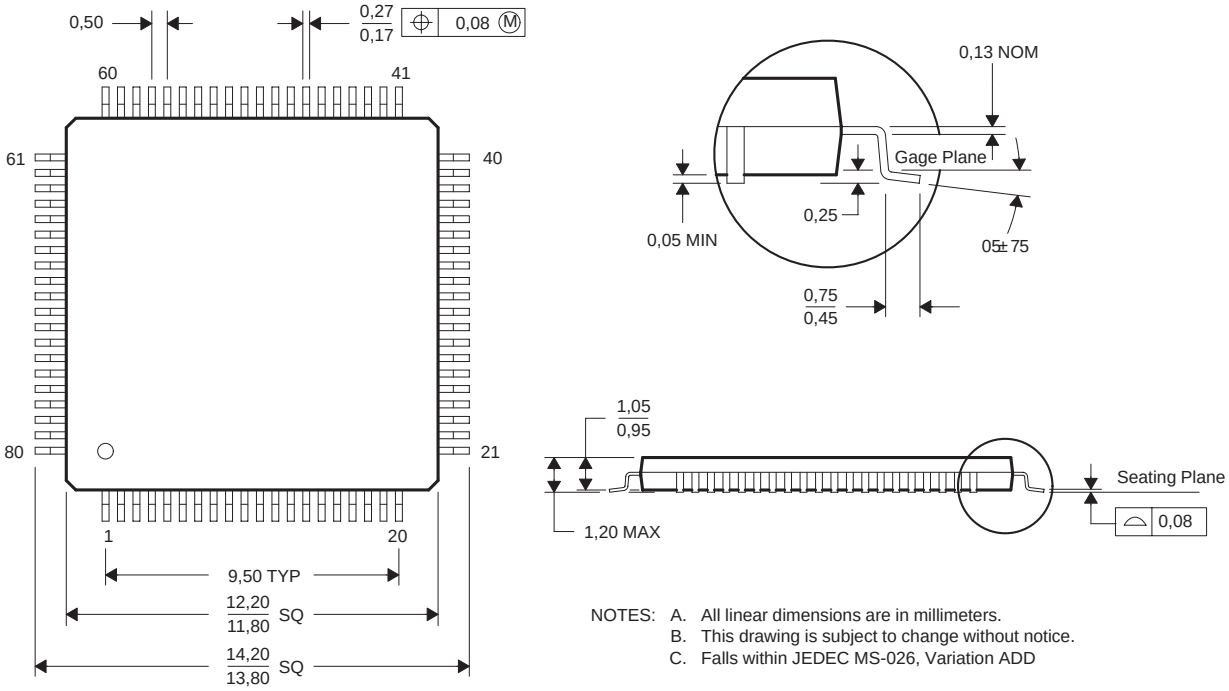
CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNITS	CONDITIONS
INPUT (digital)						
Voltage level high	Vih	Vdd-.4		Vss+.4	V	
Voltage level low	Vil	Vss		0.75	V	
Current level High	Iih		5		uA	
Current level low	Iil		-5		uA	No pull up
Pin cap to GND			10		pF	Includes package
OUTPUT(digital)						
Voltage level high	Voh	Vdd-.6		Vss+.6	V	-7mA
Voltage level low	Vol	0		0.5	V	+7mA
Current level high	Ioh		-			Measured On AFE
Current level low	Iol		5			Measured on AFE
Rise time			5		nS	.4V to 2.5V into 20pF load
Fall time			5		nS	2.5V to .4V into 20pF load
Pin cap to GND			10		pF	
INPUT(analog)						
Voltage range:						
P_REF		0		0.5	V	
G_REF		0		0.4	V	
N_REF		-0.4		0	V	
SIG_IN		-0.5		0.5	V	
OUTPUT(analog)						
Voltage range:			20		mA	
V_OUT+, V_OUT-		-1		1.25	V	Current source driver, but max voltage compliance
Supply Current						
HomePNA active			55		mA	
Turbo active			60		mA	
Low power mode			36		mA	
Propagation Delay						
Transmit delay			10		nS	
Receive delay			20		nS	
DAC Specs.						
Resolution			8		Bits	
Monotonicity			guaranteed		Guaranteed	
Integral linearity error		-1		1	LSB	
Differential Nonlinearity		-1		1	LSB	
Offset error		-0.01		0.01	%FSR	
Gain error		-10		10	%FSR	
Full scale output current			10		mA	
Output Resistance			100		KΩ	
Output capacitance			TBD		pF	
Internal Vref		1.15		1.29	V	
Internal Rref		11		65	KΩ	
Offset Drift			TBD		PPM	
Gain Drift			TBD		PPM	
Comparator Specs.						
Input offset Voltage			+/-25		mV	
Input Capacitance			10		pF	
Min overdrive V				50	mV	

CPC6100 AC ELECTRICALSPECIFICATIONS

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNITS	CONDITIONS
DAC Characteristics						
Max Update rate			80		ms/S	Maximum rate
Output settling time			TBD		nS	Looking for under 35nS for full s
Glitch impulse			TBD		PV-S	Looking for max 5
Output rise time			1		nS	
Output fall time			TBD		nS	Looking for >-50 all conditions
SNDR			TBD		dB	Looking for >-60 all conditions
THD			TBD		dBc	Looking for >60 all conditions
Dynamic range			TBD		dBc	
Comparator Specifications						
Max input sig Freq			15		MHz	
Propagation delay			TBD		nS	Looking for <23nS
Max output update rate			80		ms/S	

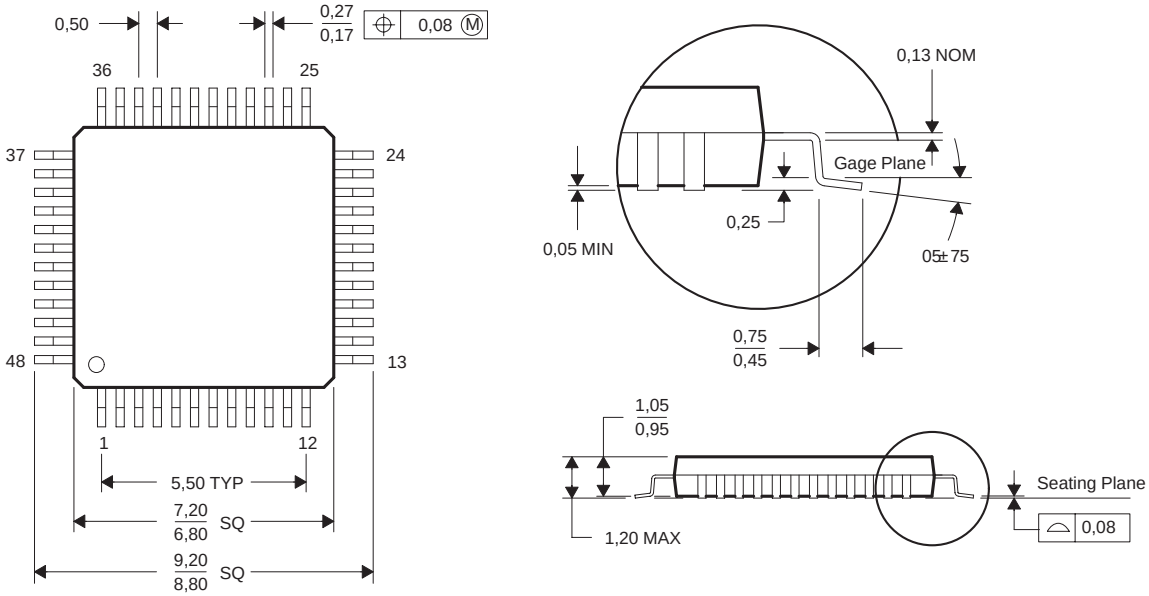
Mechanical Dimensions

CPC6000 PHY



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026, Variation ADD

CPC6100 AFE



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026, Variation ABC

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Specification: DS-CPC6000/CPC6100-R0A

3/13/00

** JackRabbit™ utilizes Cosine Segment Modulation (CSM), Dual Carrier Segment Modulation (DCSM) and Adaptive Template Demodulation (ATCD) which are patent and patent pending technologies of X-Com Inc., Mannasses, VA, USA*