Common single PWM Controller with Multiform supply Voltage

Features

- **Adjustable Output Voltage from +0.6V to +5.0V**
  - **0.6V Reference Voltage**
  - **±0.6% Accuracy**
- **Operates from An Input Battery Voltage Range of +3V to +25V**
- **Multiform Purpose Input Voltage Collocation**
  - **V_{CC}=5V / V_{IN}=8~19V For NB application**
  - **V_{CC}=5~12V / V_{IN}=5~12V For table PC application**
- **Remote Feedback Sense for Excellent Output Voltage Regulation**
- **Power-On-Reset Monitoring on VCC pin**
- **Excellent line and load transient responses**
- **Ultrasonic Operation Eliminated Audio Noise**
- **PFM mode for increased light load efficiency**
- **300kHz Constant PWM Switching Frequency**
- **Integrated MOSFET Drivers**
- **Integrated Bootstrap Forward P-CH MOSFET**
- **Adjustable Integrated Soft-Start**
- **Power Good Monitoring**
- **70% Under-Voltage Protection**
- **125% Over-Voltage Protection**
- **Adjustable Current-limit protection**
  - **Using Sense Low-Side MOSFET's RDS(ON)**
- **Over-Temperature Protection**
- **TDFN3x3-10 Package**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

- **Notebook**
- **Table PC**
- **Hand-Held Portable**
- **AIO PC**
- **Wide input DC/DC Regulators**

General Description

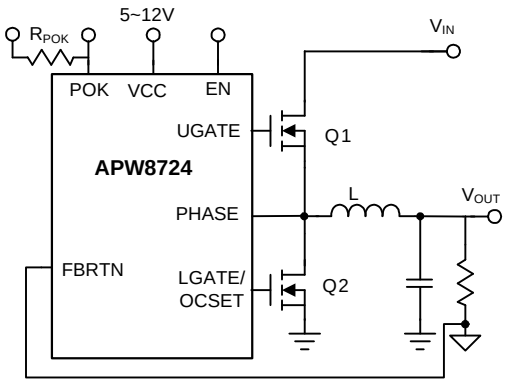
The APW8724 is a single-phase, constant on-time, synchronous PWM controller, which drives N-channel MOSFETs. The APW8724 steps down high voltage to generate low-voltage chipset, RAM supplies in notebook computers or mother board applications.

The APW8724 provides excellent transient response and accurate DC voltage output in either PFM or PWM Mode. In Pulse Frequency Mode (PFM), the APW8724 provides very high efficiency over light to heavy loads with loading-modulated switching frequencies. In PWM Mode, the converter works nearly at constant frequency for low-noise requirements. The unique ultrasonic mode maintains the switching frequency above 37kHz, which eliminates noise in audio application. APW8724 is built in remote sense function for applications that require remote sense.

The APW8724 is equipped with accurate positive current limit, output under-voltage, and output over-voltage protections, perfect for multiform applications. The Power-On-Reset function monitors the voltage on VCC to prevent wrong operation during power-on. The APW8724 has an internal 4ms digital soft start that ramps up the output voltage with programmable slew rate to reduce the start-up current. The enable function can let user easy to apply APW8724.

The APW8724 is available in 10pin TDFN 3x3 package respectively.

Simplified Application Circuit



ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Rev. A.1 - Jan., 2013

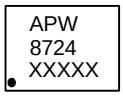
Ordering and Marking Information

APW8724 □□-□□□

- Assembly Meterial
- Handling Code
- Temperature Range
- Package Code

Package Code
QB:TDFN3x3-10
Temperature Range
I : -40 to 85 °C
Handling Code
TR: Tape & Reel
Assembly Meterial
L: Lead Free Device G : Halogen and Lead Free Device

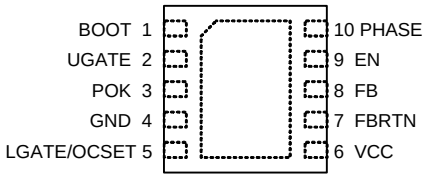
APW8724QB:



XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Pin Configuration



TDFN-10 3X3
(top view)

= GND and Thermal Pad (connected to GND plane for better heat dissipation)

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{CC}	VCC Supply Voltage (VCC to GND)	-0.3 ~ 16	V
$V_{BOOT-GND}$	BOOT Supply Voltage (BOOT to GND)	-0.3 ~ 44	V
V_{BOOT}	BOOT Supply Voltage (BOOT to PHASE)	-0.3 ~ 16	V
V_{EN}	EN to GND	-0.3 ~ V_{CC}+0.3	V
	All Other Pins (POK, FBRTN and FB to GND)	-0.3~7	V
	UGATE Voltage (UGATE to PHASE) <20ns pulse width >20ns pulse width	 -5 ~ V_{BOOT}+0.3 -0.3 ~ V_{BOOT}+0.3	V
	LGATE Voltage (LGATE to GND) <20ns pulse width >20ns pulse width	 -5 ~ V_{CC}+0.3 -0.3 ~ V_{CC}+0.3	V
V_{PHASE}	PHASE Voltage (PHASE to GND) <20ns pulse width >20ns pulse width	 -5 ~ 35 -0.3~ 28	V

Absolute Maximum Ratings (Cont.) (Note 1)

Symbol	Parameter	Rating	Unit
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Soldering Temperature, 10 Seconds	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Thermal Resistance -Junction to Ambient (Note 2) TDFN3x3-10	55	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of package is soldered directly on the PCB.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{IN}	Converter Input Voltage	3 ~ 25	V
VCC	VCC Supply Voltage	4.5 ~ 13.2	V
V_{OUT}	Converter Output Voltage	0.6~5	V
I_{OUT}	Converter Output Current	0~25	A
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3: Refer to the application circuit for further information.

Electrical Characteristics

These specifications apply for TA = -40°C to +85°C, unless otherwise stated. All typical specifications TA= +25°C, V_{CC} = 12V

Symbal	Parameter	Test Condition	APW8724			
			Min.	Typ.	Max.	Unit
Reference VOLTAGE						
V_{REF}	Reference Voltage		-	0.6	-	V
	Regulation Accuracy	T_A = 25 °C	-0.6	-	+0.6	%
		T_A = -40 °C ~ 85 °C, Line / Load Transient	-1.0	-	+1.0	%
I_{FB}	FB Input Bias Current	FB=0.5V	-	-	1	µA
I_{FBRTN}	FBRTN Leakage Current		-	-	1	µA

Electrical Characteristics

These specifications apply for TA = -40°C to +85°C, unless otherwise stated. All typical specifications TA= +25°C, V_{CC} = 12V

Symbal	Parameter	Test Condition	APW8724			
			Min.	Typ.	Max.	Unit
SUPPLY CURRENT						
I_{VCC}	VCC Input Bias Current	VCC Current, EN=5V, VFB=0.7V, PHASE=0.5V	-	2	3	mA
I_{VCC_SHDN}	VCC Shutdown Current	EN=GND, VCC=5V	-	-	10	µA
SWITCHING FREQUENCY AND DUTY						
T_{ON}	PWM On Time	V_{in}=12V, VOUT=1V	222	278	333	ns
$T_{ON(MIN)}$	Minimum on time		-	100	-	ns
$T_{OFF(MIN)}$	Minimum off time	V_{FB}=0.45V, V_{PHASE}=-0.1V	300	400	500	ns
	Minimum Ultrasonic Skip Operating Frequency		25	37	-	kHz
Power On Timing						
	Maximum Current Limit Setting Time	R_{OCSET} is open	-	-	500	µs
D1 only	I_{OCSET} Early Sourcing Timing	From POR_R to Internal sample clock start	-	150	-	µs
	The First Pulse Delay by EA Offset	Positive Offset 60mV(Typ.), When T_{SS} is about 4ms, the first pulse delays from sample & hold completed	-	350	-	µs
T_{SS}	Internal Soft Start Time	V_{OUT}=0% to V_{OUT} Regulation(95%)	-	4	-	ms
GATE DRIVER						
	5V UG Pull-Up Resistance	VCC=5V, BOOT-UG=1V	-	5	-	Ω
	12V UG Pull-Up Resistance	VCC=12V, BOOT-UG=1V	-	3	-	Ω
	5V UG Sink Resistance	VCC=5V, UG-PHASE=1V	-	2	-	Ω
	12V UG Sink Resistance	VCC=12V, UG-PHASE=1V	-	1.3	-	Ω
	5V LG Pull-Up Resistance	VCC=5V, VCC-LG=1V	-	5	-	Ω
	12V LG Pull-Up Resistance	VCC=12V, VCC-LG=1V	-	3	-	Ω
	5V LG Sink Resistance	VCC=5V, LG-GND=1V	-	2	-	Ω
	12V LG Sink Resistance	VCC=12V, LG-GND=1V	-	1.3	-	Ω
	UG to LG Dead time	UG falling to LG rising at VCC=5V	-	40	-	ns
		UG falling to LG rising at VCC=12V	-	20	-	ns
	LG to UG Dead time	LG falling to UG rising at VCC=5V	-	40	-	ns
		LG falling to UG rising at VCC=12V	-	20	-	ns
BOOTSTRAP SWITCH						
V_F	Ron	V_{VCC} – $V_{BOOT-GND}$, I_F = 10mA	-	0.2	0.4	V
I_R	Reverse Leakage	$V_{BOOT-GND}$ = 30V, V_{PHASE} = 25V, V_{VCC} = 5V	-	-	0.5	µA

Electrical Characteristics

These specifications apply for TA = -40°C to +85°C, unless otherwise stated. All typical specifications TA= +25°C, V_{CC} = 12V

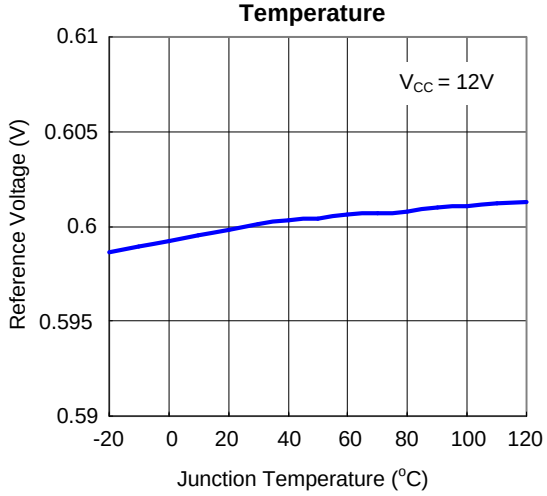
Symbal	Parameter	Test Condition	APW8724			
			Min.	Typ.	Max.	Unit
VCC POR THRESHOLD						
V_{VCC_THR}	Rising VCC POR Threshold Voltage		4.25	4.35	4.45	V
	VCC POR Hysteresis		-	300	-	mV
CONTROL INPUTS						
	EN Threshold	Shutdown	-	-	0.4	V
		Enable	0.83	-	-	
	EN Leakage	EN=0V	-	0.1	1.0	µA
POWER-OK INDICATOR						
V_{POK}	POK Threshold	POK in from Lower (POK Goes High)	87	90	93	%
		POK out from normal falling (POK Goes Low)	65	70	75	%
		POK out from normal rising (POK Goes Low)	120	125	130	%
I_{POK}	POK Leakage Current	V_{POK}=5V	-	0.1	1	µA
	POK Sink Current	V_{POK}=0.5V	5	15	-	mA
	POK Enable Delay Time	V_{OUT} from 0% to POK High	-	5.5	-	ms
CURRENT SENSE						
I_{OCSET}	I_{OCSET} OCP Threshold	I_{OCSET} Sourcing	22.5	25	27.5	µA
$T_{CIOCSET}$	I_{OCSET} Temperature Coefficient	On The Basis of 25°C	-	2780	-	ppm/°C
V_{ROCSET}	Maximum Current Limit Threshold	R_{OCSET} open	360	400	440	mV
	Zero Crossing Comparator Offset	$V_{GND-PHASE}$ Voltage	-3	0	3	mV
PROTECTION						
V_{UV}	UVP Threshold		65	70	75	%
	UVP Debounce Interval		-	30	-	µs
	UVP Enable Delay	V_{OUT} from 0% to UVP enable	-	5.5		ms
V_{OVR}	OVP Rising Threshold	V_{FB} rising, LG fully turn on	120	125	130	%
	OVP Falling Threshold	V_{FB} falling, Driver both off	-	105	-	%
	OVP Propagation Delay	V_{FB} Rising	-	2	-	µs
T_{OTR}	OTP Rising Threshold (Note 4)		-	150	-	°C
	OTP Hysteresis (Note 4)		-	25	-	°C

Pin Description

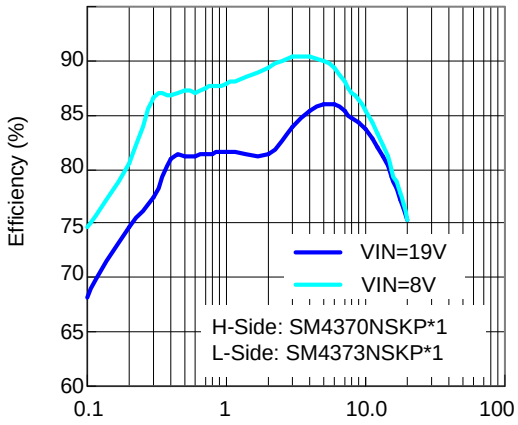
PIN		FUNCTION
No.	Name	
1	BOOT	Supply Input for The UGATE Driver and An Internal Level-shift Circuit. Connect to an external capacitor to create a boosted voltage suitable to drive a logic-level N-channel MOSFET.
2	UGATE	Output of The High-side MOSFET Driver. Connect this pin to Gate of the high-side MOSFET.
3	POK	Power Good Output. POK is an open drain output used to indicate the status of the output voltage. Connect the POK in to +5V through a pull-high resistor.
4	GND	Signal Ground for The IC
5	LGATE/OCSET	Output of The Low-side MOSFET Driver And Current-Limit Setting Input. Connect this pin to Gate of the low-side MOSFET. There is an internal source current 25μA through a resistor from LGATE/OCSET pin to GND before power on. This action is used to monitor the voltage drop across the Drain and Source of the low-side MOSFET for current limit.
6	VCC	Supply Voltage Input Pin for Control Circuitry. Connect +5V~+12V from the VCC pin to the GND. Decoupling at least 1μF of a MLCC capacitor from the VCC pin to the GND.
7	FBRTN	This pin is the negative node of the differential remote voltage sensing. The RTN pin should be connected to the remote GND sense point directly.
8	FB	Output Voltage Feedback Pin. This pin is connected to the resistive divider in remote side that set the desired output voltage. The POK, UVP, and OVP circuits detect this signal to report output voltage status.
9	EN	Enable/Shutdown Pin. When EN=1, enable the PWM controller, EN=0, shutdown the PWM controller.
10	PHASE	Junction Point of The High-side MOSFET Source, Output Filter Inductor and The Low-side MOSFET Drain. Connect this pin to the Source of the high-side MOSFET. PHASE serves as the lower supply rail for the UG high-side gate driver.
Exposed pad	GND	Signal Ground for The IC

Typical Operating Characteristics

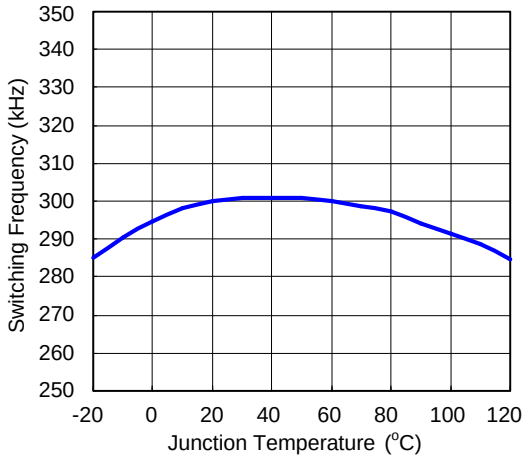
Reference Voltage vs. Junction Temperature



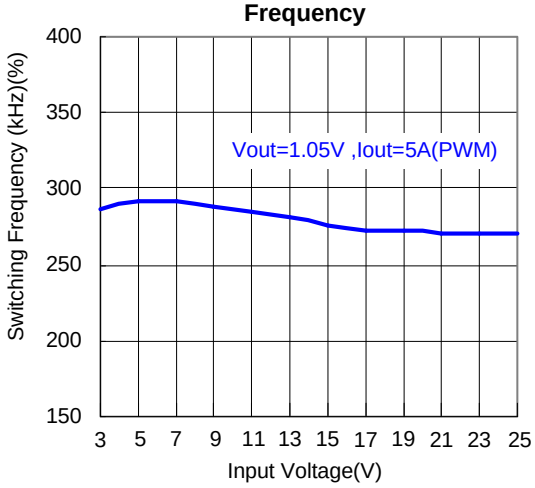
Efficiency vs. Load Current
F_{SW}=300KHz, V_{OUT}=1.05V



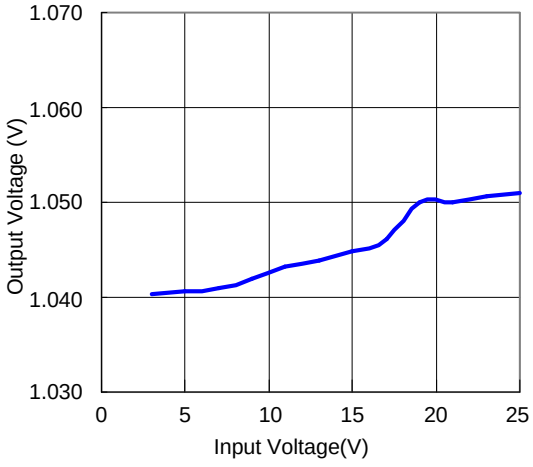
Switching Frequency vs. Junction Temperature



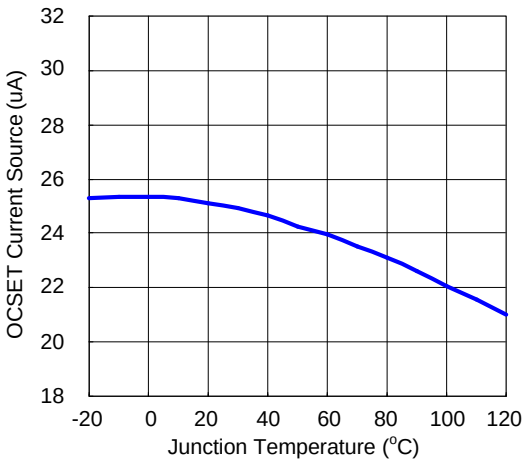
Input Voltage vs Switching Frequency



Input Voltage vs Output Voltage



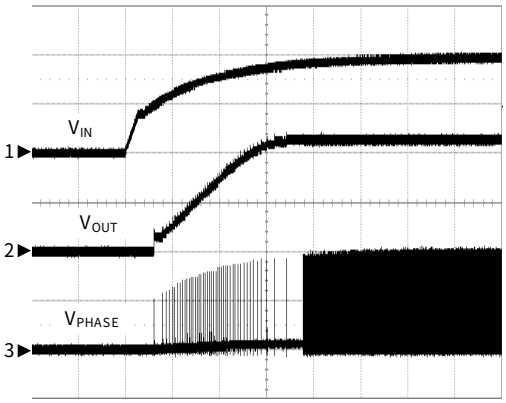
I_{OCSET} vs. Junction Temperature



Operating Waveforms

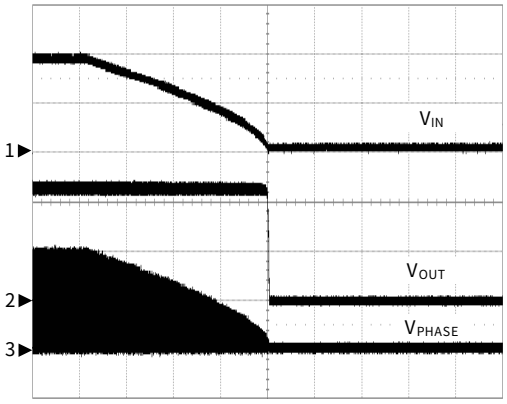
Refer to the typical application circuit. The test condition is V_{IN}=19V, T_A= 25°C unless otherwise specified.

Power On



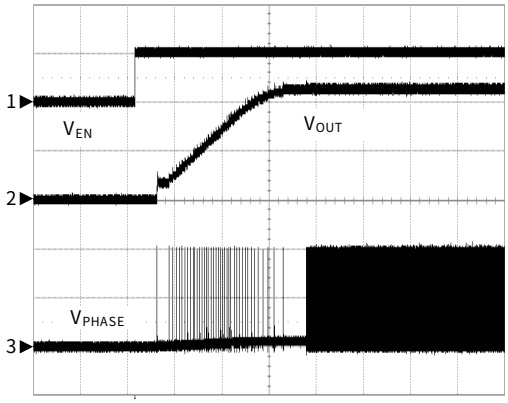
CH1: V_{IN} , 10V/Div
CH2: Vout , 500mV/Div
CH3: V_{PHASE} , 10V/Div
TIME: 2ms/Div

Power Off



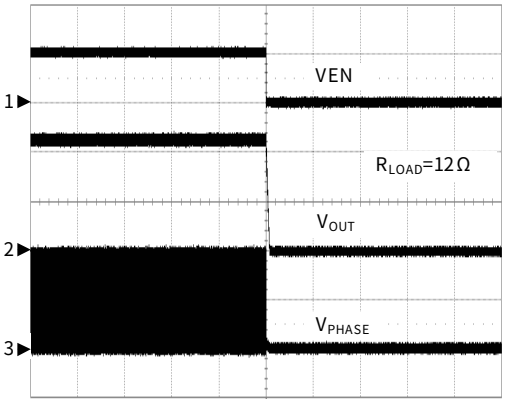
CH1: VIN , 10V/Div
CH2: Vout , 500mV/Div
CH3: V_{PHASE} , 10V/Div
TIME: 50ms/Div

Enable



CH1: V_{EN} , 5V/Div
CH2: Vout , 500mV/Div
CH3: V_{PHASE} , 10V/Div
TIME: 1ms/Div

Shutdown

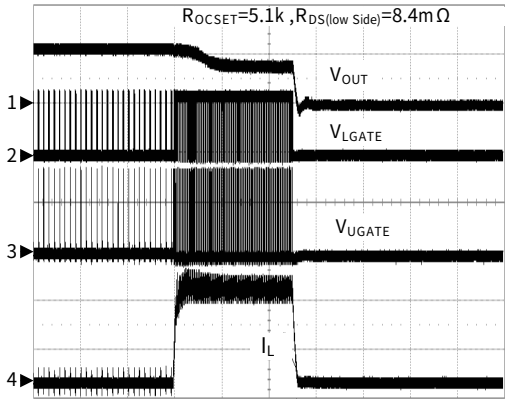


CH1: V_{EN} , 5V/Div
CH2: Vout , 500mV/Div
CH3: V_{PHASE} , 10V/Div
TIME: 5ms/Div

Operating Waveforms

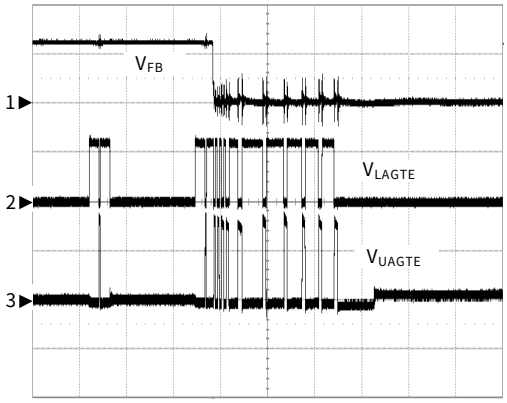
Refer to the typical application circuit. The test condition is V_{IN}=19V, T_A= 25°C unless otherwise specified.

Over-Current Protection



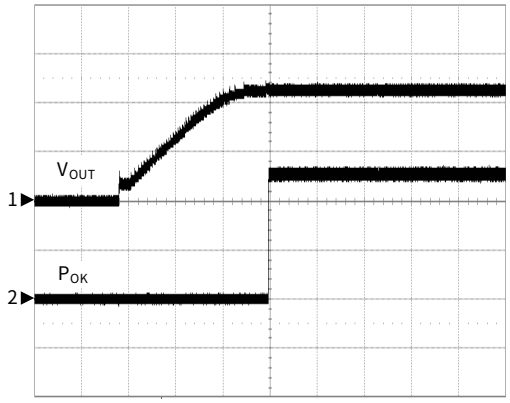
CH1: V_{OUT} , 10V/Div
CH2: V_{LGATE} , 10V/Div
CH3: V_{UGATE} , 20V/Div
CH4: I_L , 10A/Div
TIME: 20ms/Div

Under-Voltage Protection



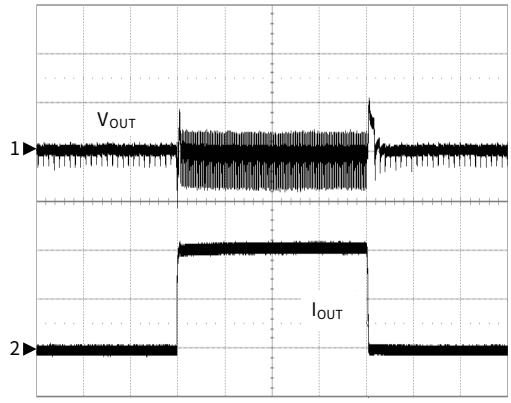
CH1: V_{FB} , 500mV/Div
CH2: V_{LGATE} , 10V/Div
CH3: V_{UGATE} , 20V/Div
TIME: 10us/Div

Power OK



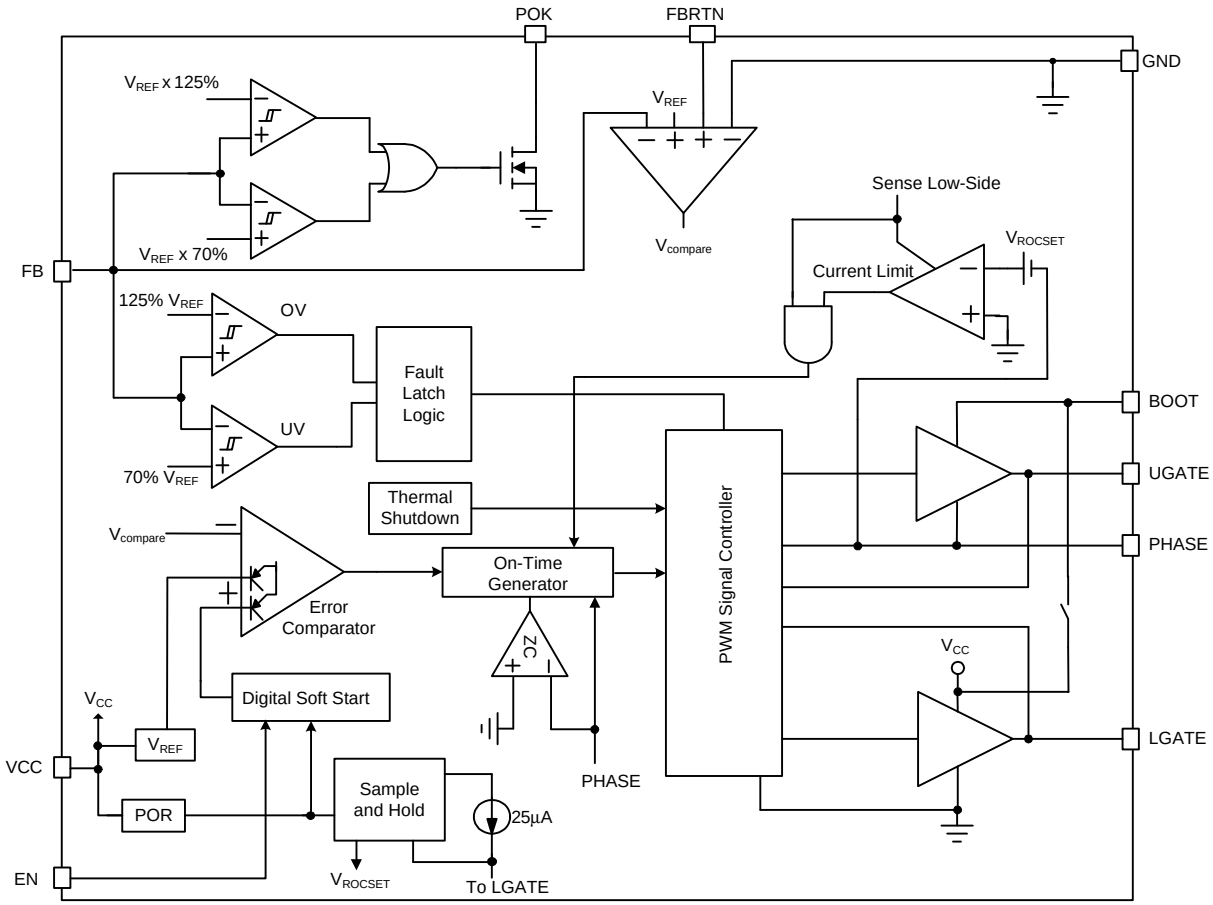
CH1: V_{OUT} , 500mV/Div
CH2: V_{POK} , 5V/Div
TIME: 1ms/Div

Load Transient

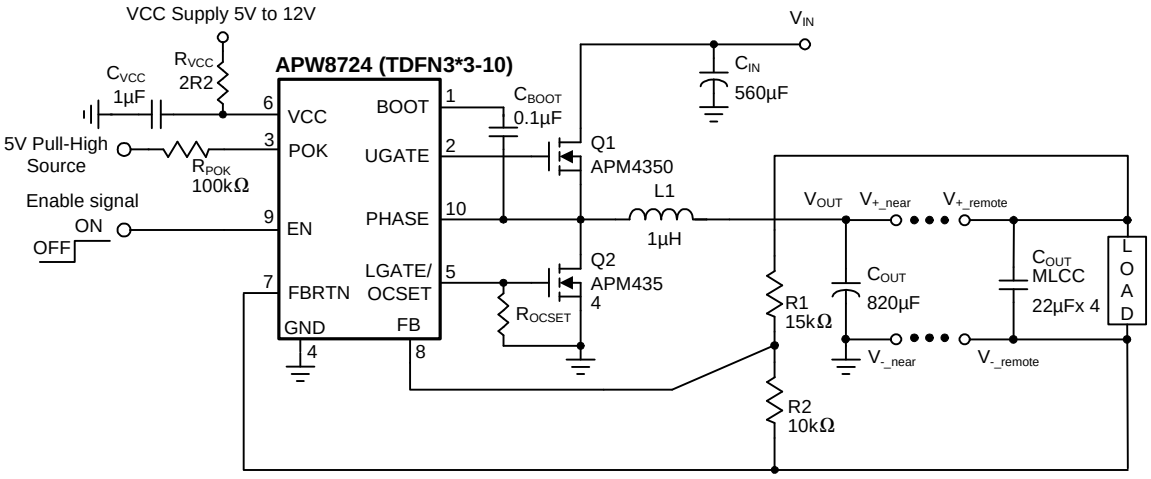


CH1: V_{OUT} , 50mV/Div
CH2: I_{OUT} , 5A/Div
TIME: 200us/Div

Block Diagram



Typical Application Circuit



Function Description

Constant-On-Time PWM Controller with Input Feed-Forward

The constant-on-time control architecture is a pseudo-fixed frequency with input voltage feed-forward. This architecture relies on the output filter capacitor's effective series resistance (ESR) to act as a current-sense resistor so the output ripple voltage provides the PWM ramp signal. In PFM operation, the high-side switch on-time is controlled by the on-time generator is determined solely by a one-shot whose pulse width is inversely proportional to the input voltage and directly proportional to the output voltage. In PWM operation, the high-side switch on-time is determined by a switching frequency control circuit in the on-time generator block.

The switching frequency control circuit senses the switching frequency of the high-side switch and keeps regulating it at a constant frequency in PWM mode. The design improves the frequency variation and is more outstanding than a conventional constant-on-time controller, which has large switching frequency variation over input voltage, output current, and temperature. Both in PFM and PWM, the on-time generator, which senses input voltage on PHASE pin, provides very fast on-time response to input line transients.

Another one-shot sets a minimum off-time (typical: 400ns). The on-time one-shot is triggered if the error comparator is high, the low-side switch current is below the current-limit threshold, and the minimum off-time one-shot has timed out.

Pulse-Frequency Modulation (PFM)

In PFM mode, an automatic switchover to pulse-frequency modulation (PFM) takes place at light loads. This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current zero crossing. This mechanism causes the threshold between PFM and PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation (also known as the critical conduction point). The on-time of PFM is given by:

$$T_{ON-PFM} = \frac{1}{F_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

Where F_{SW} is the nominal switching frequency of the converter in PWM mode.

The load current at handoff from PFM to PWM mode is given by:

$$I_{LOAD(PFMtoPWM)} = \frac{1}{2} \times \frac{V_{IN} - V_{OUT}}{L} \times T_{ON-PFM}$$
$$= \frac{V_{IN} - V_{OUT}}{L} \times \frac{1}{F_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

In this case, APW8724 operates in ultrasonic mode with PFM when the load is zero. The ultrasonic mode is illustrated as below description.

Ultrasonic Mode

The ultrasonic mode activates an unique PFM mode with a minimum switching frequency of 25kHz. The minimum frequency 25kHz of ultrasonic mode eliminates audio-frequency interference in light load condition. It will transit to unique PFM mode when output loading makes the frequency bigger than ultrasonic frequency.

In ultrasonic mode, the controller automatically transits to fixed-frequency PWM operation when the load reaches the same critical conduction point ($I_{LOAD(PFM\ to\ PWM)}$).

When the controller detects that no switching has occurred within about 40μs (Typical), an ultrasonic pulse will be occurred. The ultrasonic controller turns on the low-side MOSFET firstly to reduce the output voltage. After feedback voltage drops below the internal reference voltage, the controller turns off the low-side MOSFET and triggers a constant-on-time. When the constant-on-time has expired, the controller turns on the low-side MOSFET again until the inductor current is below the zero-crossing threshold. The behavior is the same as PFM mode.

Power-On-Reset (POR)

A Power-On-Reset (POR) function is designed to prevent wrong logic controls when the VCC voltage is low. The POR function continually monitors the bias supply voltage on the VCC pin if at least one of the enable pins is set high. When the rising VCC voltage reaches the rising POR voltage threshold (4.35V, typical), the POR signal goes high and the chip initiates soft-start operations. When this voltage drops lower than 4.25V (typical), the POR disables the chip.

Function Description (Cont.)

Current-Limit

The current-limit circuit employs a "valley" current-sensing algorithm (See Figure 1). The APW8724 uses the low-side MOSFET $R_{DS(ON)}$ of the synchronous rectifier as a current-sensing element. If the magnitude of the current-sense signal at PHASE pin is above the current-limit threshold, the PWM is not allowed to initiate a new cycle. The actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are the functions of the sense resistance, inductor value, and input voltage.

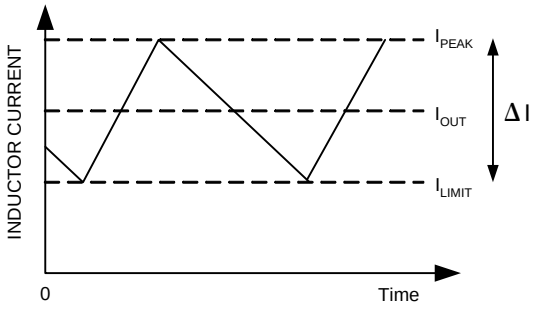


Figure 1. Current-Limit Algorithm

A resistor (R_{OCSET}), connected from the LGATE/OCSET to GND, programs the current-limit threshold. Before the IC initiates a soft-start process, an internal current source, I_{OCSET} (25μA typical), flowing through the R_{OCSET} develops a voltage (V_{OCSET}) across the R_{OCSET}. The device holds V_{OCSET} and stops the current source, I_{OCSET}, during normal operation. The relationship between the sampled voltage V_{OCSET} and the current-limit threshold I_{LIMIT} is given by:

$$I_{LIMIT} = \frac{2 \times I_{OCSET} \times R_{OCSET}}{R_{DS(ON)}(low-side)}$$

I_{LIMIT} can be expressed as I_{OUT} minus half of peak-to-peak inductor current.

The APW8724 has an internal current-limit voltage (V_{OCSET_MAX}), and the value is 0.4V typically. When the R_{OCSET} x I_{OCSET} exceeds 0.4V or the R_{OCSET} is floating or not connected, the over current threshold will be the internal default value 0.4V.

The PCB layout guidelines should ensure that noise and DC errors do not corrupt the current-sense signals at PHASE. Place the hottest power MOSEFTs as close to the IC as possible for best thermal coupling. When combined with the under-voltage protection circuit, this current-limit method is effective in almost every circumstance.

Under-Voltage Protection

In the operational process, if a short-circuit occurs, the output voltage will drop quickly. When load current is bigger than current-limit threshold value, the output voltage will fall out of the required regulation range. The under-voltage protection circuit continually monitors the FB voltage after soft-start is completed. If a load step is strong enough to pull the output voltage lower than the under-voltage threshold, the under-voltage threshold is 70% of the nominal output voltage, the internal UVP delay counter starts to count. After 30μs debounce time, the device turns off both high-side and low-side MOSEFET with latched and starts a soft-stop process to shut down the output gradually. Toggling enable pin to low or recycling VCC, will clear the latch and bring the chip back to operation.

Over-Voltage Protection (OVP) of the PWM Converter

The over-voltage protection monitors the FB voltage to prevent the output from over-voltage condition. When the output voltage rises above 125% of the nominal output voltage, the APW8724 turns off the high-side MOSFET and turns on the low-side MOSFET until the output voltage falls below the falling below 105%, the OVP comparator is disengaged and both high-side and low-side drivers turn off.

This OVP scheme only clamps the voltage overshoot and does not invert the output voltage when otherwise activated with a continuously high output from low-side MOSFET driver. It's a common problem for OVP schemes with a latch. Once an over-voltage fault condition is set, it can be reset by releasing COMP or toggling VCC power-on-reset signal.

Function Description (Cont.)

EN Pin Control

When V_{EN} is above the EN high threshold (0.83V, minimum). th converter is enabled in automatic PFM/ PWM operation mode. When V_{EN} is below the EN low threshold (0.4V, maximum), the chip is in the shutdown and only low leakage current is taken from VCC.

Adaptive Shoot-Through Protection of the PWM Converter

The gate drivers incorporate an adaptive shoot-through protection to prevent high-side and low-side MOSFETs from conducting simultaneously and shorting the input supply. This is accomplished by ensuring the falling gate has turned off one MOSFET before the other is allowed to rise.

During turn-off the low-side MOSFET, the LGATE voltage is monitored until it is below 1.5V threshold, at which time the UGATE is released to rise after a constant delay. During turn-off of the high-side MOSFET, the UGATE-to-PHASE voltage is also monitored until it is below 1.5V threshold, at which time the LGATE is released to rise after a constant delay.

Remote Sense

APW8724 has a FBRTN pin for applications that require remote sense. In some applications where high current, low voltage and accurate output voltage regulation are needed, FBRTN can sense the negative terminal of remote load capacitor directly, and improve output voltage drop which is due to the board interconnection loss.

Power OK Indicator

The APW8724 features an open-drain POK output pin to indicate one of the IC's working statuses including soft-start, under-voltage fault, over-current fault.

In normal operation, when the output voltage rises 90% of its target value, the POK goes high. When the output voltage outruns 50% or 125% of the target voltage, POK signal will be pulled low immediately.

Application Information

Output Voltage Selection

The output voltage can be programmed with a resistive divider. Use 1% or better resistors for the resistive divider is recommended. The FB pin is the inverter input of the error amplifier, and the reference voltage is 0.6V. The output voltage is determined by:

$$V_{OUT} = 0.6 \times \left(1 + \frac{R_1}{R_2}\right)$$

Where R1 is the resistor connected from V_{OUT} to FB and R2 is the resistor connected from FB to the GND.

Output Inductor Selection

The duty cycle (D) of a buck converter is the function of the input voltage and output voltage. Once an output voltage is fixed, it can be written as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

The inductor value (L) determines the inductor ripple current, I_{RIPPLE}, and affects the load transient reponse. Higher inductor value reduces the inductor's ripple current and induces lower output ripple voltage. The ripple current and ripple voltage can be approximated by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{F_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

Where F_{SW} is the switching frequency of the regulator. Although the inductor value and frequency are increased and the ripple current and voltage are reduced, a tradeoff exists between the inductor's ripple current and the regulator load transient response time.

A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current. Increasing the switching frequency (F_{SW}) also reduces the ripple current and voltage, but it will increase the switching loss of the MOSFETs and the power dissipation of the converter. The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current. Once the inductance value has been chosen, selecting an inductor which is capable of carrying the required peak current without going into saturation. In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly when it saturates. This results in a larger output ripple voltage. Besides, the inductor needs to have low DCR to reduce the loss of efficiency.

Output Capacitor Selection

Output voltage ripple and the transient voltage deviation are factors which have to be taken into consideration when selecting an output capacitor. Higher capacitor value and lower ESR reduce the output ripple and the load transient drop. Therefore, selecting high performance low ESR capacitors is recommended for switching regulator applications. In addition to high frequency noise related to MOSFET turn-on and turn-off, the output voltage ripple includes the capacitance voltage drop ΔV_{COUT} and ESR voltage drop ΔV_{ESR} caused by the AC peak-to-peak inductor's current. These two voltages can be represented by:

$$\Delta V_{COUT} = \frac{I_{RIPPLE}}{8 C_{OUT} F_{SW}}$$

$$\Delta V_{ESR} = I_{RIPPLE} \times R_{ESR}$$

These two components constitute a large portion of the total output voltage ripple. In some applications, multiple capacitors have to be paralleled to achieve the desired ESR value. If the output of the converter has to support another load with high pulsating current, more capacitors are needed in order to reduce the equivalent ESR and suppress the voltage ripple to a tolerable level. A small decoupling capacitor (1μF) in parallel for bypassing the noise is also recommended, and the voltage rating of the output capacitors are also must be considered. To support a load transient that is faster than the switching frequency, more capacitors are needed for reducing the voltage excursion during load step change. Another aspect of the capacitor selection is that the total AC current going through the capacitors has to be less than the rated RMS current specified on the capacitors in order to prevent the capacitor from over-heating.

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, selecting the capacitor voltage rating to be at least 1.3 times

Application Information (Cont.)

Input Capacitor Selection (Cont.)

higher than the maximum input voltage. The maximum RMS current rating requirement is approximately $I_{OUT}/2$, where I_{OUT} is the load current. During power-up, the input capacitors have to handle great amount of surge current. For low-duty notebook appliactions, ceramic capacitor is recommended. The capacitors must be connected between the drain of high-side MOSFET and the source of low-side MOSFET with very low-impeadance PCB layout.

MOSFET Selection

The application for a notebook battery with a maximum voltage of 24V, at least a minimum 30V MOSFETs should be used. The design has to trade off the gate charge with the $R_{DS(ON)}$ of the MOSFET:

For the low-side MOSFET, before it is turned on, the body diode has been conducting. The low-side MOSFET driver will not charge the miller capacitor of this MOSFET.

In the turning off process of the low-side MOSFET, the load current will shift to the body diode first. The high dv/dt of the phase node voltage will charge the miller capacitor through the low-side MOSFET driver sinking current path. This results in much less switching loss of the low-side MOSFETs. The duty cycle is often very small in high battery voltage applications, and the low-side MOSFET will conduct most of the switching cycle; therefore, when using smaller $R_{DS(ON)}$ of the low-side MOSFET, the converter can reduce power loss. The gate charge for this MOSFET is usually the secondary consideration. The high-side MOSFET does not have this zero voltage switching condition; in addition, it conducts for less time compared to the low-side MOSFET, so the switching loss tends to be dominant. Priority should be given to the MOSFETs with less gate charge, so that both the gate driver loss and switching loss will be minimized.

The selection of the N-channel power MOSFETs are determined by the $R_{DS(ON)}$, reversing transfer capacitance (C_{RSS}) and maximum output current requirement. The losses in the MOSFETs have two components: conduction loss and transition loss. For the high-side and low-side MOSFETs, the losses are approximately given by the following equations:

$$P_{high\text{-}side} = I_{OUT}^{2}(1+TC)(R_{DS(ON)})D + (0.5)(I_{OUT})(V_{IN})(t_{SW})F_{SW}$$

$$P_{low\text{-}side} = I_{OUT}^{2}(1+TC)(R_{DS(ON)})(1-D)$$

Where

I_{OUT} is the load current

TC is the temperature dependency of $R_{DS(ON)}$

F_{SW} is the switching frequency

t_{SW} is the switching interval

D is the duty cycle

Note that both MOSFETs have conduction losses while the high-side MOSFET includes an additional transition loss. The switching interval, t_{SW}, is the function of the reverse transfer capacitance C_{RSS}. The (1+TC) term is a factor in the temperature dependency of the $R_{DS(ON)}$ and can be extracted from the "$R_{DS(ON)}$ vs. Temperature" curve of the power MOSFET.

Layout Consideration

In any high switching frequency converter, a correct layout is important to ensure proper operation of the regulator. With power devices switching at higher frequency, the resulting current transient will cause voltage spike across the interconnecting impedance and parasitic circuit elements. As an example, consider the turn-off transition of the PWM MOSFET. Before turn-off condition, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is freewheeling by the low side MOSFET and parasitic diode. Any parasitic inductance of the circuit generates a large voltage spike during the switching interval. In general, using short and wide printed circuit traces should minimize interconnecting impedances and the magnitude of voltage spike. Besides, signal and power grounds are to be kept separating and finally combined using ground plane construction or single point grounding. The best tie-point between the signal ground and the power ground is at the negative side of the output capacitor on each channel, where there is less noise. Noisy traces beneath the IC are not recommended. Below is a checklist for your layout:

- Keep the switching nodes (UGATE, LGATE, BOOT, and PHASE) away from sensitive small signal nodes since these nodes are fast moving signals.
  Therefore, keep traces to these nodes as short as

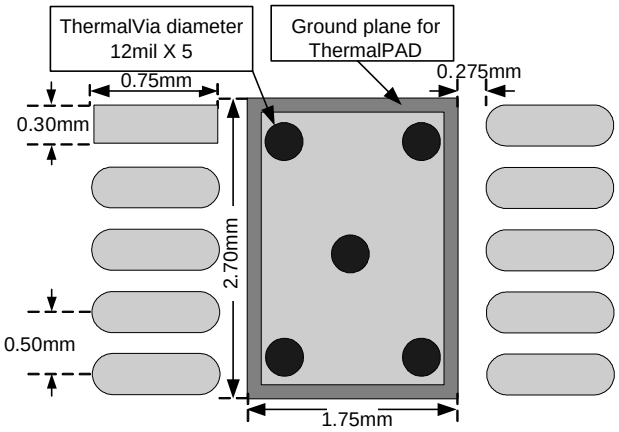
Application Information (Cont.)

Layout Consideration (Cont.)

possible and there should be no other weak signal traces in parallel with theses traces on any layer.

- The signals going through theses traces have both high dv/dt and high di/dt with high peak charging and discharging current. The traces from the gate drivers to the MOSFETs (UGATE and LGATE) should be short and wide.
- Place the source of the high-side MOSFET and the drain of the low-side MOSFET as close as possible. Minimizing the impedance with wide layout plane between the two pads reduces the voltage bounce of the node. In addition, the large layout plane between the drain of the MOSFETs (V_{IN} and PHASE nodes) can get better heat sinking.
- The PGND is the current sensing circuit reference ground and also the power ground of the LGATE low-side MOSFET. On the other hand, the PGND trace should be a separate trace and independently go to the source of the low-side MOSFET. Besides, the current sense resistor should be close to OCSET pin to avoid parasitic capacitor effect and noise coupling.
- Decoupling capacitors, the resistor-divider, and boot capacitor should be close to their pins. (For example, place the decoupling ceramic capacitor close to the drain of the high-side MOSFET as close as possible.)
- The input bulk capacitors should be close to the drain of the high-side MOSFET, and the output bulk capacitors should be close to the loads. The input capacitor's ground should be close to the grounds of the output capacitors and low-side MOSFET.
- Locate the resistor-divider close to the FB pin to minimize the high impedance trace. In addition, FB pin traces can't be close to the switching signal traces (UGATE, LGATE, BOOT, and PHASE).

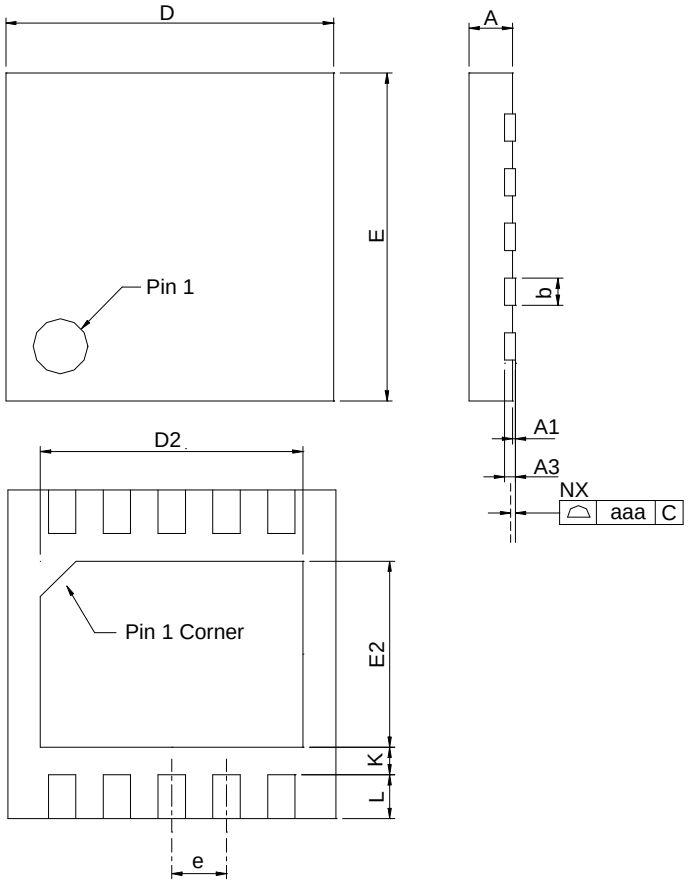
Recommended Minimum Footprint



TDFN3X3 -10L and Pattern R ecommendation

Package Information

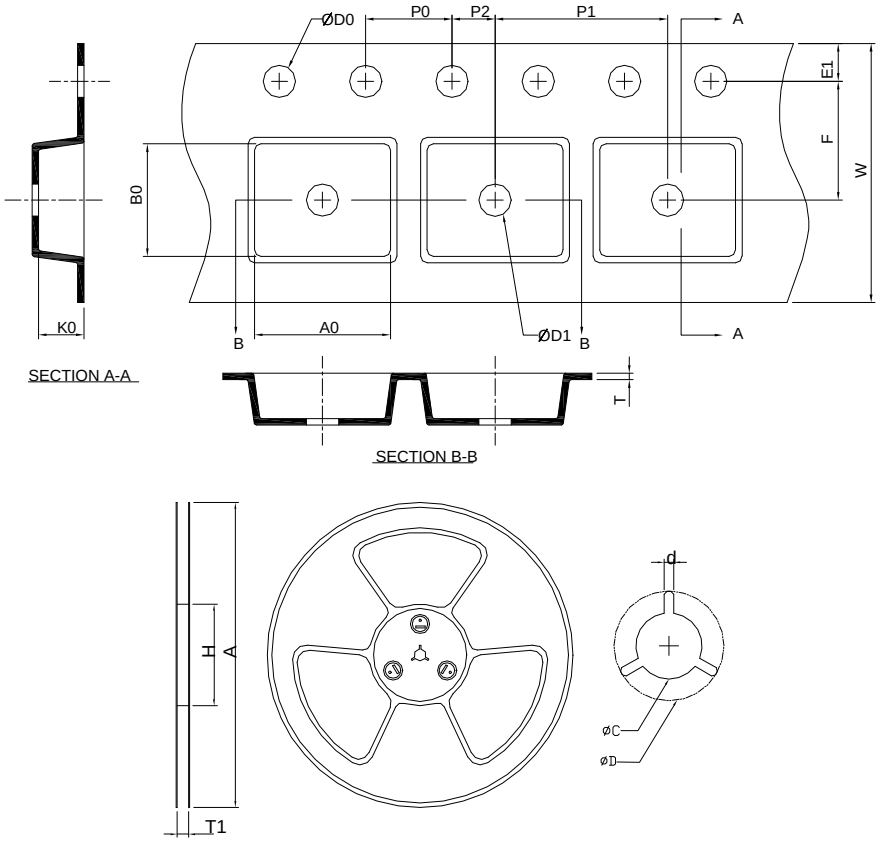
TDFN3x3-10



SYMBOL	TDFN3x3-10			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	2.90	3.10	0.114	0.122
D2	2.20	2.70	0.087	0.106
E	2.90	3.10	0.114	0.122
E2	1.40	1.75	0.055	0.069
e	0.50 BSC		0.016 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	
aaa	0.08		0.003	

Note : 1. Followed from JEDEC MO-229 VEED-5.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TDFN3x3-10	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.30±0.20

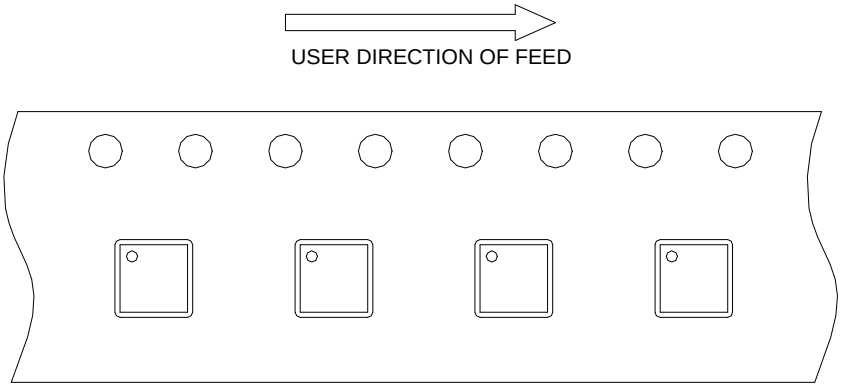
(mm)

Devices Per Unit

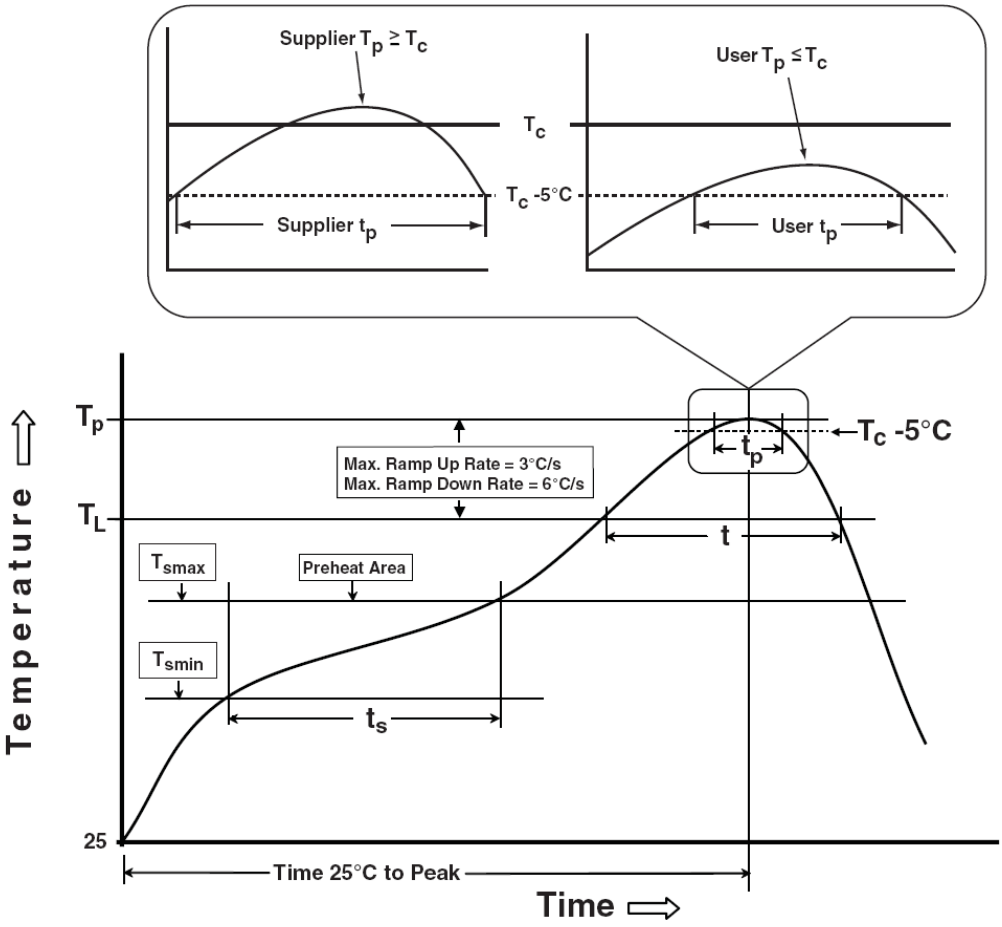
Package Type	Unit	Quantity
TDFN3x3-10	Tape & Reel	3000

Taping Direction Information

TDFN3x3-10



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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