



SPP2305D

P-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP2305D is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

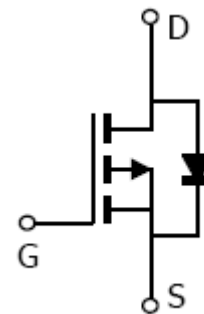
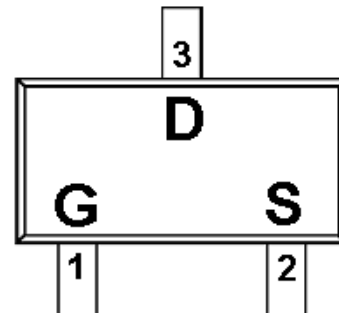
FEATURES

- ◆ -15V/-3.5A, $R_{DS(ON)} = 70\text{m}\Omega @ V_{GS} = -4.5\text{V}$
- ◆ -15V/-3.0A, $R_{DS(ON)} = 85\text{m}\Omega @ V_{GS} = -2.5\text{V}$
- ◆ -15V/-2.0A, $R_{DS(ON)} = 105\text{m}\Omega @ V_{GS} = -1.8\text{V}$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOT-23 package design

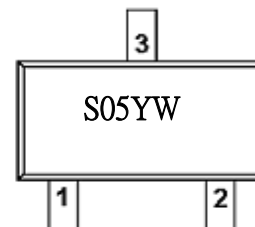
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION(SOT-23)



PART MARKING



Y : Year Code
W : Week Code



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PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP2305DS23RG	SOT-23	S05YW

※ Week Code : A ~ Z (1 ~ 26) ; a ~ z (27 ~ 52)

※ SPP2305DS23RG : Tape Reel ; Pb – Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V _{DSS}	-15	V	
Gate –Source Voltage	V _{GSS}	±12	V	
Continuous Drain Current(T _J =150°C)	I _D	TA=25°C	-3.5	A
		TA=70°C	-2.8	
Pulsed Drain Current	I _{DM}	-10	A	
Continuous Source Current(Diode Conduction)	I _S	-1.6	A	
Power Dissipation	P _D	TA=25°C	1.25	W
		TA=70°C	0.8	
Operating Junction Temperature	T _J	150	°C	
Storage Temperature Range	T _{STG}	-55/150	°C	
Thermal Resistance-Junction to Ambient	R _{θJA}	120	°C/W	



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ELECTRICAL CHARACTERISTICS

($T_A=25^{\circ}\text{C}$ Unless otherwise noted)

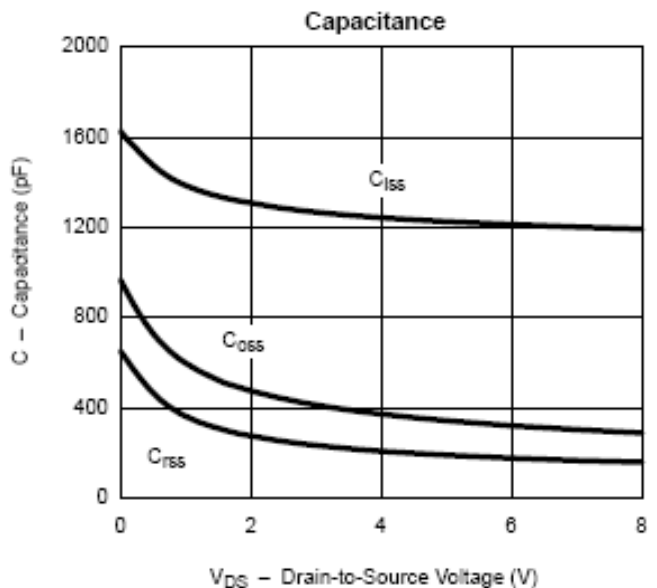
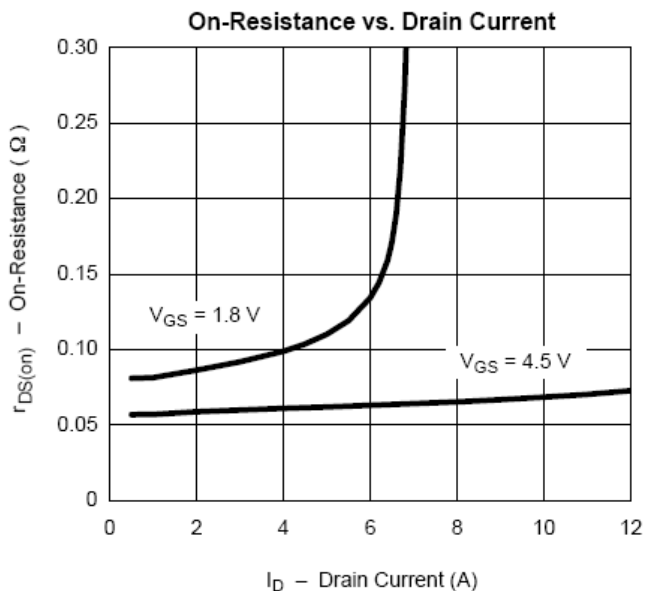
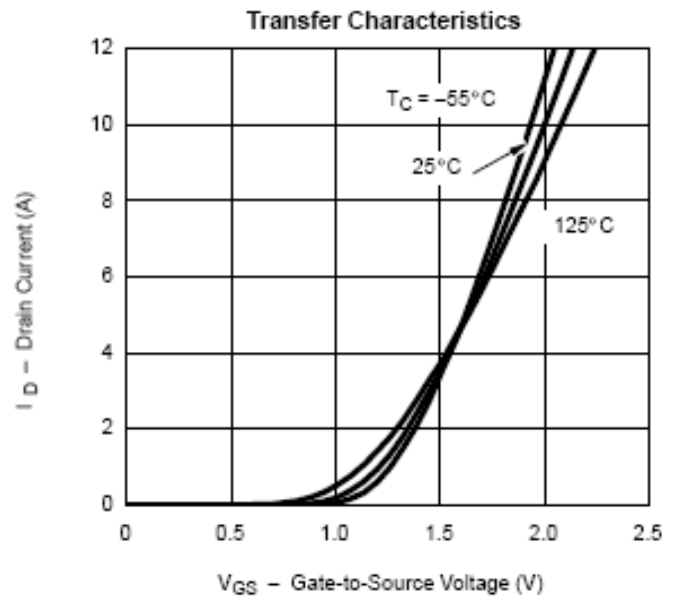
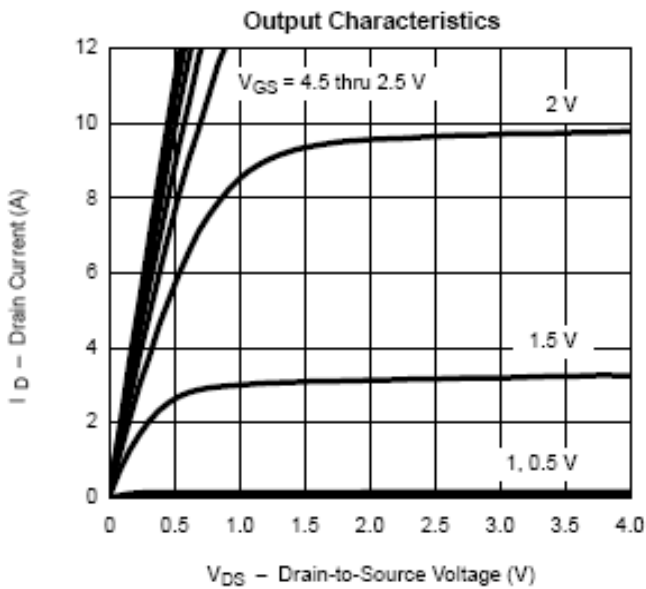
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-15			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.35		-0.85	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 10V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-12V, V_{GS}=0V$			-1	uA
		$V_{DS}=-12V, V_{GS}=0V$ $T_J=55^{\circ}\text{C}$			-10	
On-State Drain Current	$I_{D(on)}$	$V_{DS}\leq -5V, V_{GS}=-4.5V$	-4			A
		$V_{DS}\leq -5V, V_{GS}=-2.5V$	-2			
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=-4.5V, I_D=-3.5A$		0.060	0.70	Ω
		$V_{GS}=-2.5V, I_D=-3.0A$		0.072	0.85	
		$V_{GS}=-1.8V, I_D=-2.0A$		0.090	0.105	
Forward Transconductance	g_{fs}	$V_{DS}=-5V, I_D=-3.5A$		8.5		S
Diode Forward Voltage	V_{SD}	$I_S=-1.5A, V_{GS}=0V$		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=-6V, V_{GS}=-4.5V$ $I_D=-2.8A$		4.8	8	nC
Gate-Source Charge	Q_{gs}			1.0		
Gate-Drain Charge	Q_{gd}			1.0		
Input Capacitance	C_{iss}	$V_{DS}=-6V, V_{GS}=0V$ $f=1\text{MHz}$		485		pF
Output Capacitance	C_{oss}			85		
Reverse Transfer Capacitance	C_{rss}			40		
Turn-On Time	$t_{d(on)}$	$V_{DD}=-6V, R_L=6\Omega$ $I_D=-1.0A, V_{GEN}=-4.5V$ $R_G=6\Omega$		10	16	ns
	t_r			13	23	
Turn-Off Time	$t_{d(off)}$			18	25	
	t_f			15	20	



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TYPICAL CHARACTERISTICS

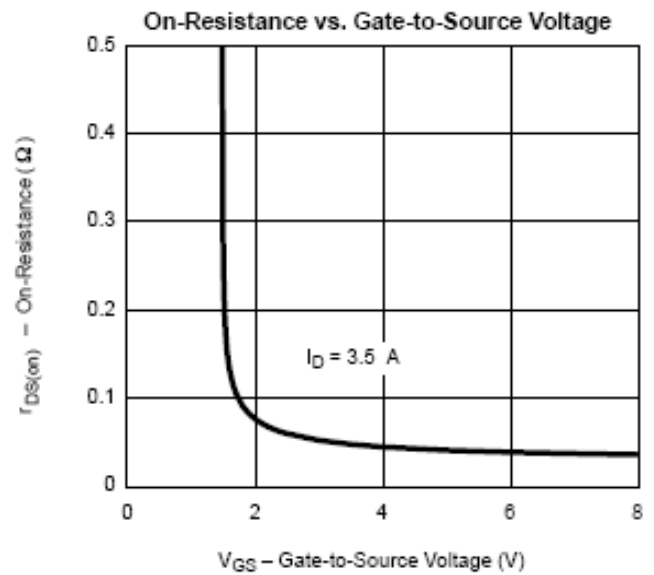
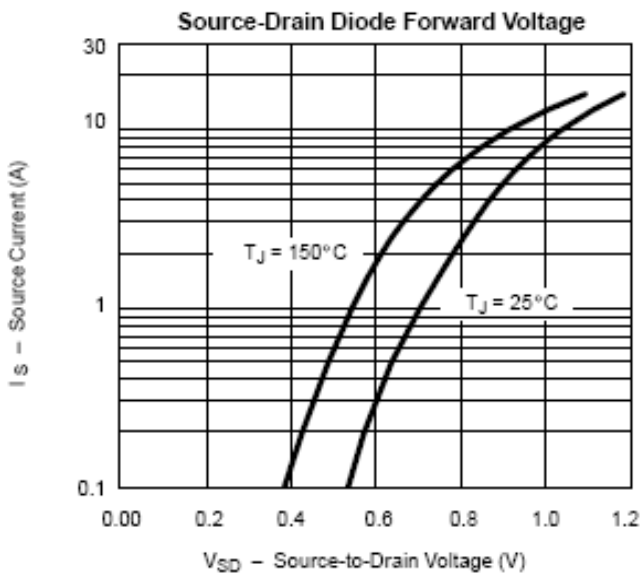
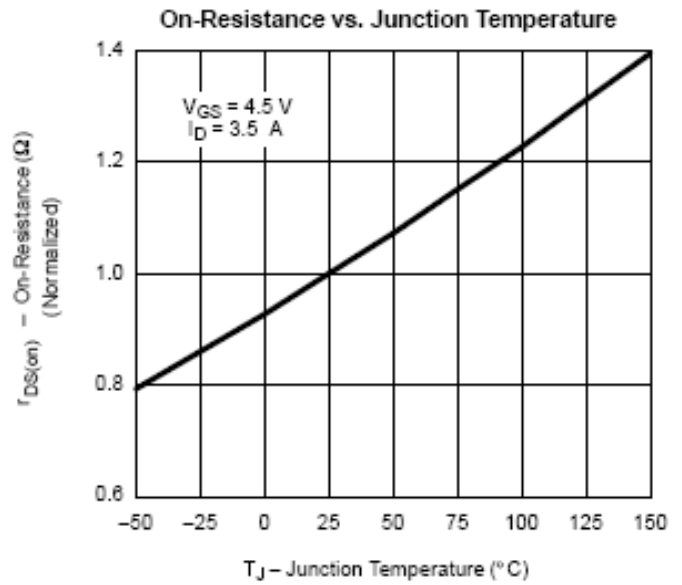
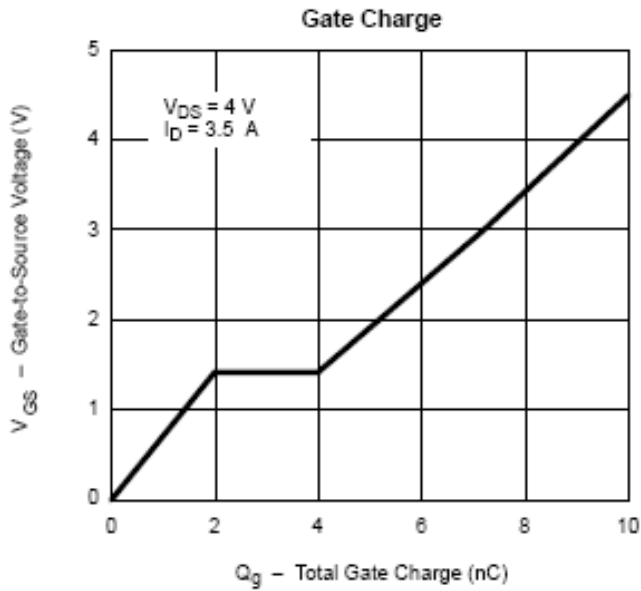




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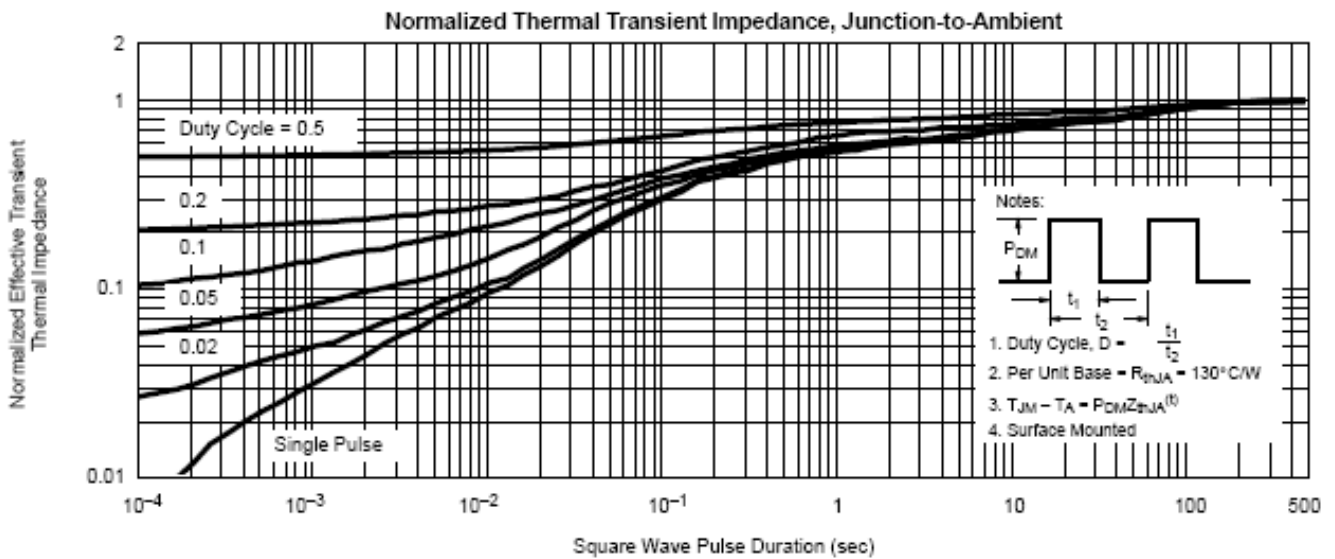
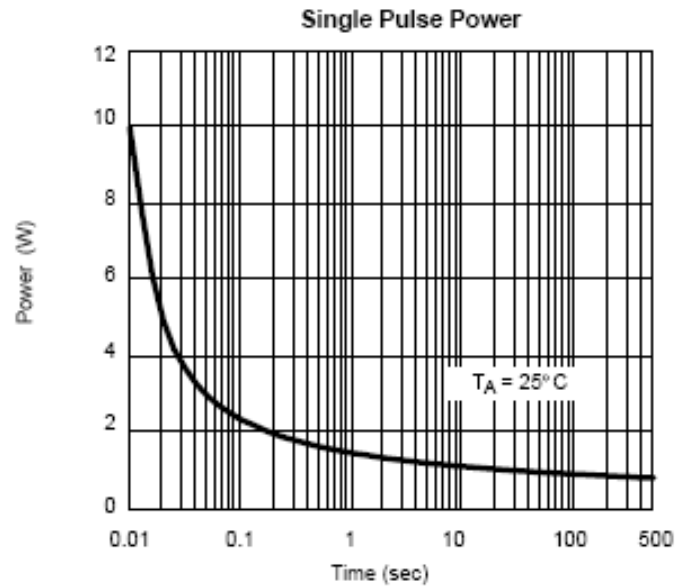
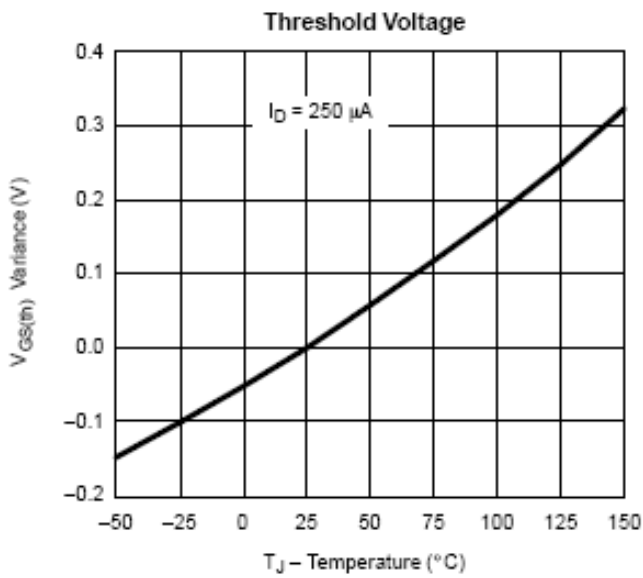




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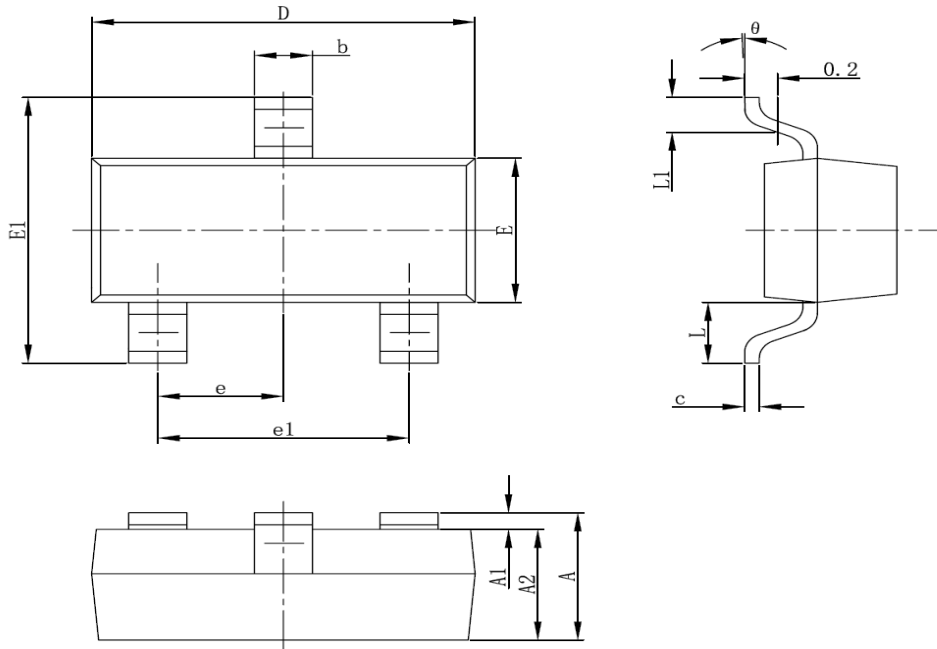




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SOT-23 PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.550REF		0.022REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°



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