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AKD4705A-A

AK4705A Evaluation Board Rev.0

GENERAL DESCRIPTION

AKD4705A-A is an evaluation board for quickly evaluating the AK4705A, 2ch DAC with AV SCART switch. Evaluation requires audio/video analog analyzers/generators, a digital audio signal source, and a power supply. AKM's ADC evaluation board can be also used for the audio source. Also included is a AK4112B digital audio interface receiver which receives S/PDIF compatible audio data. The digital audio data is available via optical connector or BNC.

AKD4705A-A --- AK4705A Evaluation Board

(Cable for connecting with printer port of IBM-AT compatible PC and a control software are enclosed with board. This control software dose not support Windows NT.)

FUNCTION

- BNC connectors for analog audio input/output
- BNC connectors for analog video input/output
- On-board clock generator
- BNC connector for an external clock input
- Compatible with 2 types of digital interface
 1. Serial interface: Direct interface with evaluation boards for AKM's A/D converter evaluation boards.
 2. S/PDIF: On-board AK4112BVF as DIR that accepts optical input or BNC input
- 10pin header for serial control interface

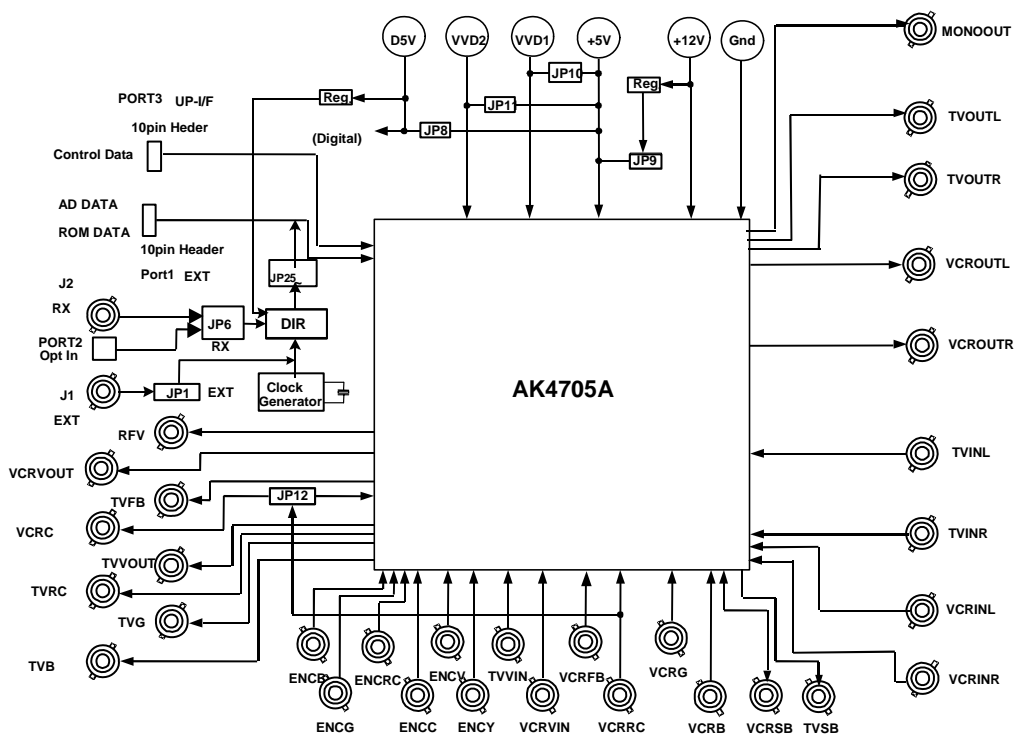


Figure 1. AKD4705A-A Block Diagram

Note 1. Circuit diagram and PCB layout are attached at the end of this manual.

■ Operation sequence

- 1) Set up the power supply lines.

| Name | Color | Voltage | Comments | Attention |
|-------|---------|----------------------|----------------|--|
| +12V | Orange | +11.4 [V] ~ +12.6[V] | Regulator, VP | This jack should be always connected. |
| +5V | Red | +4.75[V] ~ +5.25[V] | VD | This jack is open when JP9 (REG) is short. |
| D5V | Red | +4.75[V] ~ +5.25[V] | Logic | This jack is open when JP8 (D-A) is short. |
| VVD1 | Red | +4.75[V] ~ VVD2 | VVD1 | This jack is open when JP10 (VDD1) is short. |
| VVD2 | Blue | VDD1 ~ +5.25[V] | VVD2 | This jack is open when JP11 (VDD2) is short. |
| AGND | Black | 0[V] | Analog Ground | This jack should be always connected. |
| DGND | Black | 0[V] | Digital ground | This jack should be always connected. |
| VVSS2 | (Black) | 0[V] | Analog Ground | This jack should be always connected. |

Table 1. Set up of power supply lines

Note 2. Each supply line should be distributed from the power supply unit.

- 2) Set-up the evaluation modes, jumper pins and DIP-switches. (Refer next sections.)
- 3) Connect the PORT3 (μ P-I/F) with PC by the enclosed 10-wire flat cable.
- 4) Set up the PC and execute the enclosed control software.
(Please refer to the Control Software Manual.)
- 5) Turn the power on.
- 6) Reset the AK4705A once by bringing the SW1 (PDN) "L", and return it to "H".

■ Evaluation mode

1) S/PDIF mode (Optical Link or BNC: default)

When the CM0 (DIP-switch S1_1 on board) is “L”, the AK4112B (DIR) generates MCLK, BICK, LRCK and SDATA from the received bit stream through PORT2 (TORX176: optical link) or J2 (BNC). This mode is used for the evaluation using CD test disk. The PORT1 (EXT) should be open.

1)-1. DIP-switch set-up

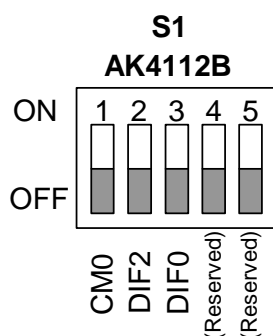
| No. | CM0 | DIF2 | DIF0 | Audio Data Format of AK4112B | Notes |
|-----|-----|------|------|------------------------------|-------------|
| 1 | “L” | “L” | “L” | 16bit LSB justified | 1 |
| 2 | “L” | “L” | “H” | 18bit LSB justified | 2 |
| 3 | “L” | “H” | “L” | 24bit MSB justified | 3 |
| 4 | “L” | “H” | “H” | 24bit I ² S | 4 (Default) |

Table 2. DIP-switch set-up (DIF1=“L”)

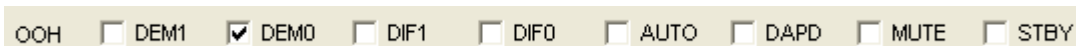
Much the data format of the AK4705A via I²C-bus control as following notes.

Note 1. 16bit LSB justified

Set up the DIP-switch as follows.

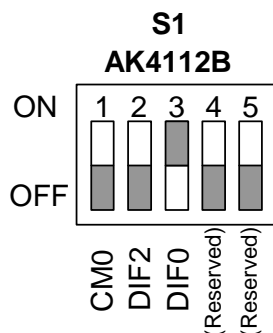


Set up the control registers DIF1/0 of the AK4705A by enclosed software as follows.



Note 2. 18bit LSB justified

Set up the DIP-switch as follows.

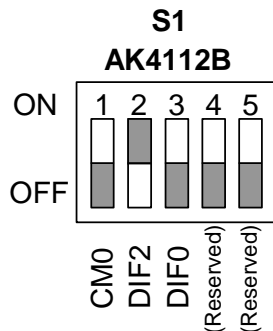


Set up the control registers DIF1/0 of the AK4705A by enclosed software as follows.



Note 3. 24bit MSB justified

Set up the DIP-switch as follows.

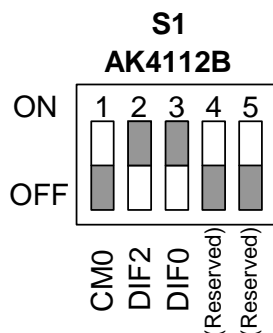


Set up the control registers DIF1/0 of the AK4705A by enclosed software as follows.



Note 4. 24bit I²S (Default)

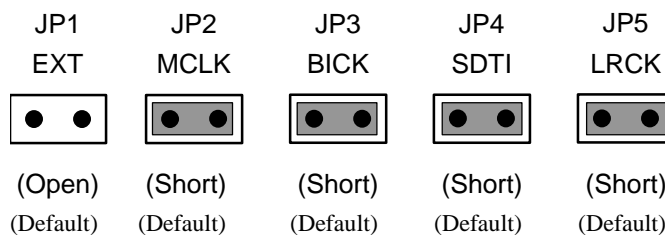
Set up the DIP-switch as follows.



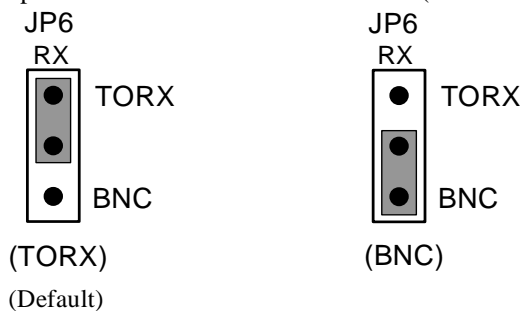
Set up the control registers DIF1/0 of the AK4705A by enclosed software as follows.



1)-2. Jumper pins set up



The JP6 selects the input port of S/PDIF bit stream form Port2 (TOTX176) or J2 (BNC RX).



2) On-board X'tal mode/ Feeding external MCLK via BNC

When the CM0 (DIP-switch S1_1 on board) is “H”, the AK4112B generates MCLK, BICK and LRCK from on-board X'tal or external clock form J1. SDATA should be fed via PORT1.

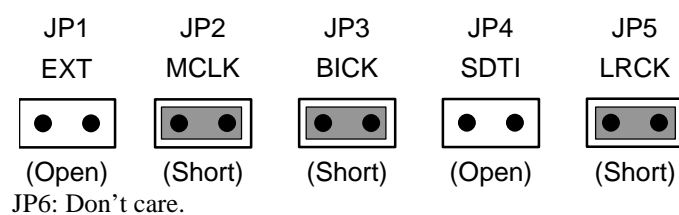
2)-1. DIP-switch set-up

| No. | CM0 | DIF2 | DIF0 |
|-----|-----|------------|------------|
| 1 | “H” | Don't care | Don't care |

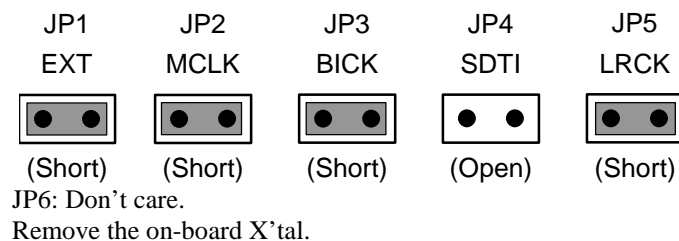
Table 3. DIP-switch set-up (DIF1=“L”)

2)-2. Jumper pins set up

2)-2-a. Using on-board X'tal



2)-2-b. Using external clock via BNC connector J1



3) Feeding all clocks from external

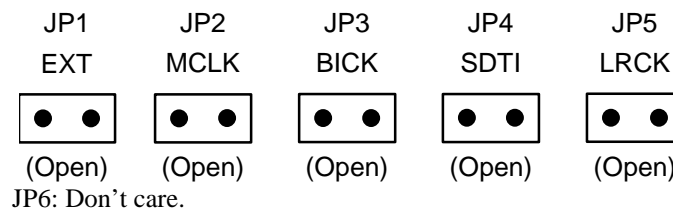
Under the following set-up, all external signals can be fed to the AK4705A through POTR1 (EXT).
The AKM's evaluation board for ADC can be used.

3)-1. DIP-switch set-up

| No. | CM0 | DIF2 | DIF0 |
|-----|------------|------------|------------|
| 1 | Don't care | Don't care | Don't care |

Table 4. DIP-switch set-up (DIF1="L")

3)-2. Jumper pins set up

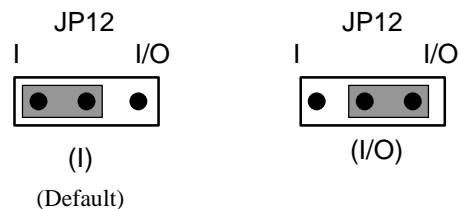


■ Other jumper pins set up

[JP12](VCRRC): Input Jack selection for the VCRRC pin of AK4705A

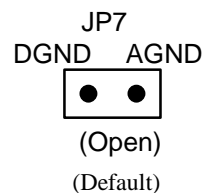
When the VCRC pin of the AK4705A outputs 0V by setting CIO bit to "1", the signal can be fed through the J27 (VCRRCOUT) to VCRRC pin.

- "I": The signal is fed through the J18 (VCRRC) to VCRRC pin. (Default)
- "I/O": The signal is fed through the J27 (VCRRCOUT) to VCRRC pin.
The CIO bit of AK4705A should be set to "1".



[JP7](GND): Analog ground and digital ground

- Open: separated. (Default)
- Short: connected. (The jack "DGND" can be open.)



■ DIP-switch (S1) List

| No. | Switch Name | Default | Function |
|-----|-------------|---------|---|
| 1 | CM0 | OFF | S/P DIF mode (Refer the evaluation mode) |
| 2 | DIF2 | ON | 24 bit I2S mode (Refer the evaluation mode) |
| 3 | DIF0 | ON | |
| 4 | - | OFF | (Reserved) |
| 5 | - | OFF | (Reserved) |

Table 5. DIP-switch list (DIF1="L")

■ Jumper List

| No. | Jumper Name | Function |
|-------------|---------------------------|---|
| 1 | EXT | MCLK source set-up when CM0="H". Open: X'tal (Default). Short: External clock via BNC (J1). Remove the on-board X'tal. |
| 2,3, 4,5 | MCLK, BICK, LRCK, SDTI | Clock source set-up Short: Connect the DIR (AK4112B). (Default) Open: Separate the DIR. Supply clocks via Port1. |
| 6 | RX | S/PDIF's port set-up when CM0="L". TORX: Optical connector PORT2. (Default) BNC: BNC connector J2. |
| 7 | GND | Analog ground and digital ground Open: separated (Default). Short: connected (The connector "DGND" can be open.). |
| 8 | D-A | Power supply source set-up for digital section of AKD4705A-A. Open: from the "D5V" Jack. Short: from the regulator or the "+5V" Jack. Don't connect anything to the "D5V" Jack. (Default) |
| 9 | REG | Power supply source set-up for VD of AK4705A. Open: from the "+5V" Jack. Short: from the regulator. Don't connect anything the "+5V" Jack. (Default) |
| 10 | VVD1 | Power supply source set-up for VVD1 of AK4705A. Open: from the "VVD1" Jack. Short: from the regulator or the "+5V" Jack. Don't connect anything to the "VVD1" Jack. (Default) |
| 11 | VVD2 | Power supply source set-up for VVD1 of AK4705A. Open: from the "VVD2" Jack. Short: from the regulator or the "+5V" Jack. Don't connect anything to the "VVD2" Jack. (Default) |
| 12 | VCRRC | Input Selection for VCRRC "I" side: Input to VCRRC from VCRRC jack. (Default) "I/O" side: Input to VCRC from VCRC jack. (Note: Refer CIO bit of AK4705A) |

Table 6. Jumper list

■ Serial Control

The AK4705A-A can be controlled via the printer port (parallel port) of IBM-AT compatible PC. Connect PORT3 (μ P-IF) with PC by 10 wire flat cable packed with the AKD4705A-A.

Be careful connector direction. Flat cable should be connected 10-pin header, red line put on 10pin header 5 and 6 pin.

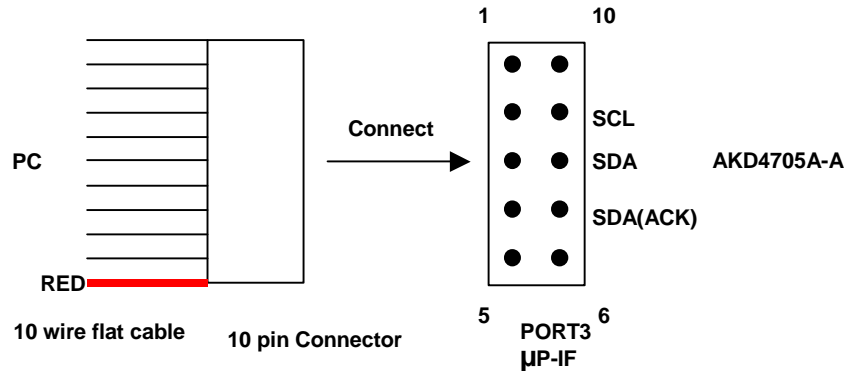


Figure 2. Connection of 10 pin flat cable for PORT3

■ Input/Output port List

| | | Signal Name | Notes |
|---------------|--------|---|----------------|
| Audio | Input | J5 (VCRINL), J3 (VCRINR), J9 (TVINL), J8 (TVINR) | Max: 2Vrms |
| | Output | J12 (VCROUTL), J10 (VCROUTR), J6 (TVOUTL), J7 (TVOUTR), J4 (MONOOUT) | Max: 3Vrm |
| Digital | Input | Port2 (TORX176) or J2 BNC (RX) | Max: D5V+0.3V |
| Video | Input | J13 (ENCB), J15 (ENCG), J17 (ENCRC), J19 (ENCC), J21 (ENCV), J23(ENCY), J25(TVVIN), J14(VCRVIN), J18(VCRRC; Note), J20(VCRG), J22(VCRB) | Max: 1.5Vp-p |
| | Output | J27 (VRCOUT; Note), J29 (TVVOUT), J30 (TVRC), J31 (TVG), J32 (TVB), J33 (RFV), J34 (VCRVOUT) | Max: 3Vp-p |
| Slow Blanking | Input | J24 (VCRSB) | Max: VP+0.3V |
| | Output | J24 (VCRSB), J28 (TVSB) | Max: VP |
| Fast Blanking | Input | J16 (VCRFB) | Max: VVD1+0.3V |
| | Output | J26 (TVFB) | Max: VVD2 |

Table 7. Input / Output port List

Note 3. Please refer to JP12 and CIO bit of the AK4705A.

■ The indication content for LED

LED turns on during each output is “H”.

[LE1] Indicates unlock or parity error of S/PDIF. Connected to the ERF pin of DIR (AK4112B).
(Normally off.)

[LE2] Indicates the validity status of S/PDIF. Connected to the V pin of DIR (AK4112B).
(Normally off.)

■ Toggle switch (SW1 on board) operation

“H”: AK4705A is active.

“L”: AK4705A is powered down.

Note 4. When the power of AKD4705A-A is ON at first, SW1 should be switched from “L” to “H”.

4) Control Software Manual

■ Set-up of evaluation board and control software

1. Set up the AKD4705A-A according to previous term.
2. Connect IBM-AT compatible PC with AKD4705A-A by 10-line type flat cable (packed with AKD4705A-A). Take care of the direction of 10pin header. (Please install the driver in the CD-ROM when this control software is used on Windows 2000/XP. Please refer "Installation Manual of Control Software Driver by AKM device control software". In case of Windows95/98/ME, this installation is not needed. This control software does not operate on Windows NT.)
3. Insert the CD-ROM labeled "AK4705A Evaluation Kit" into the CD-ROM drive.
4. Access the CD-ROM drive and double-click the icon of "akd4705a-a.exe" to set up the control program.
5. Then please evaluate according to the follows.

■ Operation flow

Keep the following flow.

1. Set up the control program according to explanation above.
2. Click "Port Reset" button.
3. Click "Write default" button

■ Explanation of each buttons

1. [Port Reset]: Set up the USB interface board (AKDUSBIF-A) when using the board.
2. [Write default]: Initialize the register of AK4705A.
3. [All Write]: Write all registers that is currently displayed.
4. [Function1]: Dialog to write data by keyboard operation.
5. [Function2]: Dialog to write data by keyboard operation.
6. [Function3]: The sequence of register setting can be set and executed.
7. [Function4]: The sequence that is created on [Function3] can be assigned to buttons and executed.
8. [Function5]: The register setting that is created by [SAVE] function on main window can be assigned to buttons and executed.
9. [SAVE]: Save the current register setting.
10. [OPEN]: Write the saved values to all register.
11. [Write]: Dialog to write data by mouse operation.

■ Indication of data

Input data is indicated on the register map. Red letter indicates "H" or "1" and blue one indicates "L" or "0". Blank is the part that is not defined in the datasheet.

■ Explanation of each dialog

1. [Write Dialog]: Dialog to write data by mouse operation

There are dialogs corresponding to each register.

Click the [Write] button corresponding to each register to set up the dialog. If you check the check box, data becomes "H" or "1". If not, "L" or "0".

If you want to write the input data to the AK4705A, click [OK] button. If not, click [Cancel] button.

2. [Function1 Dialog]: Dialog to write data by keyboard operation

Address Box: Input registers address in 2 figures of hexadecimal.

Data Box: Input registers data in 2 figures of hexadecimal.

If you want to write the input data to the AK4705A, click [OK] button. If not, click [Cancel] button.

3. [Function2 Dialog]: Dialog to evaluate DATT

There are dialogs corresponding to register of 02h.

Address Box: Input registers address in 2 figures of hexadecimal.

Start Data Box: Input starts data in 2 figures of hexadecimal.

End Data Box: Input end data in 2 figures of hexadecimal.

Interval Box: Data is written to AK4705A by this interval.

Step Box: Data changes by this step.

Mode Select Box:

If you check this check box, data reaches end data, and returns to start data.

[Example] Start Data = 00, End Data = 09

Data flow: 00 01 02 03 04 05 06 07 08 09 09 08 07 06 05 04 03 02 01 00

If you do not check this check box, data reaches end data, but does not return to start data.

[Example] Start Data = 00, End Data = 09

Data flow: 00 01 02 03 04 05 06 07 08 09

If you want to write the input data to the AK4705A, click [OK] button. If not, click [Cancel] button.

4. [SAVE] and [OPEN]

4-1. [SAVE]

All of current register setting values displayed on the main window are saved to the file. The extension of file name is "akr".

<Operation flow>

- (1) Click [SAVE] Button.
- (2) Set the file name and click [SAVE] Button. The extension of file name is "akr".

4-2. [OPEN]

The register setting values saved by [SAVE] are written to the AK4705A. The file type is the same as [SAVE].

<Operation flow>

- (1) Click [OPEN] Button.
- (2) Select the file (*.akr) and Click [OPEN] Button.

5. [Function3 Dialog]

The sequence of register setting can be set and executed.

(1) Click [F3] Button. The following is displayed.

(2) Set the control sequence.

Set the address, Data and Interval time. Set "-1" to the address of the step where the sequence should be paused.

(3) Click [START] button. Then this sequence is executed.

The sequence is paused at the step of Interval="-1". Click [START] button, the sequence restarts from the paused step.

This sequence can be saved and opened by [SAVE] and [OPEN] button on the Function3 window. The extension of file name is "aks".

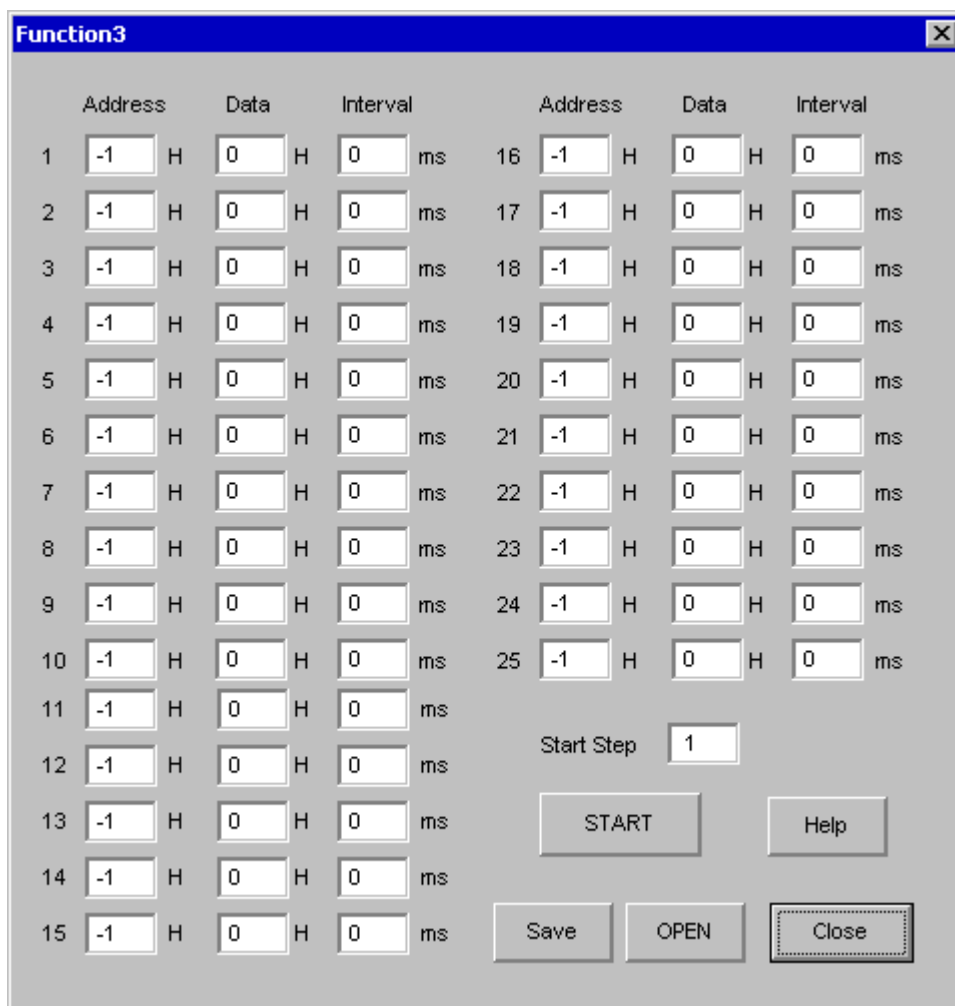


Figure 3. Window of [F3]

6. [Function4 Dialog]

The sequence file (*.aks) saved by [Function3] can be listed up to 10 files, assigned to buttons and then executed. When [F4] button is clicked, the window as shown in Figure 2 opens.

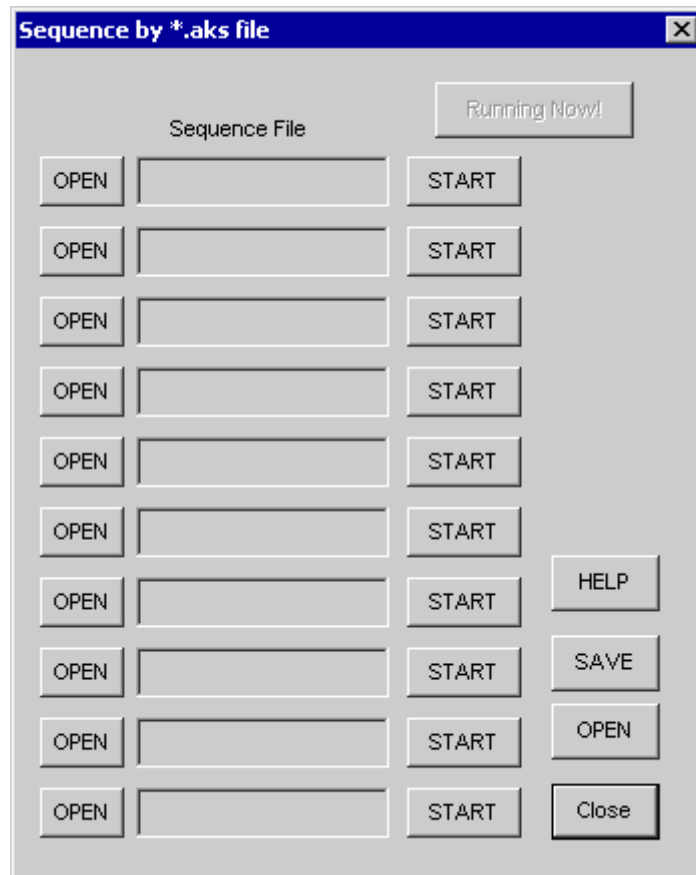


Figure 4. [F4] window (1)

6-1. [OPEN] buttons on left side and [START] buttons

(1) Click [OPEN] button and select the sequence file (*.aks) saved by [Function3].

The sequence file name is displayed as shown in Figure 3. (In case that the selected sequence file name is “DAC_Stereo_ON.aks”)

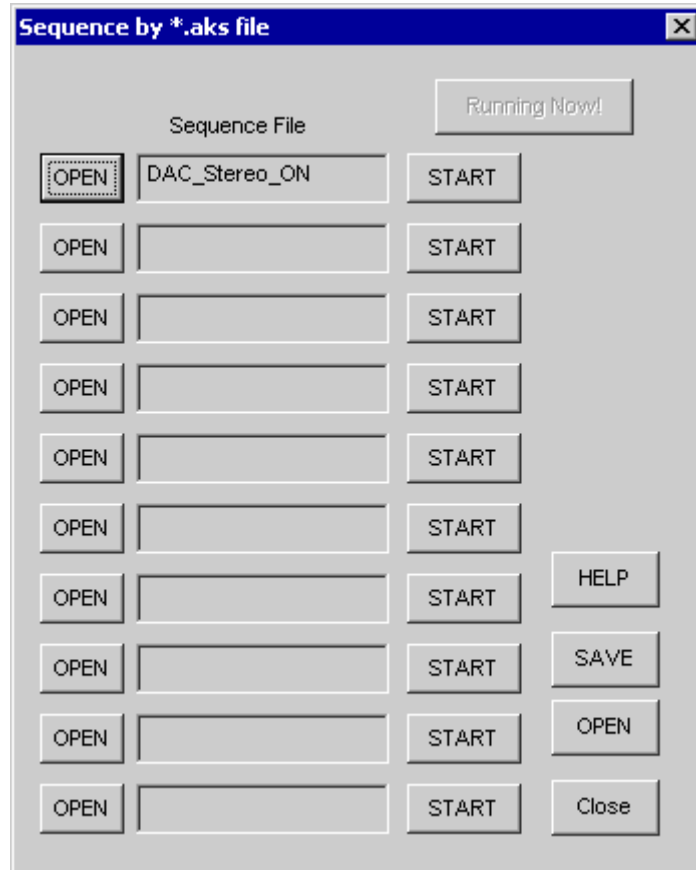


Figure 5. [F4] window (2)

(2) Click [START] button, then the sequence is executed.

6-2. [SAVE] and [OPEN] buttons on right side

[SAVE] : The name assign of sequence file displayed on [Function4] window can be saved to the file. The file name is “*.ak4”.

[OPEN] : The name assign of sequence file(*.ak4) saved by [SAVE] is loaded.

6-3. Note

- (1) This function doesn't support the pause function of sequence function.
- (2) All files used by [SAVE] and [OPEN] function on right side need to be in the same folder.
- (3) When the sequence is changed in [Function3], the sequence file (*.aks) should be loaded again in order to reflect the change.

7. [Function5 Dialog]

The register setting file (*.akr) saved by [SAVE] function on main window can be listed up to 10 files, assigned to buttons and then executed. When [F5] button is clicked, the window as shown in Figure 4 opens.

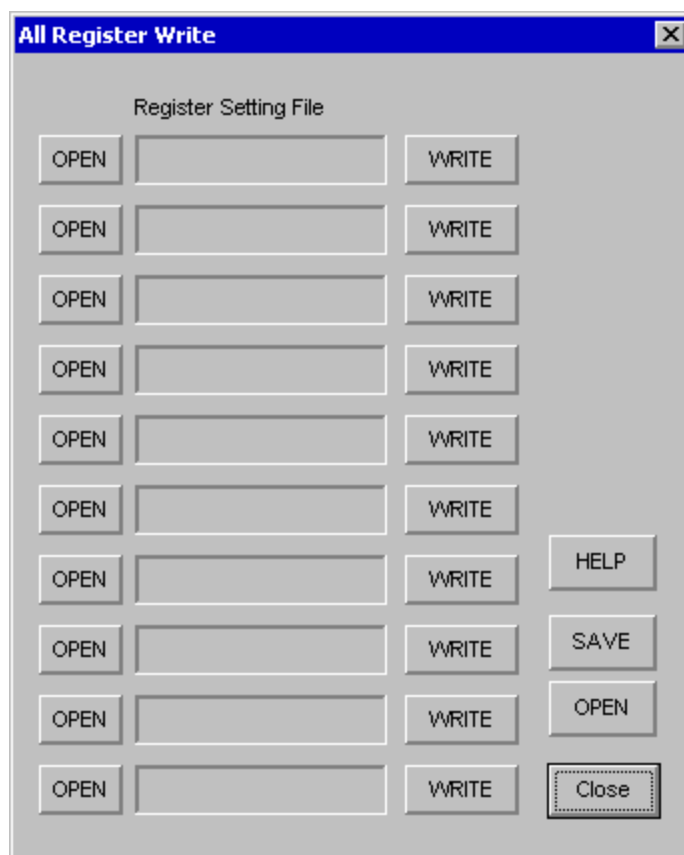


Figure 6. [F5] window

7-1. [OPEN] buttons on left side and [WRITE] button

- (1) Click [OPEN] button and select the register setting file (*.akr).

The register setting file name is displayed as shown in Figure 7. [F5] windows (2). (In case that the selected file name is "DAC_Output.akr")

- (2) Click [WRITE] button, then the register setting is executed.

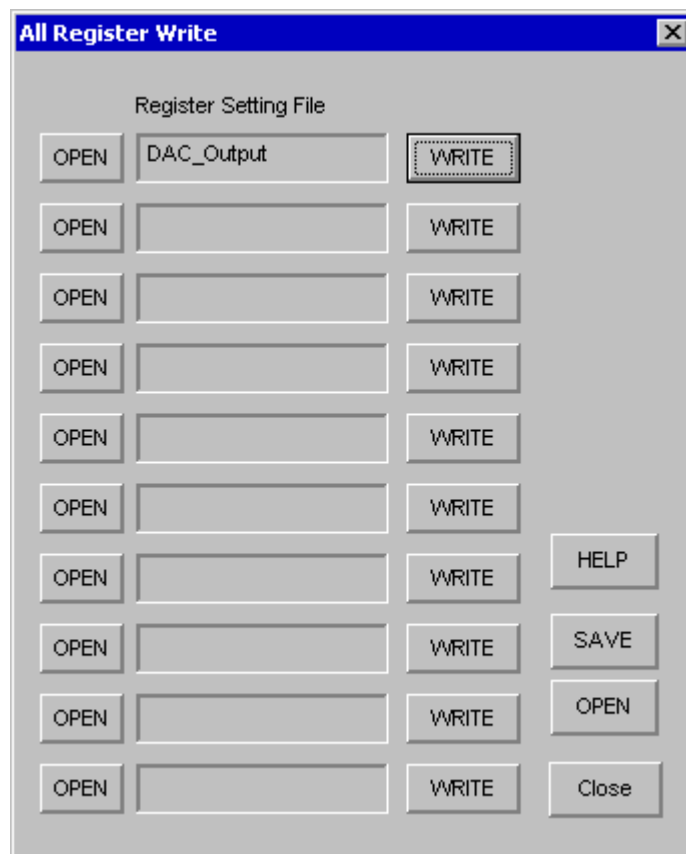


Figure 7. [F5] windows (2)

7-2. [SAVE] and [OPEN] buttons on right side

[SAVE] : The name assign of register setting file displayed on [Function5] window can be saved to the file. The file name is “*.ak5”.

[OPEN] : The name assign of register setting file(*.ak5) saved by [SAVE] is loaded.

7-3. Note

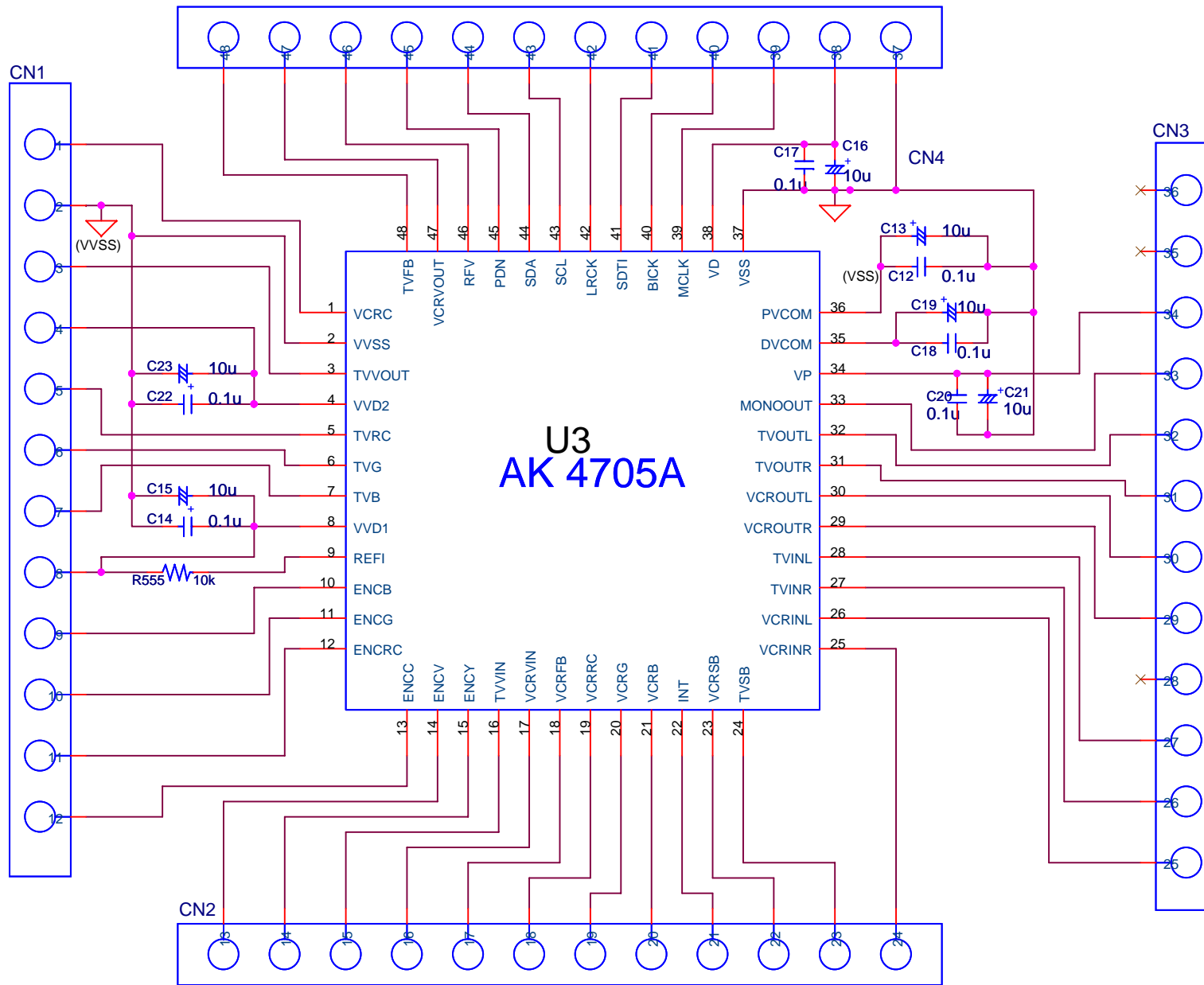
- (1) All files used by [SAVE] and [OPEN] function on right side need to be in the same folder.
- (2) When the register setting is changed by [SAVE] Button on the main window, the register setting file (*.akr) should be loaded again in order to reflect the change.

REVISION HISTORY

| Date (yy/mm/dd) | Manual Revision | Board Revision | Reason | Page | Contents |
|--------------------|--------------------|-------------------|---------------|------|----------|
| 07/09/26 | KM091000 | 0 | First Edition | | |

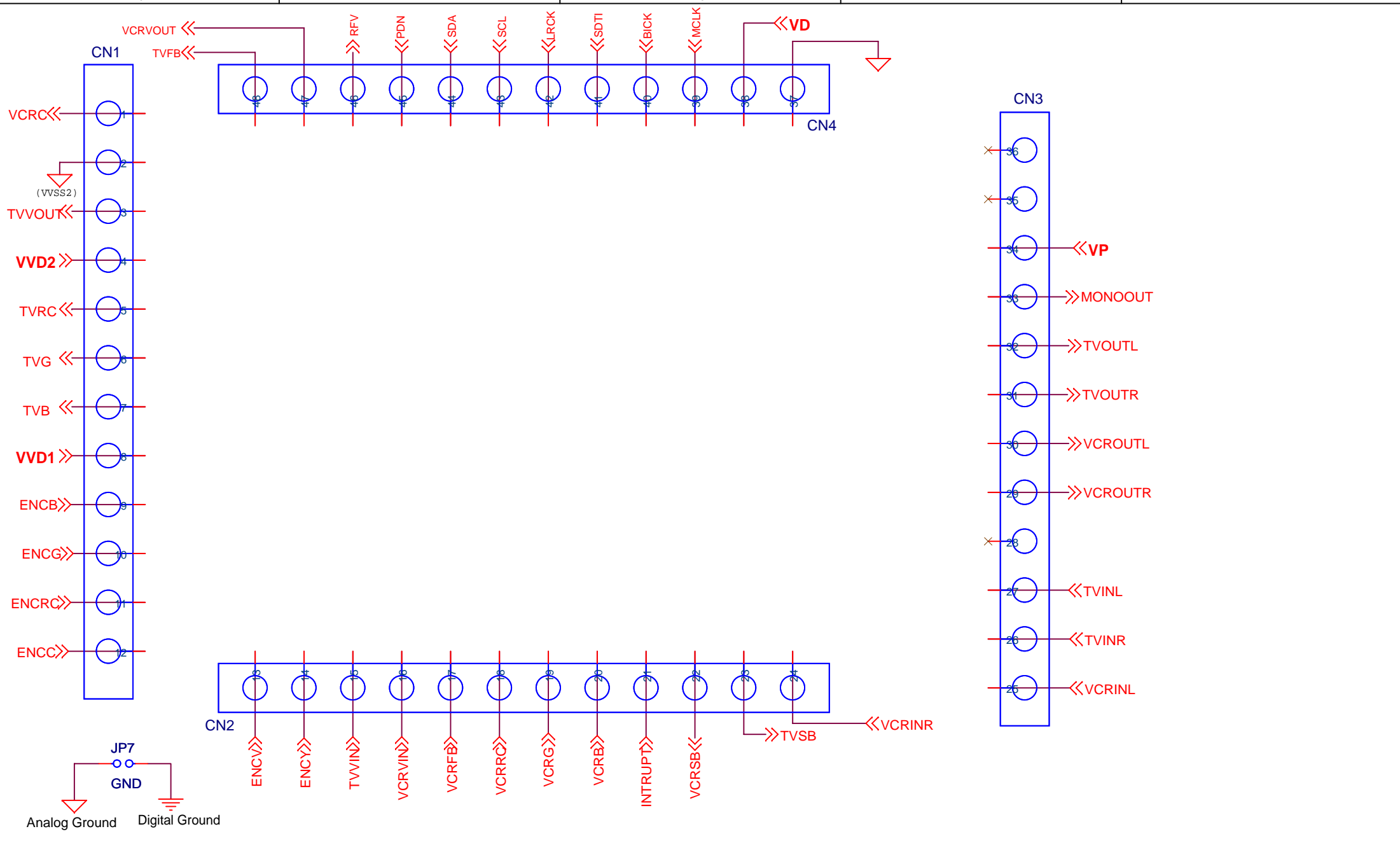
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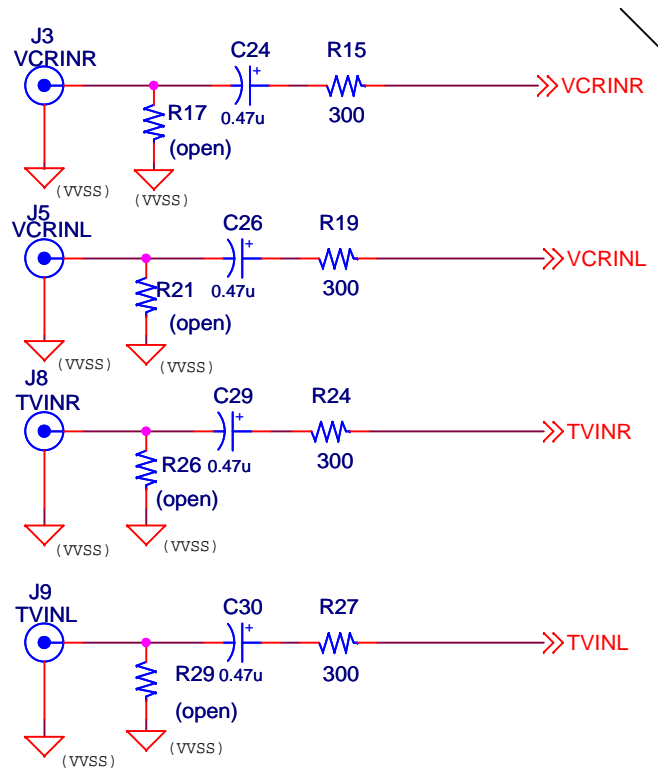


U3
AK 4705A

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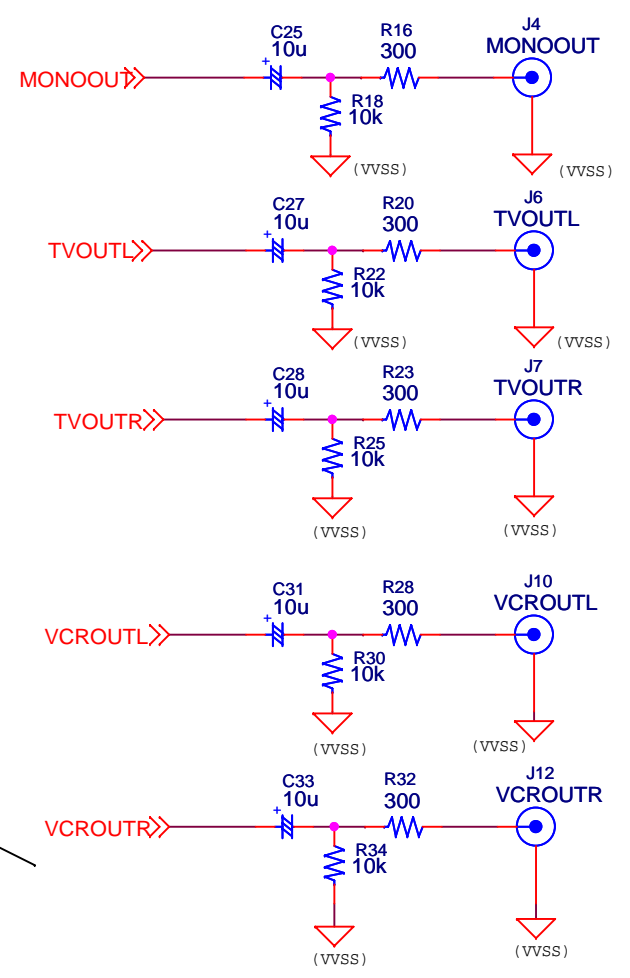


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| Date: | Sheet | | 2 | of | 6 |

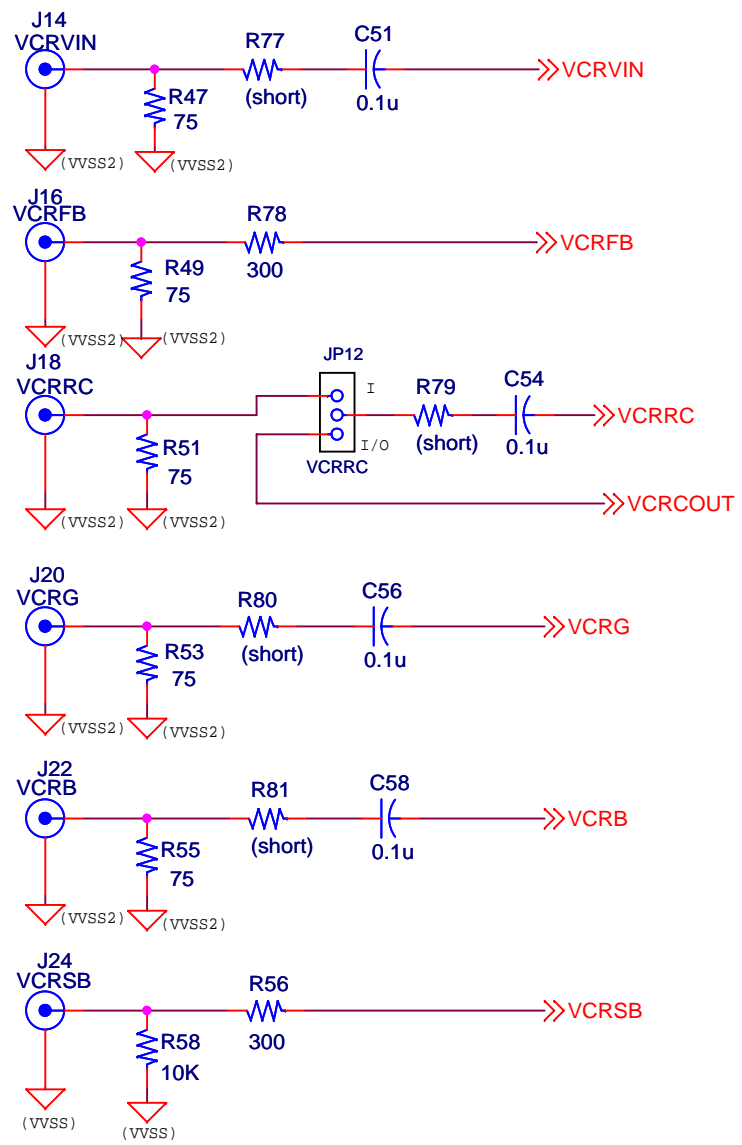
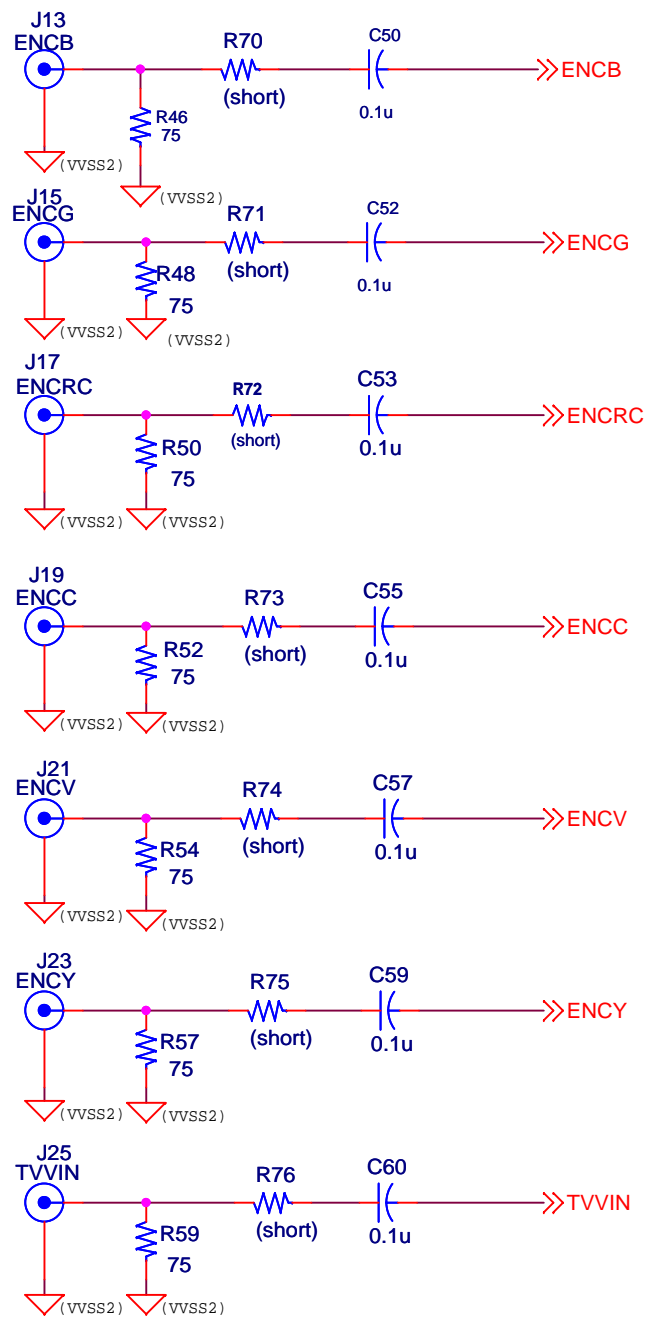


FOR Analog
input

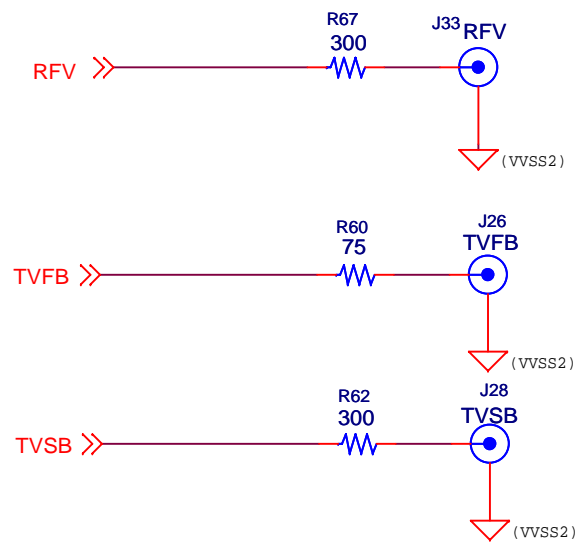
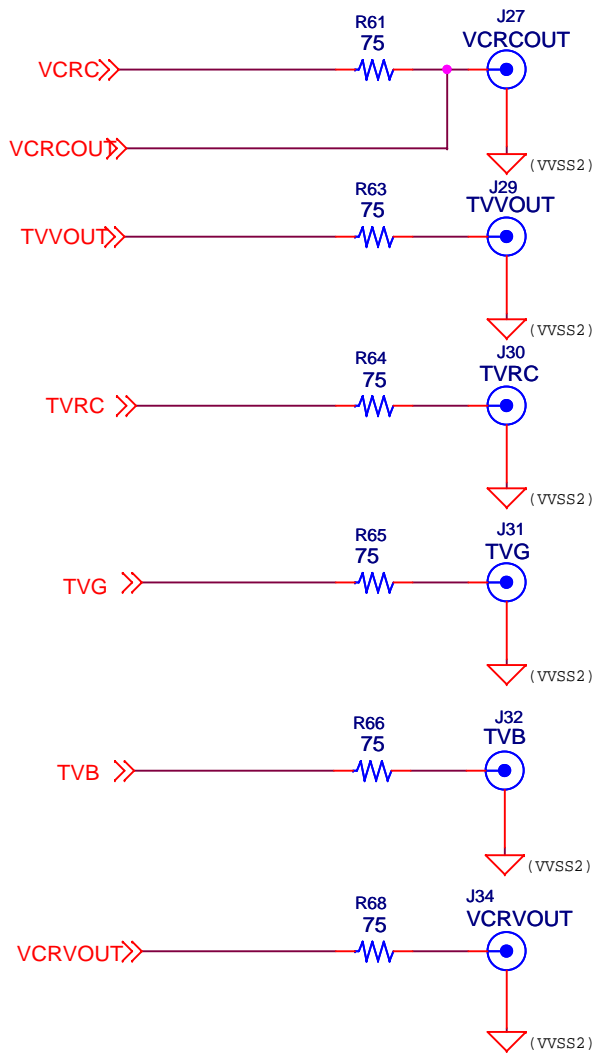
From Analog
output



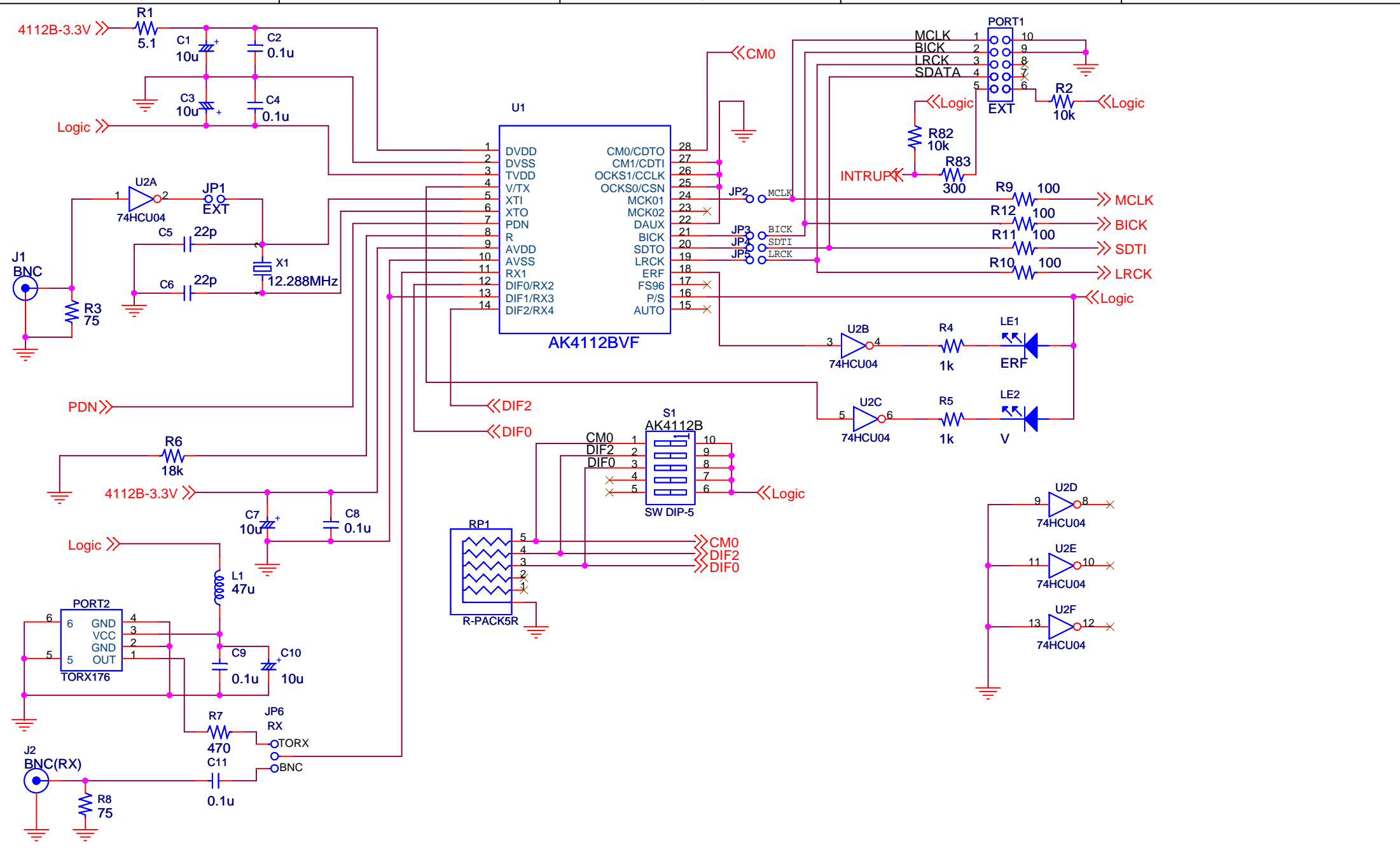
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| Title | | | AKD4705A-A | | |
| Size | Document Number | | | | Rev |
| A4 | Analog Input/Output Circuit | | | | 0 |
| Date: | Thursday, September 13, 2007 | | | | Sheet 3 of 6 |



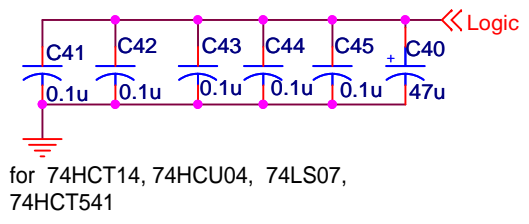
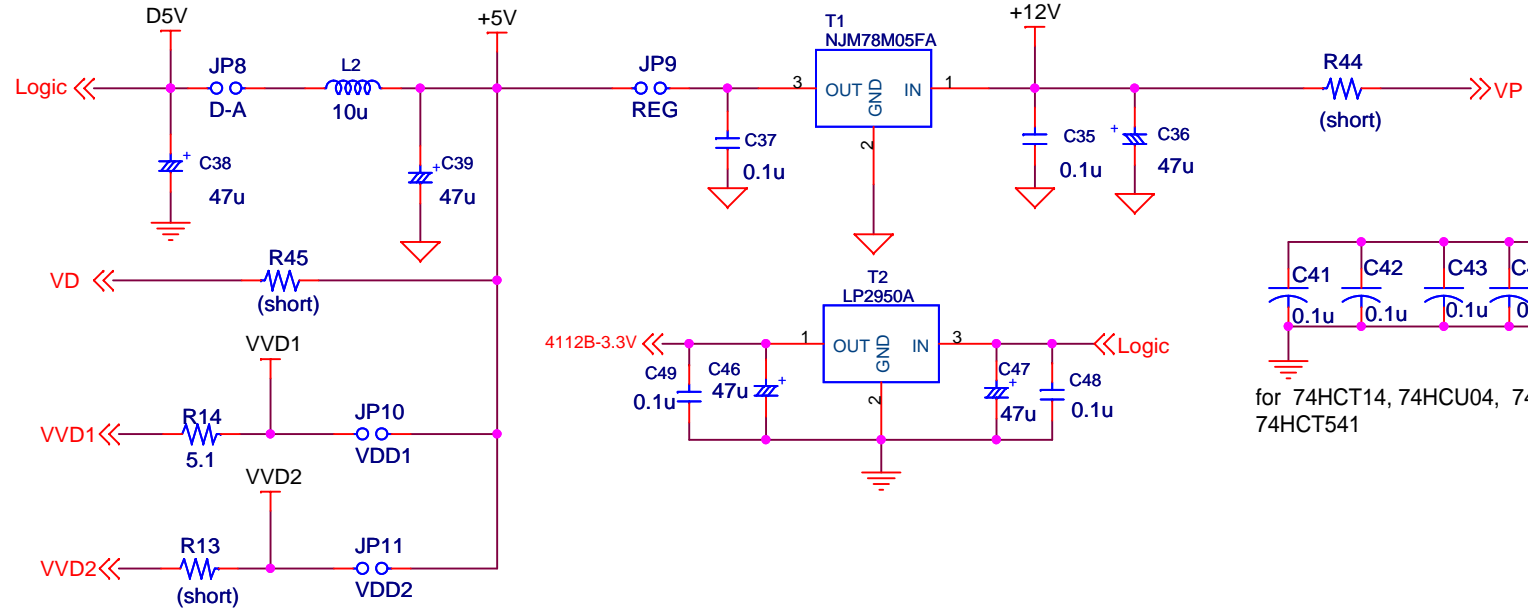
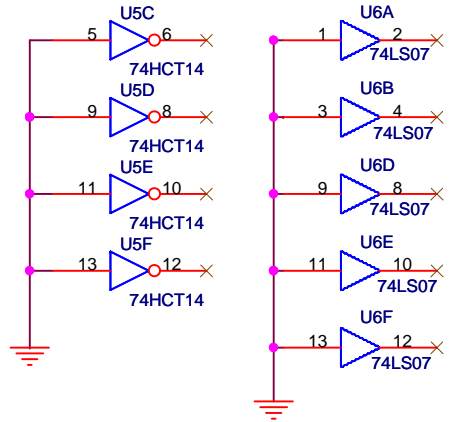
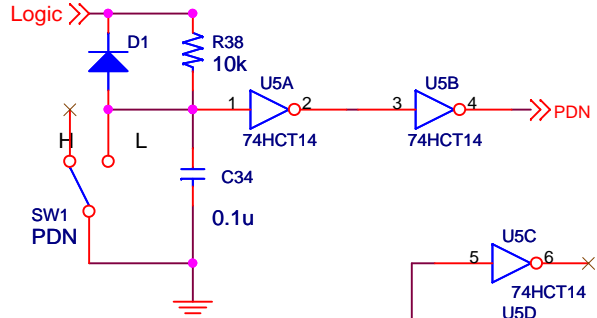
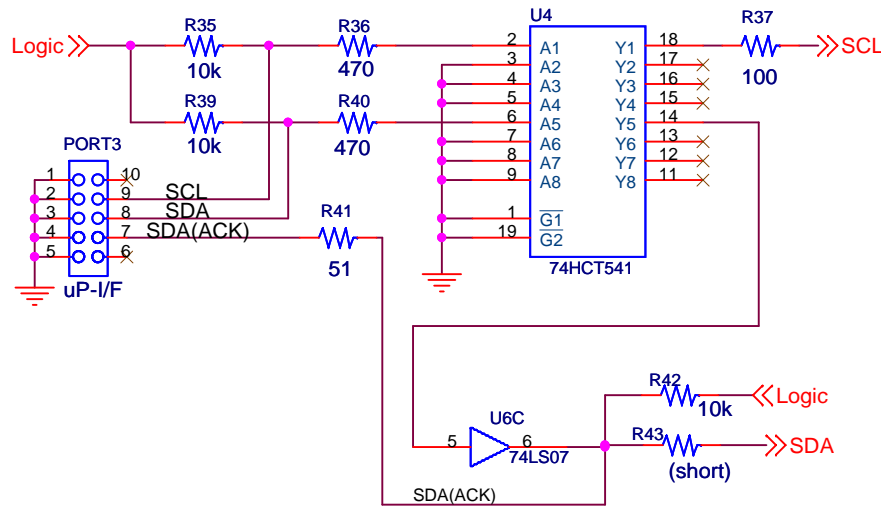
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| Title | | | AKD4705A-A | | |
| Size | Document Number | | | Rev | |
| A4 | Video Block Input Circuit | | | 0 | |
| Date: | Sheet | | 5 | of | 6 |



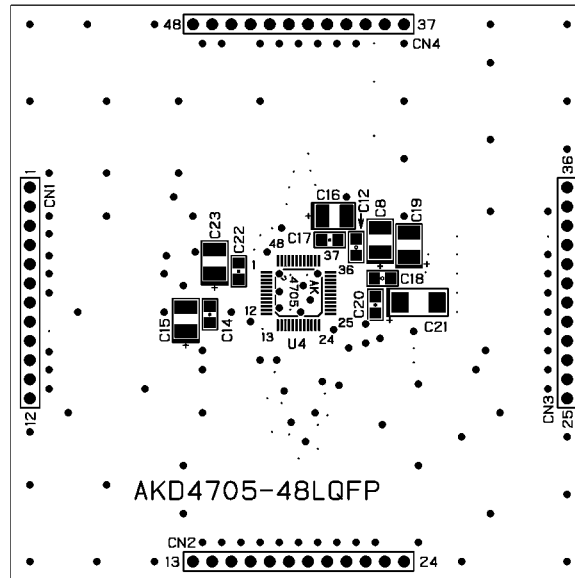
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| Size | Document Number | Rev | | | |
| A4 | Video Block Output Circuit | 0 | | | |
| Date: | 2 | Sheet | 6 | of | 6 |



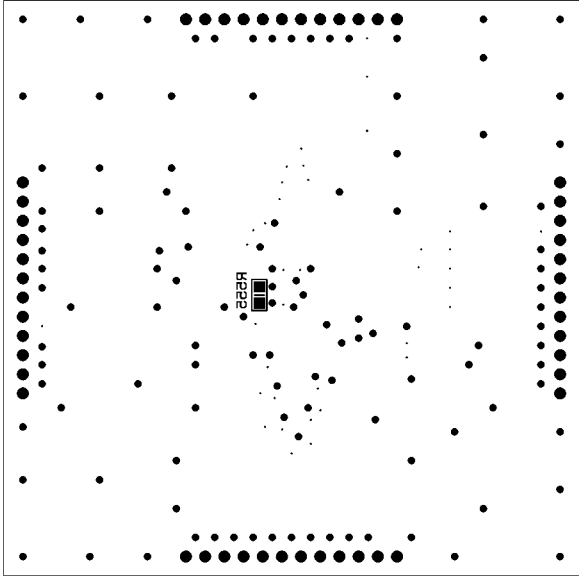
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| Size | Document Number | | | | Rev |
| A4 | AK4112B | | | | 0 |
| Date: | Sheet 1 of 6 | | | | |



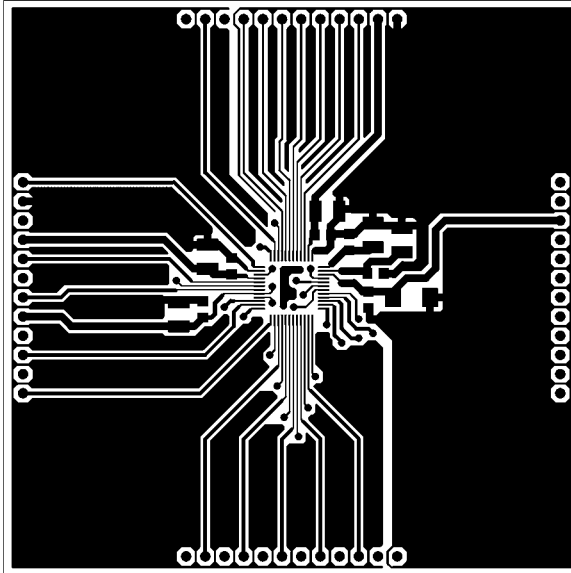
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| Size | | | | | |
| A4 | Document Number | | POWER SUPPLY | | |
| Date: | Rev | | | | |
| 2 | 1 | | 0 | | |
| Sheet | | | 4 of 6 | | |



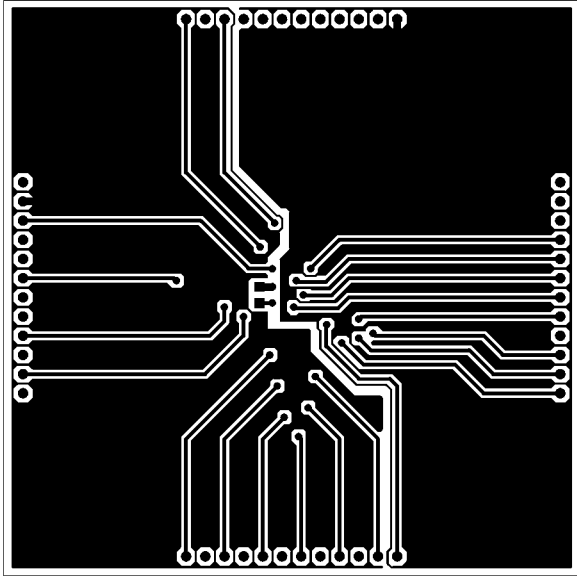
AKD4705 Rev.0 48LQFP L1 SR SILK



AKD4705 Rev.0 48LQFP LS 2R SILK



AKD4705 Rev.0 48LQFP L1



AKD4705 Rev.0.48LQFP LS

