May 1990

PRODUCT PROFILE

FUJITSU

MB85414-30/-40

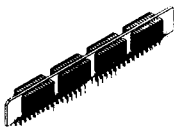
CMOS STATIC RAM MODULE

PRELIMINARY

16384 Words x 32-Bit

The Fujitsu MB85414 is a fully decoded, CMOS static random access memory module (SRAM) with eight MB81C75 devices mounted on a 64-pin Epoxy module. These modules incorporate a presence detect feature that permits system level memory density verification for those applications with multiple modules. Organized as eight 16K x 4 common I/O devices, the MB85414 is optimized for memory applications where low power, high performance, large memory storage, and high density are required.

- Organized as 16384 x 32-Bit Words
- Access Time/Cycle Time
  - −30: 30 ns
  - −40: 40 ns
- Low Power Dissipation
  - Active: 3520 mW (Max)
  - Standby: 440 mW CMOS Level
  - 880 mW TTL Level
- Static Operation
- Single +5 V ±10% Power Supply
- Four Select Pins (x8, x16, x32)
- Presence Detect: PD0 = GND; PD1 = Open
- Common Data Inputs and Outputs
- 64-pin Epoxy Module (ZIP)
- Input/Output Pins TTL Compatible
- Temperature Range: 0°C to 70°C



PLASTIC PACKAGE
MZP-64P-P01

PIN ASSIGNMENT

PD0	2	1	VSS
DQ0	4	3	PD1
DQ1	6	5	DQ4
DQ2	8	7	DQ5
DQ3	10	9	DQ6
VCC	12	11	DQ7
A6	14	13	A7
A10	16	15	A5
A3	18	17	A11
DQ8	20	19	DQ12
DQ9	22	21	DQ13
DQ10	24	23	DQ14
DQ11	26	25	DQ15
$\overline{W}$	28	27	VSS
NC	30	29	NC
$\overline{CS1}$	32	31	$\overline{CS2}$
$\overline{CS3}$	34	33	$\overline{CS4}$
NC	36	35	NC
VSS	38	37	$\overline{OE}$
DQ16	40	39	DQ20
DQ17	42	41	DQ21
DQ18	44	43	DQ22
DQ19	44	45	DQ23
A1	48	47	A2
A9	50	49	A4
A0	52	51	A13
A12	54	53	VCC
DQ24	56	55	A8
DQ25	58	57	DQ28
DQ26	60	59	DQ29
DQ27	62	61	DQ30
VSS	64	63	DQ31

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Rating
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{IN}	−3.5 to +7.0	V
Output Voltage	V_{OUT}	−0.5 to +7.0	V
Short Circuit Output Current	I_{OUT}	±50	mA
Power Dissipation	P_D	8.0	W
Temperature under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature	T_{STG}	−45 to +125	°C

NOTE: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational section of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

CAPACITANCE (T_A = 25°C, f = 1MHz)

PARAMETER	SYMBOL	VALUE		UNIT
		Typ	Max	
Input Capacitance, Address, $\overline{WE}$ and $\overline{OE}$	C_{IN1}		90	pF
Input Capacitance, $\overline{CS}_{1-4}$	C_{IN2}		30	pF
Output Capacitance, DQ_{0-31}	$C_{I/O}$		12	pF

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DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted)

PARAMETER		SYMBOL	VALUE			UNIT
			Min	Typ	Max	
Input Leakage Current (V_{IN} = OV to V_{CC})		I_{LI}	−80		80	µA
Output Leakage Current ($\overline{CS}$ = V_{IH}, V_{OUT} = OV to V_{CC})		I_{LO}	−10		10	µA
Standby Power Supply Current	CMOS level	I_{SB1}			80	mA
	TTL level	I_{SB2}			160	mA
Active Power Supply Current ($\overline{CS}$ = V_{IL}, I_{OUT} = O mA)		I_{CC1}			480	mA
Operating Supply Current (Cycle = Min., I_{OUT} = 0 mA)		I_{CC2}			640	mA
Input High Level		V_{IH}	2.2		6.0	V
Input Low Level[1]		V_{IL}	−0.5		0.8	V
Output High Level (I_{OH} = −4 mA)		V_{OH}	2.4			V
Output Low Level (I_{OL} = 16 mA)		V_{OL}			0.4	V

Note: [1]−2.OV level with a maximum pulse width of 20 ns.

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted)*

READ CYCLE

PARAMETER	SYM	MB85414–30		MB85414–40		UNIT	NOTE
		Min	Max	Min	Max		
Read Cycle Time	t_{RC}	30		40		ns	1
Address Access Time	t_{AA}		30		40	ns	
$\overline{CS}$ Access Time	t_{ACS}		30		40	ns	2
$\overline{OE}$ Access Time	t_{OE}		15		20	ns	2
Output Hold from Address Change	t_{OH}	5		5		ns	
Output Hold from Output Disable	t_{OHC}	3		3		ns	
$\overline{CS}$ to Output Low–Z	t_{CLZ}	5		5		ns	3,4
$\overline{OE}$ to Output Low–Z	t_{OLZ}	0		0		ns	3,4
$\overline{CS}$ to Output High–Z	t_{CHZ}		10		15	ns	3,4
$\overline{OE}$ to Output High–Z	t_{OHZ}		10		15	ns	3,4
Power Up from $\overline{CS}$	t_{PU}	0		0		ns	
Power Down from $\overline{CS}$	t_{PD}		20		30	ns	

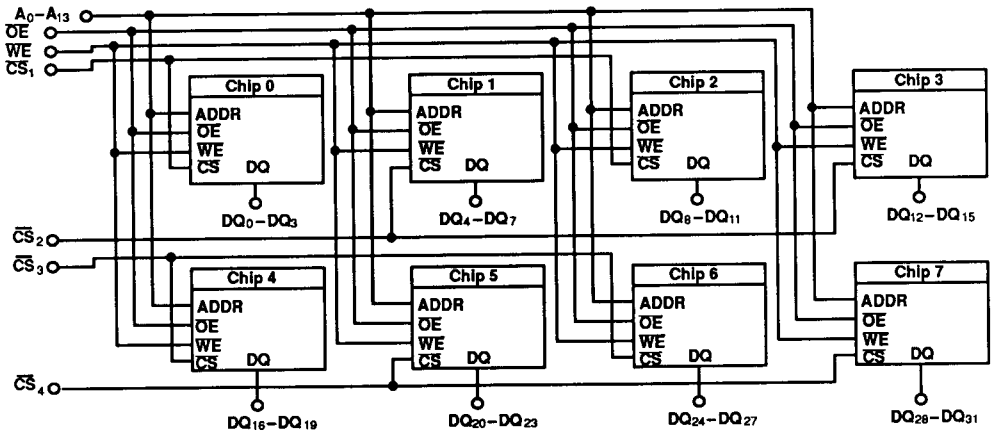
WRITE CYCLE

PARAMETER	SYM	MB85414–30		MB85414–40		UNIT	NOTE
		Min	Max	Min	Max		
Write Cycle Time	t_{WC}	30		40		ns	2
Address Valid to End of Write	t_{AW}	25		35		ns	
$\overline{CS}$ to End of Write	t_{CW}	25		35		ns	
Data Hold Time	t_{DH}	2		2		ns	
Write Pulse Width	t_{WP}	20		30		ns	
Data Valid to End of Write	t_{DW}	15		20		ns	
Address Setup Time	t_{AS}	0		0		ns	
Write Recovery Time	t_{WR}	2		2		ns	
Output High–Z from $\overline{WE}$	t_{WHZ}		10		15	ns	3,4
Output Low–Z from $\overline{WE}$	t_{LWZ}	0	20	0	20	ns	3,4

Notes: * Refer to MB81C75 data sheet electricals for an explanation of the notes.

MB85414-30/-40

FUNCTIONAL BLOCK DIAGRAM



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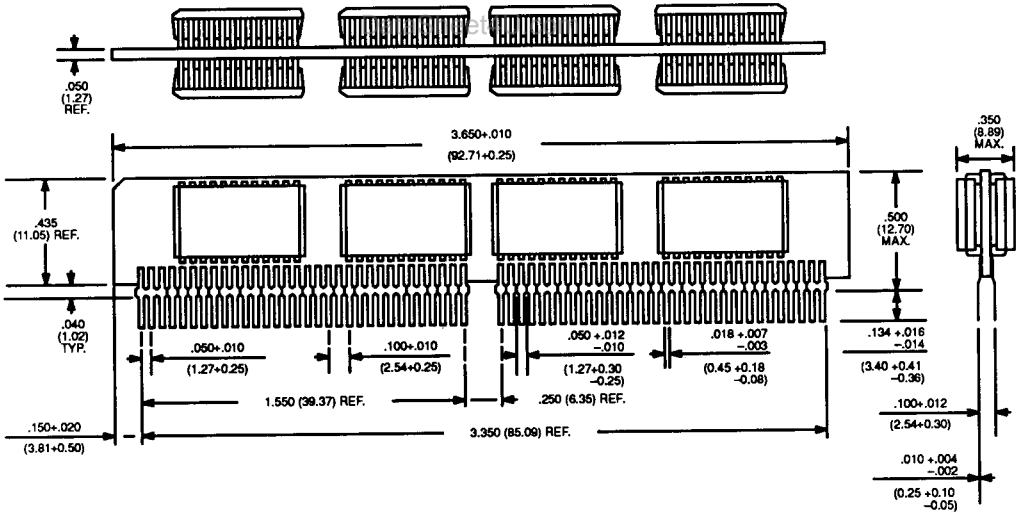
PACKAGE DIMENSIONS

64-Lead Epoxy Module
(Case No.: MZP-64P-P01)



NOTE: Dimensions in inches and (millimeters)