SYNCHRONOUS DRAM MODULE

MT2LSDT132U, MT4LSDT232UD

For the latest data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- JEDEC pinout in a 100-pin, dual in-line memory module (DIMM)
- 4MB (1 Meg x 32) and 8MB (2 Meg x 32)
- Utilizes 100 MHz and 125 MHz SDRAM components
- Single +3.3V ±0.3V power supply
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Auto Precharge and Auto Refresh Modes
- Self Refresh Mode
- 64ms, 4,096-cycle refresh
- LVTTL-compatible inputs and outputs
- Serial presence-detect (SPD)

OPTIONS   MARKING

- Package
  100-pin DIMM (gold)   G

- Timing
  8ns cycle (125 MHz clock rate)   -8
  10ns cycle (≤100 MHz clock rate)   -10

KEY SDRAM COMPONENT TIMING PARAMETERS

SPEED GRADE	CLOCK FREQUENCY	ACCESS TIME		SETUP TIME	HOLD TIME
		CL = 2*	CL = 3*		
-8	125 MHz	9ns	6ns	2ns	1ns
-10	100 MHz	9ns	7.5ns	3ns	1ns

*CL = CAS (READ) latency

PART NUMBERS

| PART NUMBER	CONFIGURATION	DEVICE PACKAGE
MT2LSDT132UG-8_	1 Meg x 32	TSOP
MT2LSDT132UG-10_	1 Meg x 32	TSOP
MT4LSDT232UDG-8_	2 Meg x 32	TSOP
MT4LSDT232UDG-10_	2 Meg x 32	TSOP

NOTE: All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT2LSDT132UG-10C1.

PIN ASSIGNMENT (Front View)
100-Pin DIMM
(H-3; 4MB)
(H-4; 8MB)
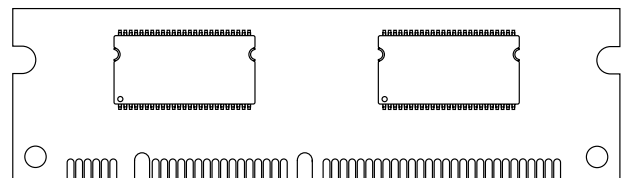
PIN	FRONT	PIN	FRONT	PIN	BACK	PIN	BACK
1	V_{SS}	26	V_{SS}	51	V_{SS}	76	V_{SS}
2	DQ0	27	CKE0	52	DQ8	77	NC/CKE1*
3	DQ1	28	WE#	53	DQ9	78	DNU
4	DQ2	29	S0#	54	DQ10	79	NC/S1#*
5	DQ3	30	S2#	55	DQ11	80	NC/S3#*
6	V_{DD}	31	V_{DD}	56	V_{DD}	81	V_{DD}
7	DQ4	32	NC	57	DQ12	82	NC
8	DQ5	33	NC	58	DQ13	83	NC
9	DQ6	34	NC	59	DQ14	84	NC
10	DQ7	35	NC	60	DQ15	85	NC
11	DQMB0#	36	V_{SS}	61	DQMB1#	86	V_{SS}
12	V_{SS}	37	DQMB2#	62	V_{SS}	87	DQMB3#
13	A0	38	DQ16	63	A1	88	DQ24
14	A2	39	DQ17	64	A3	89	DQ25
15	A4	40	DQ18	65	A5	90	DQ26
16	A6	41	DQ19	66	A7	91	DQ27
17	A8	42	V_{DD}	67	A9	92	V_{DD}
18	A10	43	DQ20	68	BA0	93	DQ28
19	NC	44	DQ21	69	NC	94	DQ29
20	NC	45	DQ22	70	NC	95	DQ30
21	V_{DD}	46	DQ23	71	V_{DD}	96	DQ31
22	DNU	47	V_{SS}	72	RAS#	97	V_{SS}
23	RFU	48	SDA	73	CAS#	98	SA0
24	RFU	49	SCL	74	RFU	99	SA1
25	CK0	50	V_{DD}	75	NC/CK1*	100	SA2

*8MB version only

GENERAL DESCRIPTION

The MT2LSDT132U and MT4LSDT232UD are high-speed CMOS, dynamic random-access, 4MB and 8MB memories organized in a x32 configuration. These modules use SDRAMs that are internally configured as dual memory arrays with a synchronous interface (all signals are registered on the positive edge of the clock signal CK0).

Read and write accesses to the SDRAM modules are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed

GENERAL DESCRIPTION (continued)

sequence. Accesses begin with the registration of an AC-TIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0 selects the bank; A0-A10 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The modules provide for programmable READ or WRITE burst lengths of 1, 2, 4 or 8 locations, or the full page, with a burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. The modules use an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the $2n$ rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing the alternate bank will hide the PRECHARGE cycles and provide seamless, high-speed, random-access operation.

The modules are designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTL-compatible.

SDRAM modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time and the capability to randomly change column addresses on each clock cycle during a burst access. For more information regarding SDRAM operation, refer to the 16Mb: x16 SDRAM data sheet.

SERIAL PRESENCE-DETECT OPERATION

These modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA(2:0), which provide eight unique DIMM/ EEPROM addresses.

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FUNCTIONAL BLOCK DIAGRAM
MT2LSDT132U (4MB)
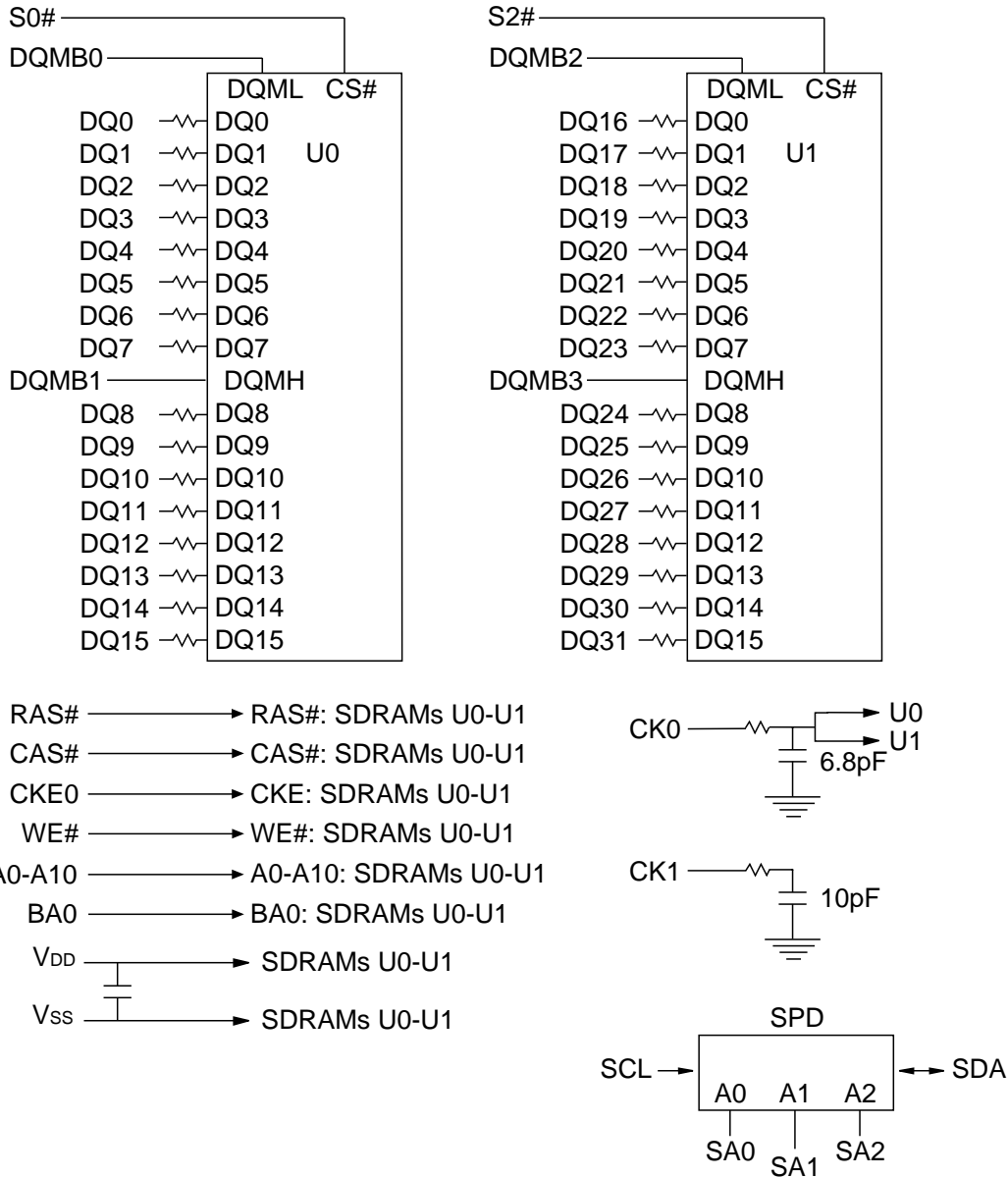
U0-U1 = MT48LC1M16A1TG SDRAMs

NOTE: 1. All resistor values are 10 ohms.
2. Reference designators in this diagram do not necessarily match the actual module.
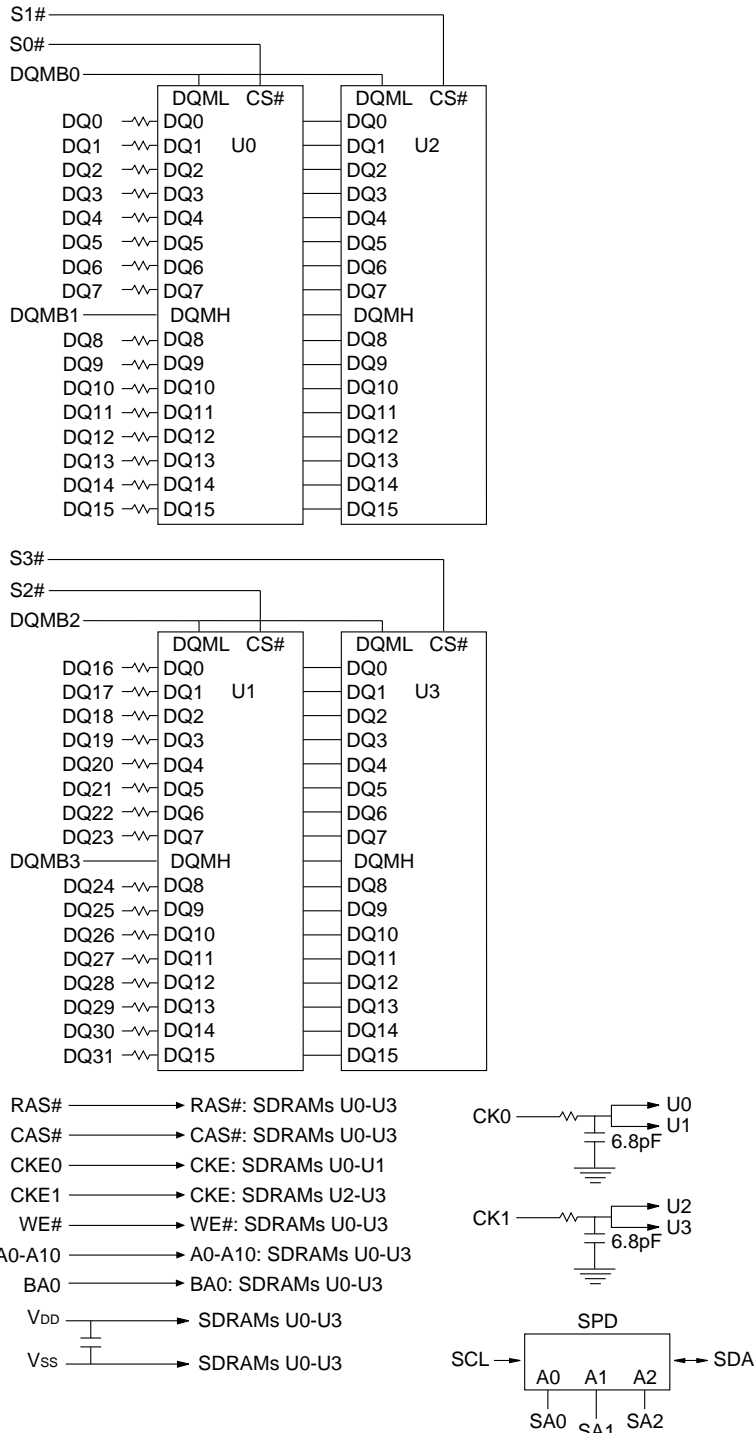
FUNCTIONAL BLOCK DIAGRAM
MT4LSDT232UD (8MB)

U0-U3 = MT48LC1M16A1TG SDRAMs

NOTE: 1. All resistor values are 10 ohms.
2. Reference designators in this diagram do not necessarily match the actual module.

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
72, 73, 28	RAS#, CAS#, WE#	Input	Command Inputs: RAS#, CAS# and WE# (along with S0#-S3#) define the command being entered.
25, 75	CK0-CK1	Input	Clock: CK0-CK1 are driven by the system clock. All SDRAM input signals are sampled on the positive edge of CK. CK also increments the internal burst counter and controls the output registers. Pin 75 is a no connect on the 4MB version.
27, 77	CKE0-CKE1	Input	Clock Enable: CKE0 and CKE1 activate (HIGH) and deactivate (LOW) the CK signal. Deactivating the clock provides POWER-DOWN and SELF REFRESH operation (all banks idle) or CLOCK SUSPEND operation (burst access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CK0-CK1, are disabled during power-down and self refresh modes, providing low standby power. Pin 77 is a no connect on the 4MB version.
29, 30, 79, 80	S0#-S3#	Input	Chip Select: S0#-S3# enable (registered LOW) and disable (registered HIGH) the command decoder. All commands are masked when S0#-S3# are registered HIGH. S0#-S3# are considered part of the command code. Pins 79 and 80 are no connects on the 4MB version.
11, 37, 61, 87	DQMB0-DQMB3	Input	Input/Output Mask: DQMB is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQMB is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (after a two-clock latency) when DQMB is sampled HIGH during a READ cycle.
68	BA0	Input	Bank Address: BA0 defines to which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied. BA0 is also used to program the twelfth bit of the Mode Register.
13-18, 63-67	A0-A10	Input	Address Inputs: A0-A10 are sampled during the ACTIVE command (row-address A0-A10) and READ/WRITE command (column-address A0-A7, with A10 defining AUTO PRECHARGE) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if both banks are to be precharged (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
49	SCL	Input	Serial Clock for Presence-Detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
98-100	SA0-SA2	Input	Presence-Detect Address Inputs: These pins are used to configure the presence-detect device.

PIN DESCRIPTIONS (continued)

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
2-5, 7-10, 38-41, 43-46, 52-55, 57-60, 88-91, 93-96	DQ0-DQ31	Input/Output	Data I/Os: Data bus.
48	SDA	Input/Output	Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and data out of the presence-detect portion of the module.
6, 21, 31, 42, 50, 56, 71, 81, 92	V_{DD}	Supply	Power Supply: +3.3V ±0.3V.
1, 12, 26, 36, 47, 51, 62, 76, 86, 97	V_{SS}	Supply	Ground.
23, 24, 74	RFU	–	Reserved for Future Use: These pins should be left unconnected.
22, 78	DNU	–	Do Not Use: These pins are not connected on these modules but are assigned pins on the compatible DRAM version.

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SPD CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figures 1 and 2).

SPD START CONDITION

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD STOP CONDITION

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

SPD ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (Figure 3).

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight-bit word. In the read mode the SPD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.
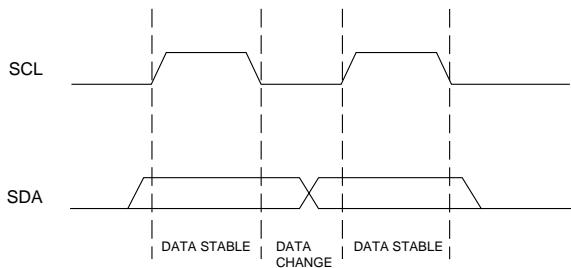
**Figure 1
DATA VALIDITY**
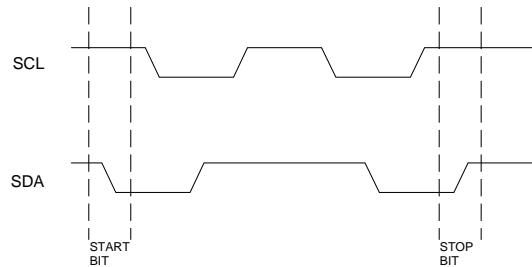
**Figure 2
DEFINITION OF START AND STOP**
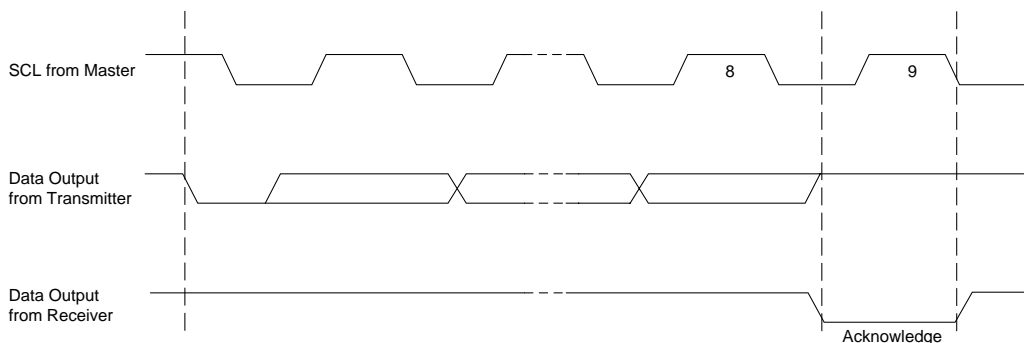
**Figure 3
ACKNOWLEDGE RESPONSE FROM RECEIVER**

SERIAL PRESENCE-DETECT MATRIX

BYTE	DESCRIPTION	ENTRY (VERSION)	SYMBOL	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
0	NUMBER OF BYTES USED BY MICRON	128		1	0	0	0	0	0	0	0	80
1	TOTAL NUMBER OF SPD MEMORY BYTES	256		0	0	0	0	1	0	0	0	08
2	MEMORY TYPE	SDRAM		0	0	0	0	0	1	0	0	04
3	NUMBER OF ROW ADDRESSES	11		0	0	0	0	1	0	1	1	0B
4	NUMBER OF COLUMN ADDRESSES	8		0	0	0	0	1	0	0	0	08
5	NUMBER OF BANKS	1 (4MB)		0	0	0	0	0	0	0	1	01
		2 (8MB)		0	0	0	0	0	0	1	0	02
6	MODULE DATA WIDTH	32		0	0	1	0	0	0	0	0	20
7	MODULE DATA WIDTH (continued)	0		0	0	0	0	0	0	0	0	00
8	MODULE VOLTAGE INTERFACE LEVELS	LVTTL		0	0	0	0	0	0	0	1	01
9	SDRAM CYCLE TIME (CAS LATENCY= 3)	8 (-8)	^{t}CK	1	0	0	0	0	0	0	0	80
		10 (-10)		1	0	1	0	0	0	0	1	A0
10	SDRAM ACCESS FROM CLOCK (CAS LATENCY= 3)	6 (-8)	^{t}AC	0	1	1	0	0	0	0	0	60
		7.5 (-10)		0	1	1	1	0	1	0	1	75
11	MODULE CONFIGURATION TYPE	NONPARITY		0	0	0	0	0	0	0	0	00
12	REFRESH RATE/TYPE	15.6μs/SELF		1	0	0	0	0	0	0	0	80
13	SDRAM WIDTH (PRIMARY SDRAM)	16		0	0	0	1	0	0	0	0	10
14	ERROR-CHECKING SDRAM DATA WIDTH	NONE		0	0	0	0	0	0	0	0	00
15	MIN. CLOCK DELAY FROM BACK-TO-BACK RANDOM COLUMN ADDRESSES	1	^{t}CCD	0	0	0	0	0	0	0	1	01
16	BURST LENGTHS SUPPORTED	1, 2, 4, 8, PAGE		1	0	0	0	1	1	1	1	8F
17	NUMBER OF BANKS ON SDRAM DEVICE	2		0	0	0	0	0	0	1	0	02
18	CAS LATENCIES SUPPORTED	1, 2, 3		0	0	0	0	0	1	1	1	07
19	CS LATENCY	0		0	0	0	0	0	0	0	1	01
20	WE LATENCY	0		0	0	0	0	0	0	0	1	01
21	SDRAM MODULE ATTRIBUTES	UNBUFFERED		0	0	0	0	0	0	0	0	00
22	SDRAM DEVICE ATTRIBUTES: GENERAL	0E		0	0	0	0	1	1	1	0	0E
23	SDRAM CYCLE TIME (CAS LATENCY = 2)	13 (-8)	^{t}CK	1	1	0	1	0	0	0	0	D0
		15 (-10)		1	1	1	1	0	0	0	0	F0
24	SDRAM ACCESS FROM CLK (CAS LATENCY = 2)	9	^{t}AC	1	0	0	1	0	0	0	0	90
25	SDRAM CYCLE TIME (CAS LATENCY = 1)	25 (-8)	^{t}CK	0	1	1	0	0	1	0	0	64
		30 (-10)		0	1	1	1	1	0	0	0	78
26	SDRAM ACCESS FROM CLK (CAS LATENCY = 1)	22 (-8)	^{t}AC	0	1	0	1	1	0	0	0	58
		27 (-10)		0	1	1	0	1	1	0	0	6C
27	MINIMUM ROW PRECHARGE TIME	24 (-8)	^{t}RP	0	0	0	1	1	0	0	0	18
		30 (-10)		0	0	0	1	1	1	1	0	1E
28	MINIMUM ROW ACTIVE TO ROW ACTIVE	16	^{t}RRD	0	0	0	1	0	0	0	0	10
29	MINIMUM RAS# TO CAS# DELAY	24 (-8)	^{t}RCD	0	0	0	1	1	0	0	0	18
		30 (-10)		0	0	0	1	1	1	1	0	1E
30	MINIMUM RAS# PULSE WIDTH	48 (-8)	^{t}RAS	0	0	1	1	0	0	0	0	30
		60 (-10)		0	0	1	1	1	1	0	0	3C
31	MODULE BANK DENSITY	4MB		0	0	0	0	0	0	0	1	01
32	COMMAND/ADDRESS SETUP	2 (-8)	^{t}AS, ^{t}CMS	0	0	1	0	0	0	0	0	20
		3 (-10)		0	0	1	1	0	0	0	0	30

NOTE: 1. "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."

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SERIAL PRESENCE-DETECT (contined)

BYTE	DESCRIPTION	ENTRY (VERSION)	SYMBOL	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
33	COMMAND/ADDRESS HOLD	1	$^tAH, ^tCMH$	0	0	0	1	0	0	0	0	10
34	DATA SIGNAL INPUT SETUP	2 (-8)	^tDS	0	0	1	0	0	0	0	0	20
		3 (-10)		0	0	1	1	0	0	0	0	30
35	DATA SIGNAL INPUT HOLD	1	^tDH	0	0	0	1	0	0	0	0	10
36-61	RESERVED BYTES	–		0	0	0	0	0	0	0	0	00
62	SPD REVISION	REV. 2		0	0	0	0	0	0	1	0	02
63	CHECKSUM FOR BYTES 0-62	4MB (-8)		1	1	0	0	1	0	0	1	C9
		4MB (-10)		0	1	1	1	1	1	1	0	7E
		8MB (-8)		1	1	0	0	1	0	1	0	CA
		8MB (-10)		0	1	1	1	1	1	1	1	7F
64	MANUFACTURER'S JEDEC ID CODE	MICRON		0	0	1	0	1	1	0	0	2C
65-71	MANUFACTURER'S JEDEC CODE (CONT.)			1	1	1	1	1	1	1	1	FF
72	MANUFACTURING LOCATION			0	0	0	0	0	0	0	1	01
				0	0	0	0	0	0	1	0	02
				0	0	0	0	0	0	1	1	03
				0	0	0	0	0	1	0	0	04
				0	0	0	0	0	1	0	1	05
				0	0	0	0	0	1	1	0	06
73-90	MODULE PART NUMBER (ASCII)			x	x	x	x	x	x	x	x	xx
91	PCB IDENTIFICATION CODE	1		0	0	0	0	0	0	0	1	01
		2		0	0	0	0	0	0	1	0	02
		3		0	0	0	0	0	0	1	1	03
		4		0	0	0	0	0	1	0	0	04
92	IDENTIFICATION CODE (CONT.)	0		0	0	0	0	0	0	0	0	00
93	YEAR OF MANUFACTURE IN BCD			x	x	x	x	x	x	x	x	xx
94	WEEK OF MANUFACTURE IN BCD			x	x	x	x	x	x	x	x	xx
95-98	MODULE SERIAL NUMBER			x	x	x	x	x	x	x	x	xx
99-127	MANUFACTURER-SPECIFIC DATA (RSVD)			–	–	–	–	–	–	–	–	–

NOTE: 1. "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."
        2. x = Variable Data.
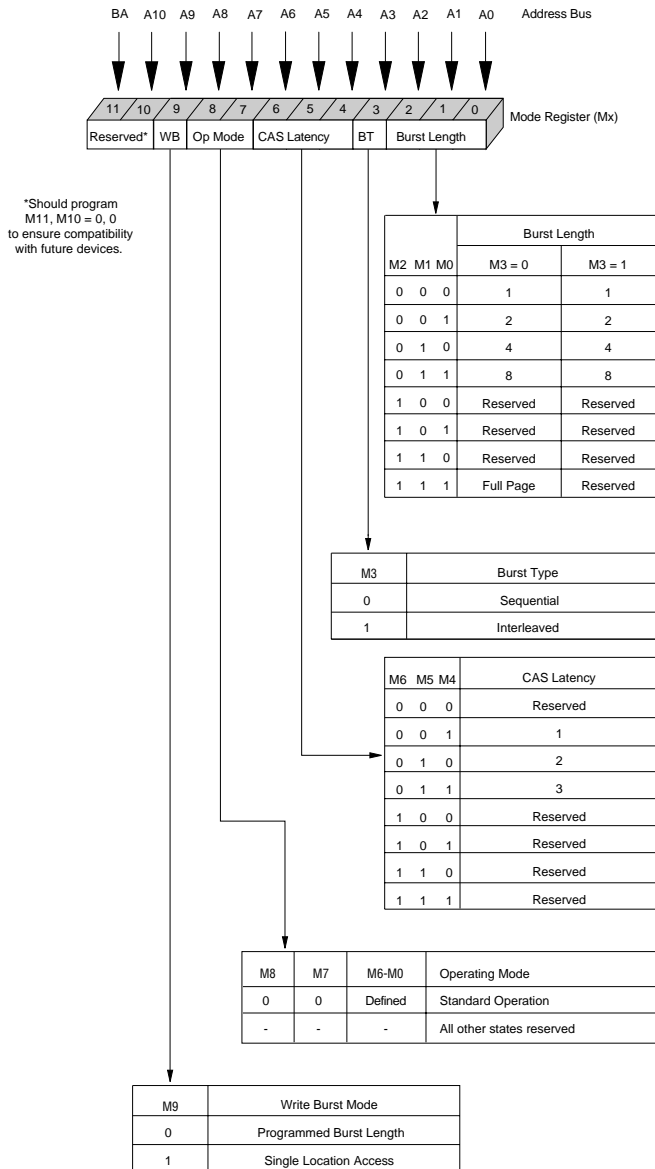
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COMMANDS

Truth Table 1 provides a general reference of available commands. For a more detailed description of commands and operations, refer to the 16Mb: x16 SDRAM data sheet.

TRUTH TABLE 1 – Commands and DQMB Operation

(Notes: 1)

NAME (FUNCTION)	CS#	RAS#	CAS#	WE#	DQMB	ADDR	DQs	NOTES
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (Select bank and activate row)	L	L	H	H	X	Bank/Row	X	3
READ (Select bank and column, and start READ burst)	L	H	L	H	L/H[8]	Bank/Col	X	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	L/H[8]	Bank/Col	Valid	4
BURST TERMINATE	L	H	H	L	X	X	Active	
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	X	X	6, 7
LOAD MODE REGISTER	L	L	L	L	X	Op-Code	X	2
Write Enable/Output Enable	–	–	–	–	L	–	Active	8
Write Inhibit/Output High-Z	–	–	–	–	H	–	High-Z	8

NOTE:
1. CKE is HIGH for all commands shown except SELF REFRESH.
2. A0-A10 and BA0 define the op-code written to the Mode Register.
3. A0-A10 provide row address and BA0 determines which bank is made active (BA0 LOW = Bank 0; BA0 HIGH = Bank 1).
4. A0-A7 provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), while A10 LOW disables the auto precharge feature; BA0 determines which bank is being read from or written to (BA0 LOW = Bank 0; BA0 HIGH = Bank 1).
5. A10 LOW: BA0 determines which bank is being precharged (BA0 LOW = Bank 0; BA0 HIGH = Bank 1). A10 HIGH: both banks are precharged and BA0 is "Don't Care."
6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
8. Activates or deactivates the DQs during WRITEs (zero-clock delay) and READs (two-clock delay).

*Should program
M11, M10 = 0, 0
to ensure compatibility
with future devices.

			Burst Length	
M2	M1	M0	M3 = 0	M3 = 1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Full Page	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

M6	M5	M4	CAS Latency
0	0	0	Reserved
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

M8	M7	M6-M0	Operating Mode
0	0	Defined	Standard Operation
-	-	-	All other states reserved

M9	Write Burst Mode
0	Programmed Burst Length
1	Single Location Access

Figure 1
MODE REGISTER DEFINITION

Table 1
BURST DEFINITION

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
2			A0		
			0	0-1	0-1
			1	1-0	1-0
4		A1	A0		
		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	A2	A1	A0		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (256)	n = A0-A7 (location 0-255)			Cn, Cn + 1, Cn + 2 Cn + 3, Cn + 4... ...Cn - 1, Cn...	Not Supported

NOTE:
1. For a burst length of two, A1-A7 select the block-of-two burst; A0 selects the starting column within the block.
2. For a burst length of four, A2-A7 select the block-of-four burst; A0-A1 select the starting column within the block.
3. For a burst length of eight, A3-A7 select the block-of-eight burst; A0-A2 select the starting column within the block.
4. For a full-page burst, the full row is selected, and A0-A7 select the starting column.
5. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
6. For a burst length of one, A0-A7 select the unique column to be accessed, and Mode Register bit M3 is ignored.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD} Supply Relative to V_{SS} .... -1V to +4.6V
Voltage on Inputs, NC or I/O Pins
   Relative to V_{SS} .... -1V to +4.6V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 4W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1, 6) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE		V_{DD}	3	3.6	V	
INPUT HIGH VOLTAGE: Logic 1; All inputs		V_{IH}	2	V_{DD} + 0.3	V	24
INPUT LOW VOLTAGE: Logic 0; All inputs		V_{IL}	-0.5	0.8	V	24
INPUT LEAKAGE CURRENT:	WE#, RAS#, CAS#, A0-A10, BA0	I_{I1}	-20	20	μA	23
Any input 0V ≤ V_{IN} ≤ V_{DD}	CK0-1, CKE0-1, DQMB0-DQMB3	I_{I2}	-10	10	μA	
(All other pins not under test = 0V)	S0#-S3#	I_{I3}	-5	5	μA	
OUTPUT LEAKAGE CURRENT: DQs are disabled; 0V ≤ V_{OUT} ≤ V_{DD}	DQ0-DQ31	I_{OZ}	-20	20	μA	23
OUTPUT LEVELS: Output High Voltage (I_{OUT} = -4mA)		V_{OH}	2.4	–	V	
Output Low Voltage (I_{OUT} = 4mA)		V_{OL}	–	0.4	V	

I_{DD} SPECIFICATIONS AND CONDITIONS

(Notes: 1, 6, 11, 13) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	SIZE	MAX -8	MAX -10	UNITS	NOTES
OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; ^tRC = ^tRC (MIN); CAS latency = 3	I_{DD1}	4MB	270	260	mA	3, 18, 19, 28
		8MB	340	320		
STANDBY CURRENT: Power-Down Mode; CKE = LOW; All banks idle	I_{DD2}	4MB	4	4	mA	28
		8MB	8	8		
STANDBY CURRENT: Active Mode; S0#-S3# = HIGH; CKE = HIGH; All banks active after ^tRCD met; No accesses in progress	I_{DD3}	4MB	70	60	mA	3, 12, 19, 28
		8MB	140	120		
OPERATING CURRENT: Burst Mode; Continuous burst; READ or WRITE; All banks active; CAS latency = 3	I_{DD4}	4MB	200	160	mA	3, 18, 19, 28
		8MB	270	220		
AUTO REFRESH CURRENT: ^tRC = 15.625μs; CAS latency = 3; S0#-S3# = HIGH; CKE = HIGH	I_{DD5}	4MB	70	60	mA	3, 12, 18, 19, 28
		8MB	140	120		
SELF REFRESH CURRENT: CKE ≤ 0.2V	I_{DD6}	4MB	2	2	mA	4
		8MB	4	4		

CAPACITANCE

PARAMETER	SYMBOL	MAX 4MB	MAX 8MB	UNITS	NOTES
Input Capacitance: A0-A10, BA0, RAS#, CAS#, WE#	C_{I1}	15	25	pF	2
Input Capacitance: S0#-S3#	C_{I2}	8	8	pF	2
Input Capacitance: DQMB0#-DQMB3#	C_{I3}	8	15	pF	2
Input Capacitance: SCL, SA0-SA2	C_{I4}	6	6	pF	2
Input Capacitance: CK0-CK1, CKE0-CKE1	C_{I5}	15	15	pF	2
Input/Output Capacitance: DQ0-DQ31, SDA	C_{IO}	9	16	pF	2

SDRAM COMPONENT* AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 11)

AC CHARACTERISTICS PARAMETER		SYMBOL	-8 MIN	-8 MAX	-10 MIN	-10 MAX	UNITS	NOTES
Access time from CLK (positive edge)	CL = 3	^{t}AC		6		7.5	ns	
	CL = 2	^{t}AC		9		9	ns	24
	CL = 1	^{t}AC		22		27	ns	24
Address hold time		^{t}AH	1		1		ns	
Address setup time		^{t}AS	2		3		ns	
CLK high-level width		^{t}CH	3		3.5		ns	
CLK low-level width		^{t}CL	3		3.5		ns	
Clock cycle time	CL = 3	^{t}CK	8		10		ns	25
	CL = 2	^{t}CK	13		15		ns	24, 25
	CL = 1	^{t}CK	25		30		ns	25
CKE hold time		^{t}CKH	1		1		ns	
CKE setup time		^{t}CKS	2		3		ns	
CS#, RAS#, CAS#, WE#, DQM hold time		^{t}CMH	1		1		ns	
CS#, RAS#, CAS#, WE#, DQM setup time		^{t}CMS	2		3		ns	
Data-in hold time		^{t}DH	1		1		ns	
Data-in setup time		^{t}DS	2		3		ns	
Data-out high-impedance time	CL = 3	^{t}HZ		6		8	ns	10
	CL = 2	^{t}HZ		9		10	ns	10
	CL = 1	^{t}HZ		22		15	ns	10
Data-out low-impedance time		^{t}LZ	1		2		ns	
Data-out hold time		^{t}OH	2.5		3		ns	
ACTIVE to PRECHARGE command period		^{t}RAS	48	120,000	60	120,000	ns	
AUTO REFRESH and ACTIVE to ACTIVE command period		^{t}RC	80		90		ns	24
AUTO REFRESH PERIOD		$^{t}RCAR$	80				ns	
ACTIVE to READ or WRITE delay		^{t}RCD	24		30		ns	24
Refresh period (4,096 cycles)		^{t}REF		64		64	ms	
PRECHARGE command period		^{t}RP	24		30		ns	24
ACTIVE bank A to ACTIVE bank B command period		^{t}RRD	16		20		ns	
Transition time		^{t}T	0.3	10	0.3	10	ns	7
WRITE recovery time		^{t}WR	1 + 2ns		1		^{t}CK	26
			10		10		ns	27
Exit SELF REFRESH to ACTIVE command		^{t}XSR	80		96		ns	20

*Specifications for the SDRAM components used on the module.

AC FUNCTIONAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 11)

PARAMETER		SYMBOL	-8	-10	UNITS	NOTES
READ/WRITE command to READ/WRITE command		^{t}CCD	1	1	^{t}CK	17
CKE to clock disable or power-down entry mode		^{t}CKED	1	1	^{t}CK	14
CKE to clock enable or power-down exit setup mode		^{t}PED	1	1	^{t}CK	14
DQM to input data delay		^{t}DQD	0	0	^{t}CK	17
DQM to data mask during WRITEs		^{t}DQM	0	0	^{t}CK	17
DQM to data high-impedance during READs		^{t}DQZ	2	2	^{t}CK	17
WRITE command to input data delay		^{t}DWD	0	0	^{t}CK	17
Data-in to ACTIVATE command	CL = 3	^{t}DAL	5	4	^{t}CK	15, 21
	CL = 2	^{t}DAL	4	3	^{t}CK	15, 21
	CL = 1	^{t}DAL	3	3	^{t}CK	15, 21
Data-in to precharge		^{t}DPL	2	1	^{t}CK	16
Last data-in to BURST STOP command		^{t}BDL	0	0	^{t}CK	17
Last data-in to new READ/WRITE command		^{t}CDL	1	1	^{t}CK	17
Last data-in to PRECHARGE command		^{t}RDL	1	1	^{t}CK	16, 21
LOAD MODE REGISTER command to ACTIVE or REFRESH command		^{t}MRD	2	2	^{t}CK	28
Data-out to high-impedance from PRECHARGE command	CL = 3	^{t}ROH	3	3	^{t}CK	17
	CL = 2	^{t}ROH	2	2	^{t}CK	17
	CL = 1	^{t}ROH	1	1	^{t}CK	17

SERIAL PRESENCE-DETECT EEPROM DC OPERATING CONDITIONS

(Notes: 1) (V_{DD} = +3.3V ±0.3V)

| PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE	V_{DD}	3	3.6	V	
INPUT HIGH VOLTAGE: Logic 1; All inputs	V_{IH}	$V_{DD} \times 0.7$	$V_{DD} + 0.5$	V	
INPUT LOW VOLTAGE: Logic 0; All inputs	V_{IL}	-1	$V_{DD} \times 0.3$	V	
OUTPUT LOW VOLTAGE: I_{OUT} = 3mA	V_{OL}	–	0.4	V	
INPUT LEAKAGE CURRENT: V_{IN} = GND to V_{DD}	I_{LI}	–	10	µA	
OUTPUT LEAKAGE CURRENT: V_{OUT} = GND to V_{DD}	I_{LO}	–	10	µA	
STANDBY CURRENT: SCL = SDA = V_{DD} - 0.3V; All other inputs = GND or 3.3V +10%	I_{SB}	–	30	µA	
POWER SUPPLY CURRENT: SCL clock frequency = 100 KHz	I_{DD}	–	2	mA	

SERIAL PRESENCE-DETECT EEPROM AC ELECTRICAL CHARACTERISTICS

(Notes: 1) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SCL LOW to SDA data-out valid	^{t}AA	0.3	3.5	µs	
Time the bus must be free before a new transition can start	^{t}BUF	4.7		µs	
Data-out hold time	^{t}DH	300		ns	
SDA and SCL fall time	^{t}F		300	ns	
Data-in hold time	$^{t}HD:DAT$	0		µs	
Start condition hold time	$^{t}HD:STA$	4		µs	
Clock HIGH period	$^{t}HIGH$	4		µs	
Noise suppression time constant at SCL, SDA inputs	^{t}I		100	ns	
Clock LOW period	^{t}LOW	4.7		µs	
SDA and SCL rise time	^{t}R		1	µs	
SCL clock frequency	^{t}SCL		100	KHz	
Data-in setup time	$^{t}SU:DAT$	250		ns	
Start condition setup time	$^{t}SU:STA$	4.7		µs	
Stop condition setup time	$^{t}SU:STO$	4.7		µs	
WRITE cycle time	^{t}WRC		10	ms	22

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{DD} = +3.3V; f = 1MHz.
3. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is ensured.
6. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. The two AUTO REFRESH command wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
7. AC characteristics assume ^{t}T = 1ns.
8. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
9. Outputs measured at 1.5V with equivalent load:

Q ──────┬──────
        ═══ 50pF
        ▽
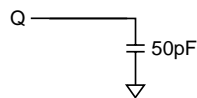
10. ^{t}HZ defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}. The last valid data element will meet ^{t}OH before going High-Z.
11. AC timing tests have V_{IL} = 0V and V_{IH} = 3V, with timing referenced to 1.5V crossover point.
12. Other input signals are allowed to transition no more than once in any two-clock period and are otherwise at valid V_{IH} or V_{IL} levels.
13. I_{DD} specifications are tested after the device is properly initialized.
14. Timing actually specified by ^{t}CKS; clock(s) specified as a reference only at minimum cycle rate.

15. Timing actually specified by ^{t}WR plus ^{t}RP; clock(s) specified as a reference only at minimum cycle rate.
16. Timing actually specified by ^{t}WR.
17. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
18. The I_{DD} current will decrease as the CAS latency is reduced. This is due to the fact that the maximum cycle rate is slower as the CAS latency is reduced.
19. Address transitions average one transition every two-clock period.
20. CLK must be toggled a minimum of two times during this period.
21. Based on ^{t}CK = 125 MHz for -8 and 100 MHz for -10.
22. The SPD EEPROM WRITE cycle time (^{t}WRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to the pull-up resistor, and the EEPROM does not respond to its slave address.
23. 4MB module values will be half of those shown.
24. V_{IH} overshoot: V_{IH} (MAX) = V_{DD} + 2V for a pulse width $\leq$ 3ns, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: V_{IL} (MIN) = -2V for a pulse width $\leq$ 3ns, and the pulse width cannot be greater than one third of the cycle rate.
25. The clock frequency must remain constant during access or precharge states (READ, WRITE, including ^{t}WR, and PRECHARGE commands). CKE may be used to reduce the data rate.
26. Auto precharge mode only.
27. Precharge mode only
28. ^{t}CK = 10ns for -8, 15ns for -10.

SPD EEPROM

☒ UNDEFINED
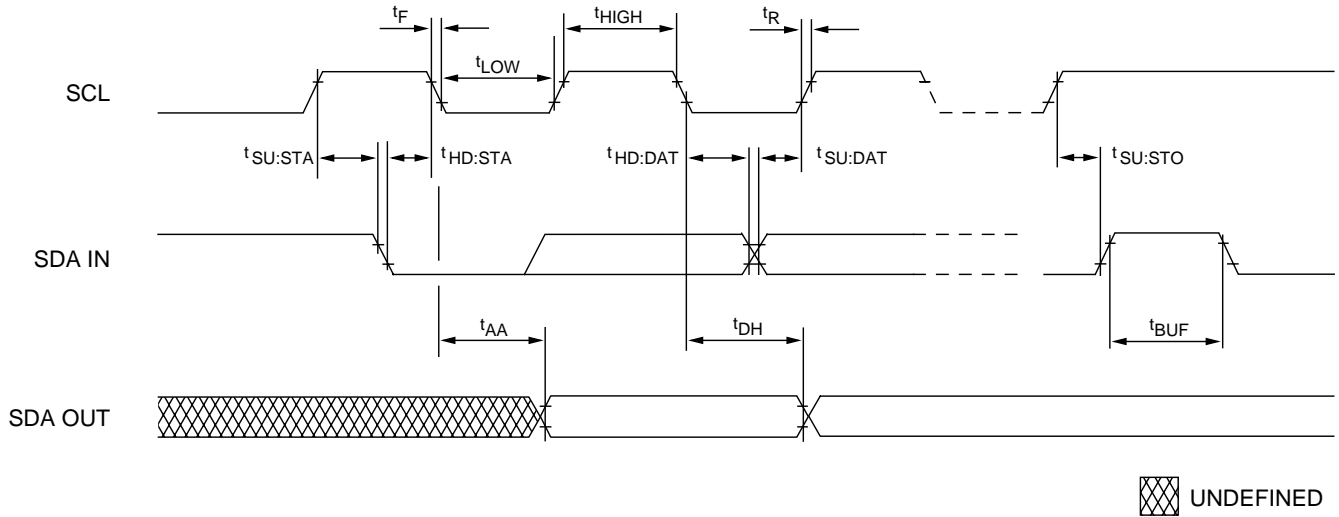
SERIAL PRESENCE-DETECT EEPROM TIMING PARAMETERS

SYMBOL	MIN	MAX	UNITS
^{t}AA	0.3	3.5	μs
^{t}BUF	4.7		μs
^{t}DH	300		ns
^{t}F		300	ns
^{t}HD:DAT	0		μs
^{t}HD:STA	4		μs

SYMBOL	MIN	MAX	UNITS
^{t}HIGH	4		μs
^{t}LOW	4.7		μs
^{t}R		1	μs
^{t}SU:DAT	250		ns
^{t}SU:STA	4.7		μs
^{t}SU:STO	4.7		μs

100-PIN DIMM

H-3

3.557 (90.34) / 3.545 (90.04)

.079 (2.00) R (2X)

.118 (3.00) (2X)

.118 (3.00) TYP

.118 (3.00) TYP

PIN 1

.039 (1.00) R(2X)

.250 (6.35) TYP

.039 (1.00) TYP

.050 (1.27) TYP

.128 (3.25) / .118 (3.00) (2X)

PIN 50

2.850 (72.39)

.700 (17.78) TYP

1.005 (25.53) / 0.995 (25.27)

.125 (3.18) MAX

.054 (1.37) / .046 (1.17)

100-PIN DIMM

H-4

3.557 (90.34) / 3.545 (90.04)

.079 (2.00) R (2X)

.118 (3.00) (2X)

.118 (3.00) TYP

.118 (3.00) TYP

PIN 1

.039 (1.00) R(2X)

.250 (6.35) TYP

.039 (1.00) TYP

.050 (1.27) TYP

.128 (3.25) / .118 (3.00) (2X)

PIN 50

2.850 (72.39)

.700 (17.78) TYP

1.005 (25.53) / 0.995 (25.27)

.157 (4.00) MAX

.054 (1.37) / .046 (1.17)
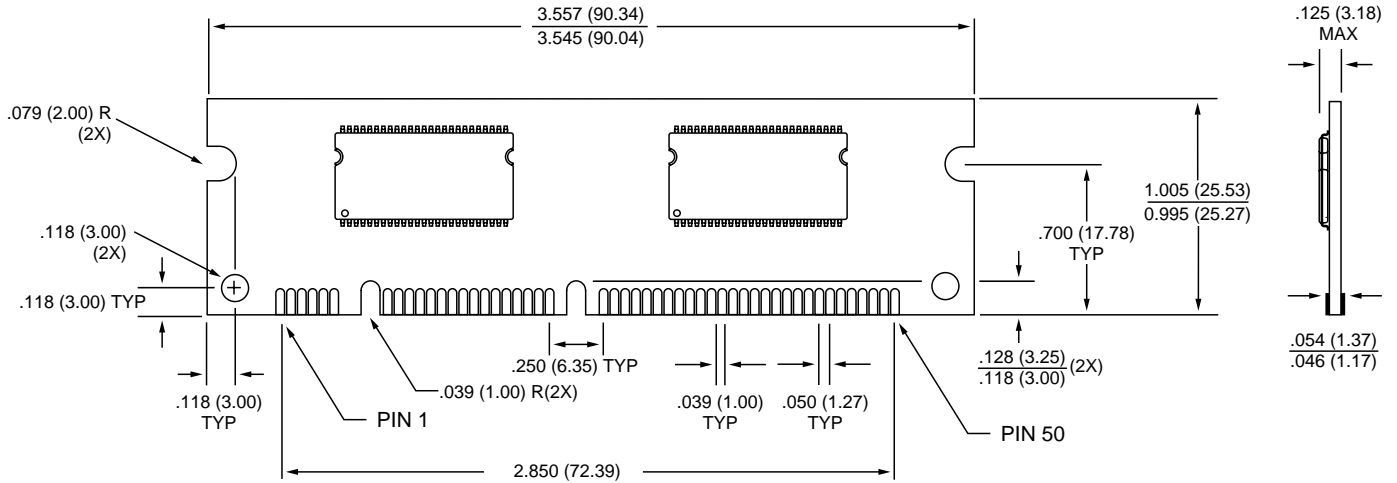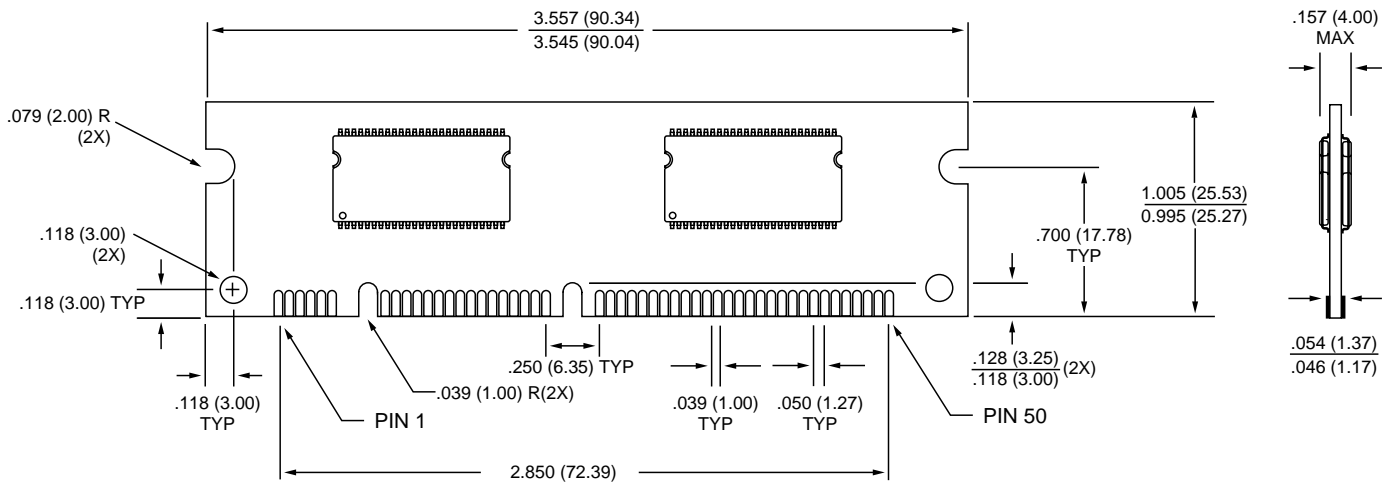
NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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