Supertex inc. HV09

Product Objective Specification

T-52-13-05

32–Channel Symmetric Row Drivers

Ordering Information

Device	Package Options			
	44 J-Lead Quad Ceramic Chip Carrier	44 J-Lead Quad Plastic Chip Carrier	Die in waffle pack	44 - Lead Ceramic J-Bend (MIL-STD-883 Processed*)
HV0923	HV0923DJ	HV0923PJ	HV0923X	RBHV0923DJ

* For Hi-Rel process flows, refer to page 5-3 of the Databook.

Features

- Processed with HVCMOS® technology
- Symmetric row drive (reduces latent imaging in ACTFEL displays)
- Output voltages up to 230V
- Very low-power level shifting
- Source/Sink current 200mA
- Shift Register Speed 4MHz
- Pin-programmable shift direction
- 44-lead plastic & ceramic surface-mount packages

General Description

The HV09 is a low-voltage serial to high-voltage parallel converter with push-pull outputs. It is especially suitable for use as a symmetric row driver in AC thin-film electroluminescent (ACTFEL) displays. The HV09 offers 32 output lines, a direction (DIR) pin to give CW or CCW shift register loading, output enable (OE), and polarity (POL) control. After DATA INPUT is entered (on the falling edge of CLOCK), a logic high will cause the output to swing to V_{PP} if POL is high, or to GND if POL is low.

Absolute Maximum Ratings

Supply voltage, V_{DD}[1]		-0.3V to +15V
Supply voltage, V_{PP}		-0.3V to +250V
Logic input levels		-0.3V to V_{DD} +0.3V
Ground currrent[2]		1.5A
Continuous total power dissipation[3]:	Ceramic	1500mW
	Plastic	1200mW
Storage temperature range		-65°C to +150°C
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds		260°C

Notes:
1. All voltages are referenced to GND.
2. Duty cycle is limited by the total power dissipated in the package.
3. For operation above 25°C ambient, derate linearly to 70°C at 12mW/°C.

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Electrical Characteristics

(over recommended operating conditions of V_{DD} = 12V and V_{PP} = 230V unless noted) T-52-13-05

DC Characteristics

Symbol	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current			10	mA	f_{CLK} = 4MHz
				3	mA	f_{CLK} = 100kHz
I_{PPQ}	High voltage quiescent supply current			4	mA	1 output high[1]
				500	µA	All Outputs low
				500	µA	High Z state
I_{DDQ}	Quiescent V_{DD} supply current			100	µA	All V_{IN} = GND or V_{DD}
V_{OH}	High-level output	HV_{OUT}	200		V	I_O= -200mA
		Data out	11		V	I_O= -500µA
V_{OL}	Low-level output	HV_{OUT}		30	V	I_O= 200mA
		Data out		1	V	I_O= 500µA
I_{IH}	High-level logic input current			1	µA	V_{IH} = 12V
I_{IL}	Low-level logic input current			-1	µA	V_{IL} = 0V
V_{OC}	High voltage output clamp voltage			-2	V	I_O= -200mA

Note 1. The total number of ON outputs times the duty cycle must not exceed the allowable P_D.

AC Characteristics (V_{DD} = 12V, T_C = 25°C)

Symbol	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency		4	MHz	
t_W	Pulse duration clock high or low	125		ns	
t_{SUD}	Data set-up time before falling clock	100		ns	
t_{HD}	Data hold time after falling clock	100		ns	
t_{SUC}	Setup time clock low before V_{PP}↑ or GND↓	300		ns	
t_{SUE}	Setup time enable high before V_{PP}↑ or GND↓	300		ns	
t_{SUP}	Setup time polarity high or low before V_{PP}↑ or GND↓	300		ns	
t_{HC}	Hold time clock high after V_{PP}↑ or GND↓	500		ns	
t_{HE}	Hold time enable high after V_{PP}↑ or GND↓	300		ns	
t_{HP}	Hold time polarity high or low after V_{PP}↑ or GND↓	300		ns	
t_{DHL}	Delay time high to low level output from clock		150	ns	C_L = 30pF
t_{DLH}	Delay time low to high level output from clock		200	ns	C_L = 30pF
t_{THL}	Transition time high to low level serial output		200	ns	C_L = 30pF
t_{TLH}	Transition time low to high level serial output		100	ns	C_L = 30pF
t_{ONH}	High level turn-on time HV outputs from enable		1000	ns	I_O = -200 mA, V_{OH} =220V R_L = 500 Ω to 120V
t_{ONL}	Low level turn-on time HV outputs from enable		500	ns	I_O = 200 mA, V_{OH} =130V R_L = 500 Ω to 30V
t_{OFFH}	High level turn-off time HV outputs from enable		1000	ns	I_O = -200 mA, V_{OH} =220V R_L = 500 Ω to 120V
t_{OFFL}	Low level turn-off time HV outputs from enable		500	ns	I_O = 200 mA, V_{OH} =130V R_L = 500 Ω to 30V
	Slew rate, V_{PP} or GND		45	V/µs	With one active output driving a 4.7 nF load to V_{PP} or GND

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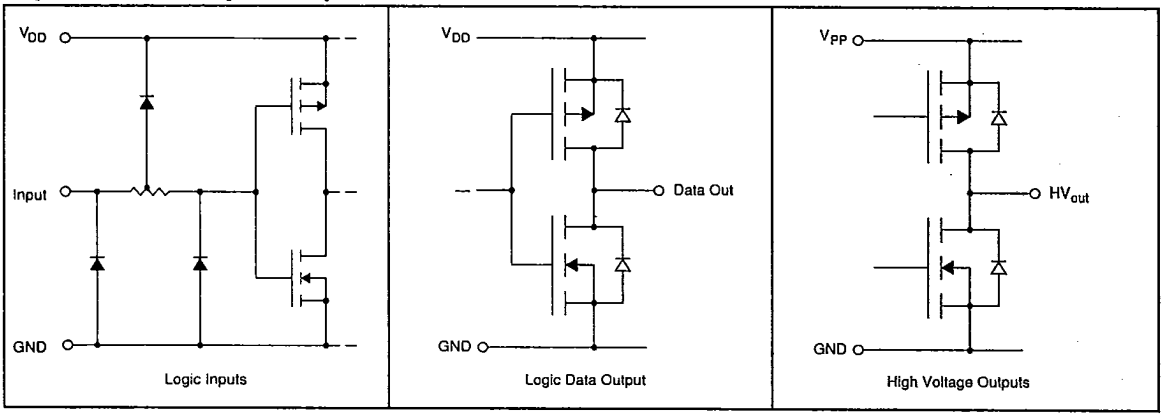
Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{DD}	Logic supply voltage		10.8	13.2	V
V_{PP}	High voltage supply			230	V
V_{IH}	High-level input voltage	V_{DD} = 10.8V	8.1		V
		V_{DD} = 13.2V	9.9		
V_{IL}	Low-level input voltage	V_{DD} = 10.8V		2.7	V
		V_{DD} = 13.2V		3.3	
f_{CLK}	Clock frequency			4	MHz
T_A	Operating free-air temperature	Commercial	0	+70	°C
		Military Hi-Rel (RB)	-55	+125	°C

Note:
Power-up sequence should be the following:
1. Connect ground.
2. Apply V_{DD}.
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply V_{PP}.

Power-down sequence should be the reverse of the above.

Input and Output Equivalent Circuits



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Switching Waveforms

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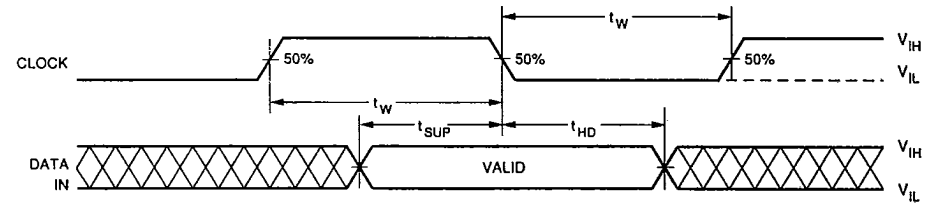
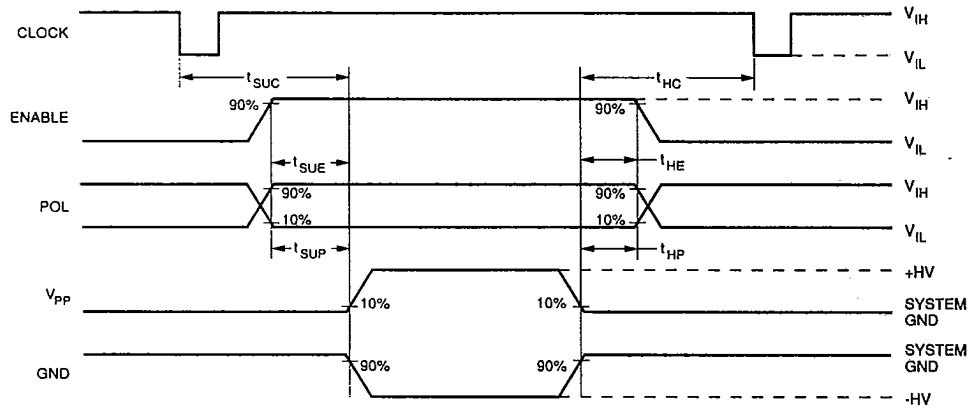
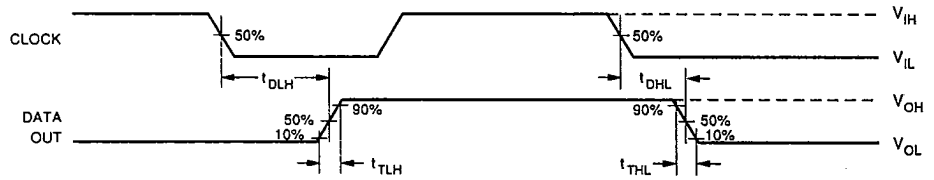


Input Timing Voltage



Control Input Timing Voltage



Voltage Waveforms for Propagation Delay Times, Clock to Data Out

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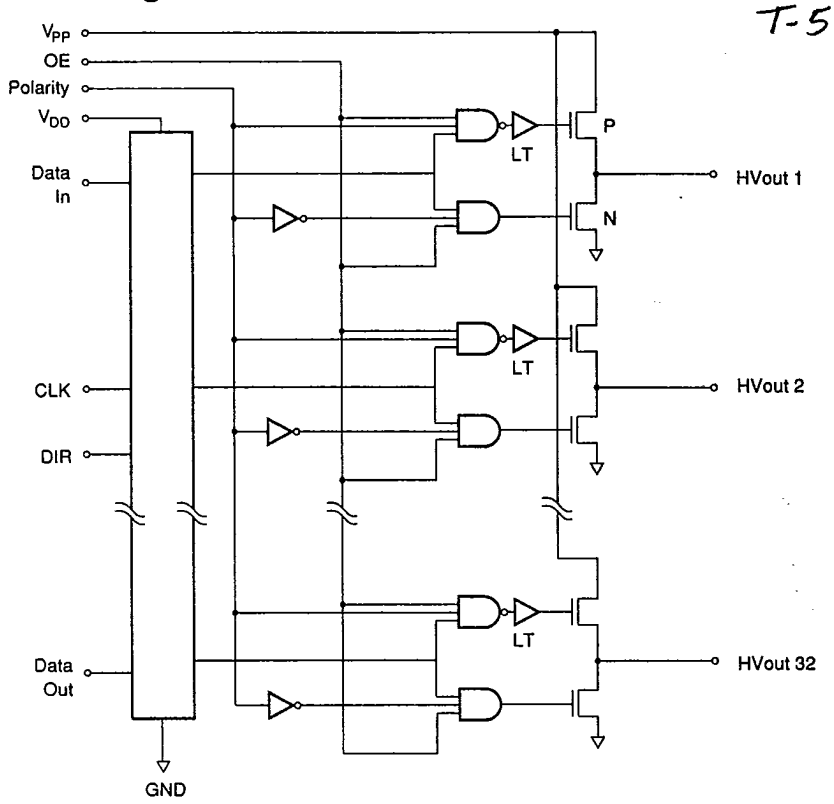
Functional Block Diagram



LT = Level Translator

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Function Table

Outputs	Inputs					Outputs		
	CLK	DIR	Data	POL	OE	Shift Reg	HV Outputs	Data Out
O/P HIGH	X	X	H	H	H	*	H	
O/P OFF	X	X	L	H	H	*	HIGH-Z	*
O/P LOW	X	X	H	L	H	*	L	*
O/P OFF	X	X	L	L	H	*	HIGH-Z	*
All O/P OFF	X	X	X	X	L	*	All O/P HIGH-Z	*
Load S/R, set DIR	↓	L	X	X	X	$Q_n \rightarrow Q_{n+1}$	*	Q_{32}
	↓	H	X	X	X	$Q_n \rightarrow Q_{n-1}$	*	Q_1
I/O Relation	—	L	D_{IO} A	X	X	—	—	D_{IO} B
	—	H	D_{IO} B			—	—	D_{IO} A

Notes:
H = logic high level, L = logic low level, X = irrelevant, Ø = high-to-low transition.
$Q_1 = HV_{out}$ 1, $Q_n = HV_{out}$ (n), etc.
* = dependent on previous state and whether an O/P or S/R command occured.

Pin Configurations

HV09
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HV_{OUT} 16/17	23	DIR
2	HV_{OUT} 15/18	24	V_{DD}
3	HV_{OUT} 14/19	25	Polarity
4	HV_{OUT} 13/20	26	Data I/O B
5	HV_{OUT} 12/21	27	GND
6	HV_{OUT} 11/22	28	V_{PP}
7	HV_{OUT} 10/23	29	HV_{OUT} 32/1
8	HV_{OUT} 9/24	30	HV_{OUT} 31/2
9	HV_{OUT} 8/25	31	HV_{OUT} 30/3
10	HV_{OUT} 7/26	32	HV_{OUT} 29/4
11	HV_{OUT} 6/27	33	HV_{OUT} 28/5
12	HV_{OUT} 5/28	34	HV_{OUT} 27/6
13	HV_{OUT} 4/29	35	HV_{OUT} 26/7
14	HV_{OUT} 3/30	36	HV_{OUT} 25/8
15	HV_{OUT} 2/31	37	HV_{OUT} 24/9
16	HV_{OUT} 1/32	38	HV_{OUT} 23/10
17	V_{PP}	39	HV_{OUT} 22/11
18	GND	40	HV_{OUT} 21/12
19	Data I/O A	41	HV_{OUT} 20/13
20	Output Enable	42	HV_{OUT} 19/14
21	Clock	43	HV_{OUT} 18/15
22	GND	44	HV_{OUT} 17/16

Note:
Pin designation for DIR = L/H
For DIR = H, Pin 1 is HV_{OUT} 16, for DIR = L Pin 1 is HV_{OUT} 17

Package Outline

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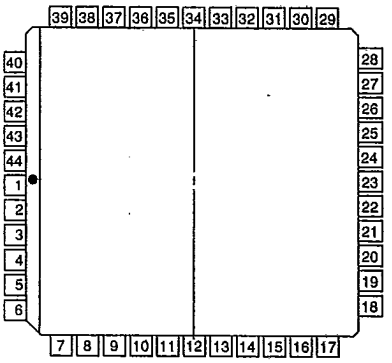

top view

44-pin J-lead Package