LOGICAL SOLUTIONS TECHNOLOGY INCORPORATED

SMT Testability Chip Set Description and Specifications

Description

The LSTI SMT Testability Chip Set is a combination of semiconductor devices that can be designed into a printed circuit board to create a "testability system" that drastically reduces test programming, test fixturing, test equipment, testing and troubleshooting costs of surface mount technology (SMT) printed circuit board designs.

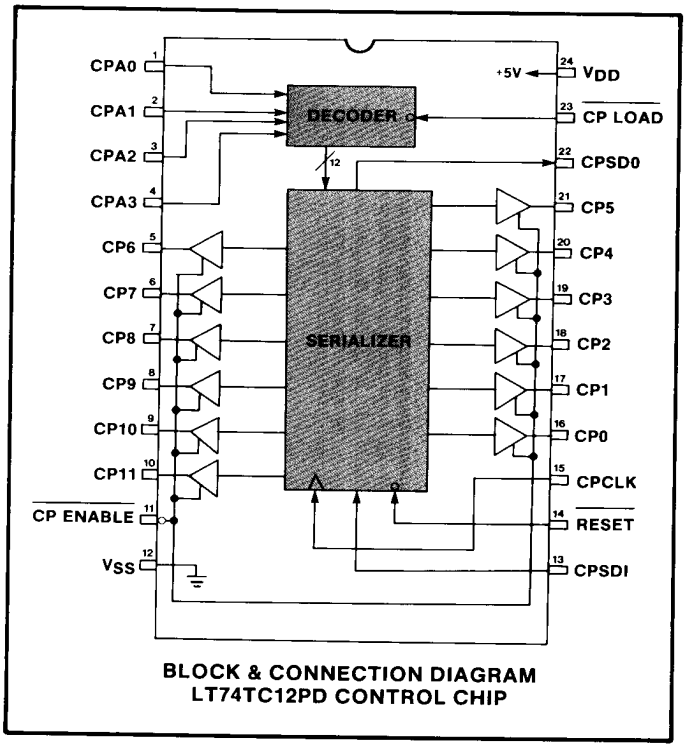
Made up of two devices, a controllability circuit and a visibility circuit that can be "mixed and matched," the chip set is available in many sizes, packages, and configurations for each specific application.

System Features

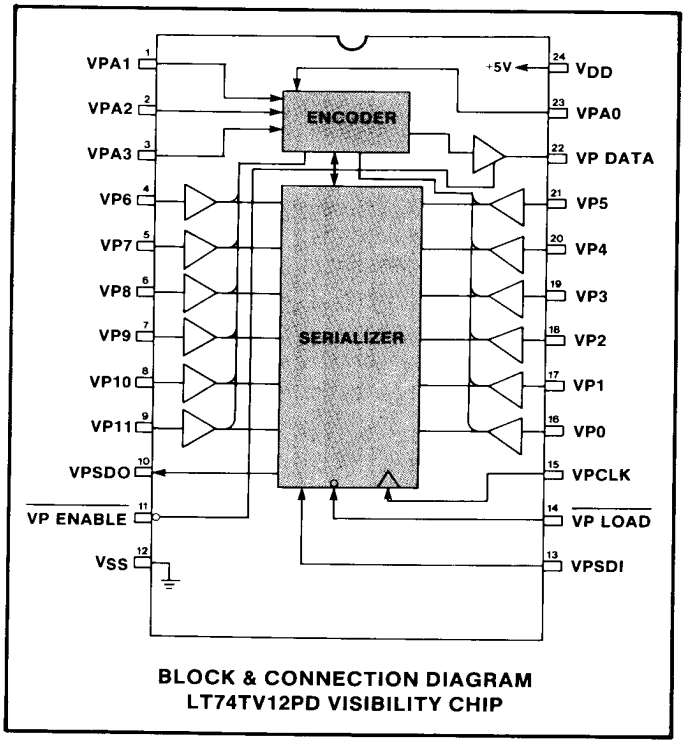
The LSTI SMT Testability Chip Set system is a powerful tool for rendering SMT printed circuit boards testable. System features include:

- Provides controllability and observability functions on both combinatorial and sequential functional logic circuits
- Provides control and visibility without affecting normal circuit logic functions and with minimal impact on initial circuit design
- Applicability to both synchronous and asynchronous functional logic circuits
- Combination serial and parallel controllability functions via tristate-able output drivers
- Combination serial and parallel visibility functions via unit load input receivers
- Expandability in either parallel or serial modes (or both), including a tristate-able Visibility Point Data output which may be "wire-ored" or multiplexed

The chip set facilitates the implementation of a standard "testability bus" that can be used at both board and final product levels. Each chip utilizes the minimum number of extra circuit elements (gates) required to perform the function. Testability devices may be used to implement and enhance stand alone testing, high speed board testing using slow automatic test equipment, or real time on-line monitoring as a section of built in test equipment.



BLOCK & CONNECTION DIAGRAM
LT74TC12PD CONTROL CHIP



BLOCK & CONNECTION DIAGRAM
LT74TV12PD VISIBILITY CHIP

Individual Device Features

The devices are fabricated with a high performance complimentary metal oxide semiconductor (CMOS) process. Device features include:

- Function and pinout compatibility to low power Schottky logic.
- TTL and CMOS compatible input/output logic levels that interface directly with standard TTL logic levels.
- Very low quiescent power dissipation.
- High noise immunity.
- Full input protection to both power and ground sources.
- Symmetric current drive.
- Full buffering on all outputs.

LSTI SMT Testability Chip Set devices are available for both industrial ("74" series) and military ("54" series) applications. Output current sink and drive capability is guaranteed over -40°C to +85°C for "74" series devices and -55°C to +125°C for "54" series devices.

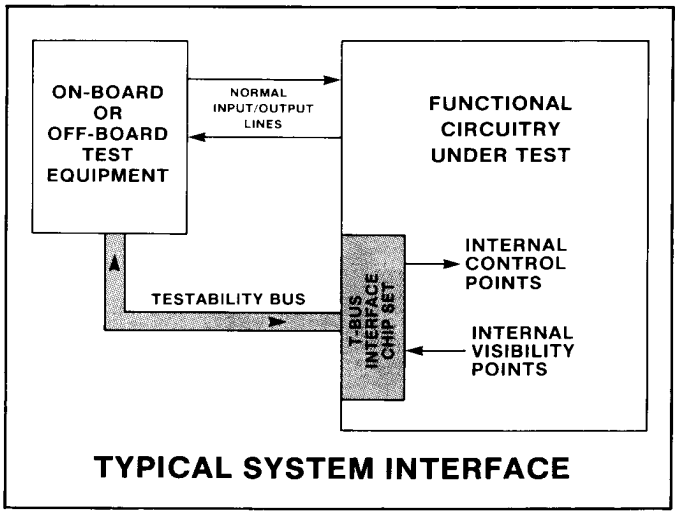
Built-In Testability

The LSTI Testability Chip Set is a specific circuit architecture that builds in enhanced testability characteristics for the functional circuitry when applied at the printed circuit board assembly or electronic system level.

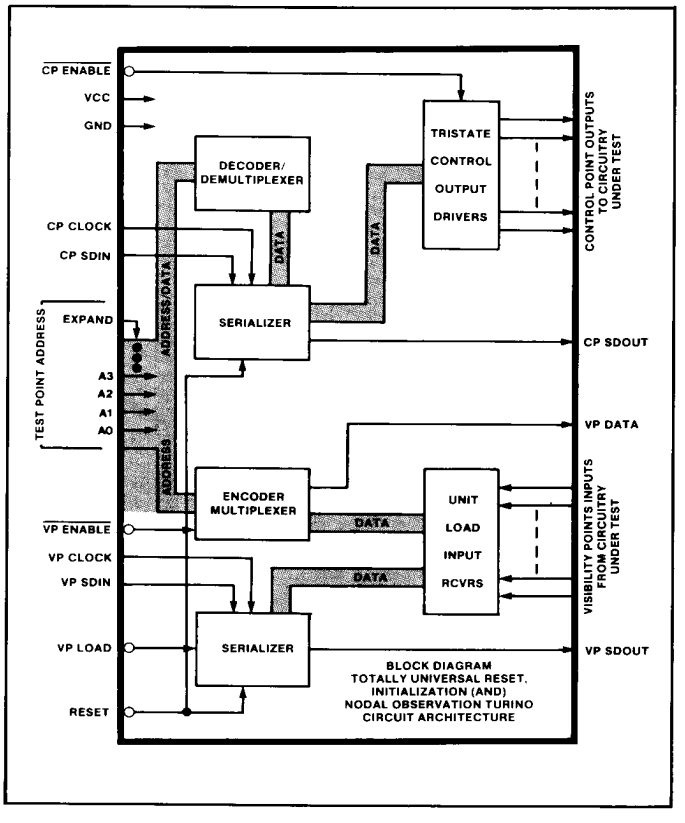
The chip set allows controllability of any or all of the inputs to circuit elements in the functional circuitry, and concurrent observability of existing or resulting logic states at the outputs of that functional circuitry.

The LSTI Chip Set allows serial data based test equipment to evaluate parallel logic states within the functional combinatorial and sequential circuitry efficiently. It also allows parallel data based test equipment and techniques to be used in place of, or in conjunction with, the serial data input/output techniques required by other testability enhancement architectures and circuits.

The LSTI Testability Chip Set transparently provides input data to and obtains output data from the functional circuitry.



TYPICAL SYSTEM INTERFACE



LT74TC12PD Controllability Circuit Functions

The five basic modes in which the controllability circuit operates are the disconnect mode, the initialize mode, the parallel mode, the serial mode and the test mode. The operation of each mode is described below.

Disconnect Mode

The disconnect mode is activated by applying a logic 1 (or open circuit) to the Control Point Enable (CPEN*) line (pin 11). When CPEN* is high, all control point outputs are in the high impedance state and do not affect the circuit nodes to which they are connected (except for a slight leakage current to VDD).

The nine testability bus inputs (CPSDI, CPLD*, CPA0-CPA3, CPEN*, CPCLK and RESET*) have built-in pull-ups of approximately 250KΩ so that the chip is in the disconnect state when these inputs are left open.

Initialize Mode

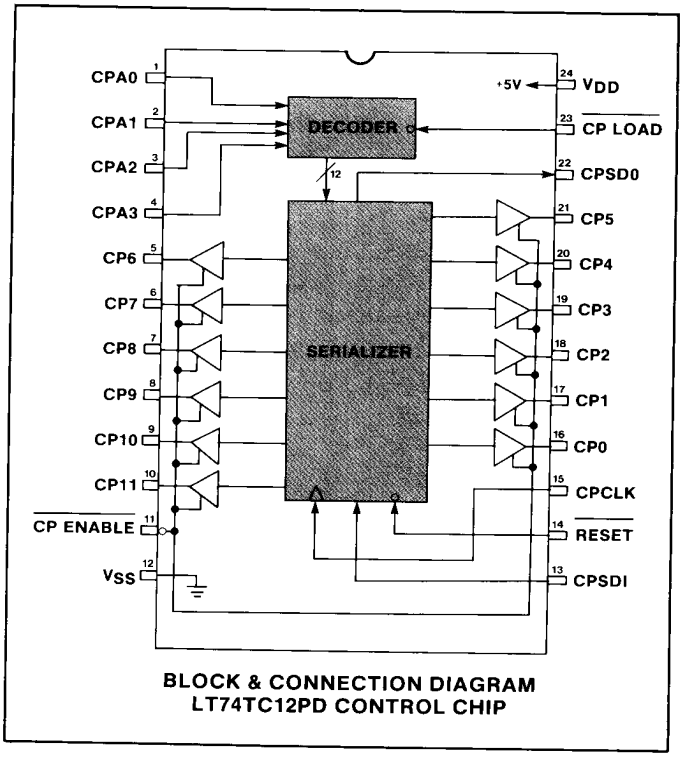
The circuit is initialized by applying a logic 0 to the RESET* line (pin 14). When initialized, the serializer contains all logic 0s. The RESET* line must be in the logic 1 state for the chip to operate in any mode other than the initialize mode.

The initial logic 0s resulting from applying a logic 0 on the RESET* input can be directly applied to the control point outputs (CP0-CP11). This is done by applying a logic 0 to the Control Point Enable (CPEN*) line (pin 11). This action enables the circuit's output drivers. When CPEN* is in the logic 1 state, no data is output on CP0-CP11 and the pins are in a high impedance state.

The CPEN* line should be left at logic 1 state during parallel or serial loading of the circuit except in two instances: if it is desirable either to apply control point output data directly to the circuit inputs to which the LT74TC12PD is connected (parallel mode), or to let data "ripple through" CP0-CP11 while data is being clocked into (serial mode) the serializer.

Parallel Mode

Data is latched into the serializer (for application to the device outputs via the tri-state drivers) by addressing the desired control point (CP0-CP11) via the Control Point Address lines (CPA0-CPA3) and activating the Control Point Load (CPLD*) line (pin 23) with a logic 0 (and then returning to a logic 1 value). This leaves a logic 1 at the selected control point. Normal operation is to initialize all control point outputs to the logic 0 state via the RESET* input. Then each control point can be brought to a logic 1 level as desired.



BLOCK & CONNECTION DIAGRAM
LT74TC12PD CONTROL CHIP

Control point addresses are as follows:

CPA3	CPA2	CPA1	CPA0	Control Point Addressed
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	x	x	(No Control Point Address)

The parallel mode takes precedence over the serial mode and should be used separately from, not in conjunction with, the serial mode.

LT74TC12PD/LT74TV12PD Testability Chip Set

Serial Mode

Data is clocked into the serializer via the Control Point Serial Data Input (CPSDI) line (pin 13) and the Control Point Clock (CPCLK) line (pin 15).

CP0 is the first cell loaded in the serializer and CP11 is the last cell loaded. Data presented at the CPSDI input will be accepted by the serializer when the CPCLK line changes from a logic 0 state to a logic 1 state (rising edge clock).

After 12 clock cycles, the data first presented at CPSDI will be stored in the serializer cell controlling CP11. The last data presented will be stored in the cell controlling CP0.

Examples (all after initial states set to logic 0 with RESET*):

	CONTROL POINT											
Input Data: (CPSDI) 001	0	1	2	3	4	5	6	7	8	9	10	11
Clock Cycles: 3	0	0	1	0	0	0	0	0	0	0	0	0

	CONTROL POINT											
Input Data: 1001001	0	1	2	3	4	5	6	7	8	9	10	11
Clock Cycles: 7	1	0	0	1	0	0	1	0	0	0	0	0

* **Note:** CPSDO logic state is always equal to CP11 logic state.

	CONTROL POINT											
Input Data: 101001001001	0	1	2	3	4	5	6	7	8	9	10	11
Clock Cycles: 12	1	0	1	0	0	1	0	0	1	0	0	1

	CONTROL POINT											
Input Data: 111111111111	0	1	2	3	4	5	6	7	8	9	10	11
Clock Cycles: 12	1	1	1	1	1	1	1	1	1	1	1	1

When more than one controllability chip is used, the Control Point Serial Data Output (CPSD0) line (pin 22) on the first device is connected to the CPSDI input on the second device. Thus for two 12 pin devices connected in series, 24 clocks would be needed to clock a logic 1 into CP23 (which is actually CP11 of the second device).

Test Mode

The CPSD0 line can be used to verify the internal functions of the decoder and serializer. Data (loaded either serially or in the parallel mode) can be clocked out of the device using CPCLK. The first data bit output is CP10; the eleventh data bit output is CP0.

Clock Cycles: 11 1 0 1 0 0 1 0 0 1 0 0 1 CP11 Data (present before clocking)
CP0 Data (Last Bit Out) — CP10 Data (First Bit Out)

LT74TV12PD Visibility Circuit Functions

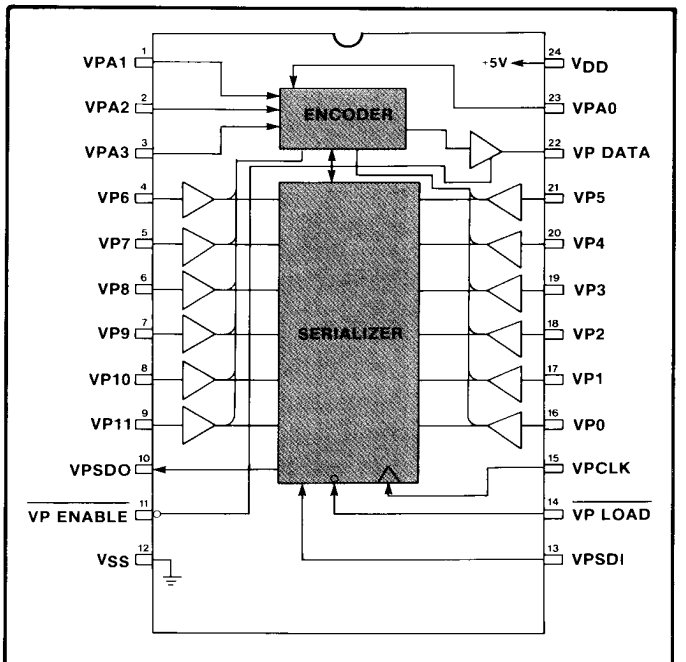
The five basic modes the visibility circuit operates in are the tri-state mode, the initialize mode, the parallel mode, the serial mode and the test mode. The operation of each mode is described below.

Tri-State Mode

The tri-state mode is activated by applying a logic 1 to the Visibility Point Enable (VPEN*) line (pin 11). When VPEN* is high, the Visibility Point Data (VP-DATA) output (pin 22) is in the high impedance state and does not output data. This allows one or more additional visibility circuits to have their VPDATA outputs "wire-ored" together (although use of a multiple input AND gate for multiple VPDATA outputs is preferred).

The VPEN* line must be in the logic 0 state when the device is to operate in the parallel mode.

The eight testability bus inputs (VPA0-VPA3, VPEN*, VPLD* and VPCLK) have built-in pullups of approximately 250KΩ so that the chip is in the tri-state mode when the inputs are left open.



BLOCK & CONNECTION DIAGRAM
LT74TV12PD VISIBILITY CHIP

Initialize Mode

The circuit is initialized by applying all logic 1 signals to the Visibility Point Address (VPA0-VPA3) inputs and a logic 0 to the VPLD* input. Internal gates decode this condition and force the serializer into a known state (all logic 0). The input address to the device must be between 0 and 11 for the device to operate in any mode other than the initialize mode.

Parallel Mode

Data is transferred from the selected visibility point input to the VPDATA output by addressing the desired visibility point (VP0-VP11) via the Visibility Point Address lines (VPA0-VPA3) and activating the VPEN* line with a logic 0. The VPDATA output will follow the VP0-VP11 signal currently addressed.

Visibility Point addresses are as follows:

VPA3	VPA2	VPA1	VPA0	Visibility Point Addressed
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	x	x	(No Visibility Point Address)

The visibility circuit can operate in the parallel mode and the serial mode at the same time. This permits real time monitoring of a selected visibility point and concurrent latching of all visibility point data into the serializer at a specific point in time for later evaluation in the serial mode.

Serial Mode

Data is loaded into the serializer via the Visibility Point Load (VPLOAD*) line (pin 14). A logic 0 on VPLOAD* will capture, in parallel, the current input states of VP0 through VP11. The captured states may then be shifted out to the Visibility Point Serial Data Output (VPSD0) line (pin 10) via the Visibility Point Clock (VPCLK) line (pin 15).

Visibility data is loaded into the serializer in parallel and clocked out of the serializer in sequence. VP11 is the first data bit that is at the VPSD0 output and VP0 is the twelfth data bit that is present at the VPSD0 output (after 11 clock pulses). Data will be clocked out of the serializer when the VPCLK* line changes from a logic 0 state to a logic 1 state (rising edge clock).

After 12 clock cycles, any data present at the Visibility Point Serial Data Input (VPSDI) line (pin 13) on the first clock transistion will be stored in the serializer cell corresponding to VP11, and any data present at the input on the twelfth clock cycle will be stored in the cell corresponding to VP0.

Examples: all after initial states set to logic 0 with VPA0-VPA3 = 1 and VPSDI input at logic 1 — pulled up or no connection (internal pull-up):

VISIBILITY POINT STATES

0	1	2	3	4	5	6	7	8	9	10	11	
0	1	0	0	1	0	0	1	0	0	1	0	At VPLOAD* Time Output Data: 010
1	1	1	0	1	0	0	1	0	0	1	0	After 3 Clock Cycles

VISIBILITY POINT STATES

0	1	2	3	4	5	6	7	8	9	10	11	
0	1	0	0	1	0	0	1	0	0	1	0	At VPLOAD* Time Output Data: 0010010
1	1	1	1	1	1	1	0	1	0	1	1	After 7 Clock Cycles

VISIBILITY POINT STATES

0	1	2	3	4	5	6	7	8	9	10	11	
0	1	0	0	1	0	0	1	0	0	1	0	At VPLOAD* Time Output Data: 010010010010
1	1	1	1	1	1	1	1	1	1	1	1	After 12 Clock Cycles

VISIBILITY POINT STATES

0	1	2	3	4	5	6	7	8	9	10	11	
0	0	0	0	0	0	0	0	0	0	0	0	At VPLOAD* Time Output Data: 000000000000
1	1	1	1	1	1	1	1	1	1	1	1	After 12 Clock Cycles

When more than one visibility chip is used, the Visibility Point Serial Data Output (VPSDO) line (pin 10) on the first device is connected to the VPSDI input on the second device. For two 12 pin devices connected in series, 23 clocks are needed to output serial data from VP0 while the data from VP23 (which is actually VP11 on the second devices) would be present at the VPSD0 output directly prior to clocking.

Test Mode

The VPSDI line can verify the internal functions of the serializer. Data can be clocked into and out of the device using VPCLK. The input buffer functions can be tested by applying parallel data to the device, activating VPLOAD*, and then clocking the latched data out the VPSDO line. The first data bit output is VP10; the eleventh data bit output is VP0.

Clock Cycles: 11 1 0 1 0 0 1 0 0 1 0 0 1 VP11 Data (present before clocking)
VP0 Data (Last Bit Out)
VP10 Data (First Bit Out)

POWER DISSIPATION

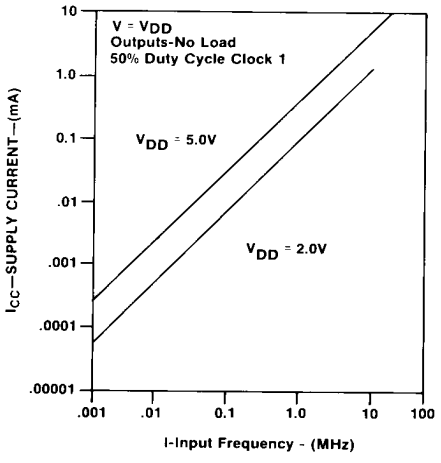


Figure 1. Supply Current vs Input Frequency LT74

INPUT CONFIGURATION

The LT54/74C series logic devices, designed in silicon gate CMOS technology, accept CMOS logic input levels and have the capability to drive both CMOS and bipolar devices. The LT54/74C family brings the designer the advantages of CMOS, namely, low quiescent power dissipation, wide power supply range, flexible interfacing and high noise immunity with speed, drive and pinout compatibility to the LT54/74HC family. This application data provides device characterization and emphasizes the interfacing ability featured in Logical Solutions Technology devices. Logical Solutions Technology also offers the LT54/74T devices designed to accept TTL logic levels.

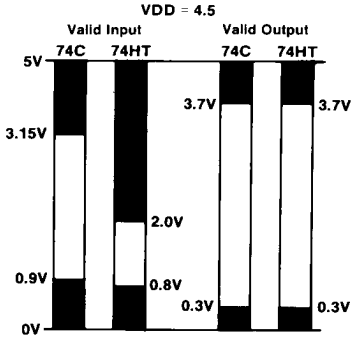


Figure 2. Interface Levels

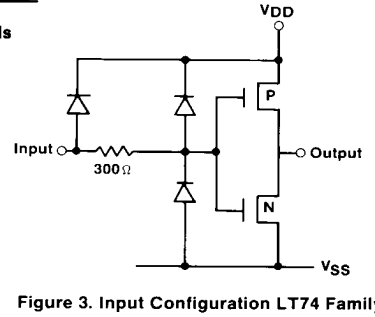


Figure 3. Input Configuration LT74 Family

OUTPUT CONFIGURATION

The outputs of the LT54/74 Series have symmetric drive characteristics. A feature of the LT54/74 series is a high 4mA minimum drive over the operating temperature range. Typical characteristics are shown in Figures 5 and 6.

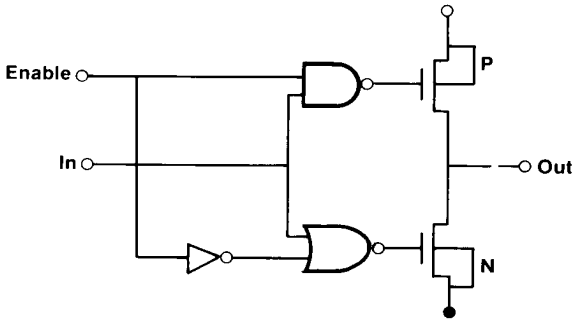


Figure 4. 3-State Output Configuration

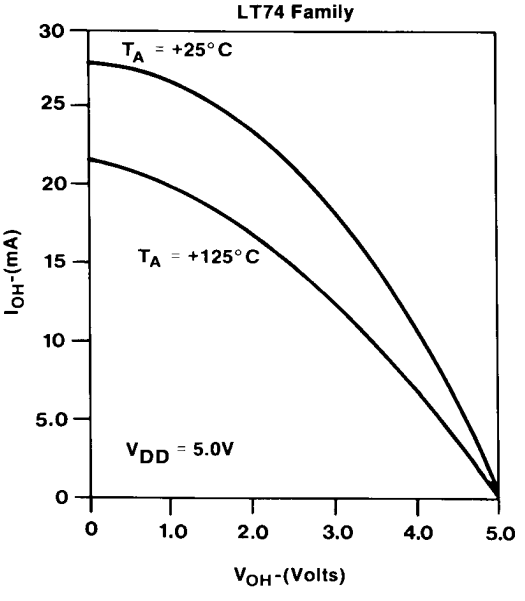


Figure 5. Output High Characteristics

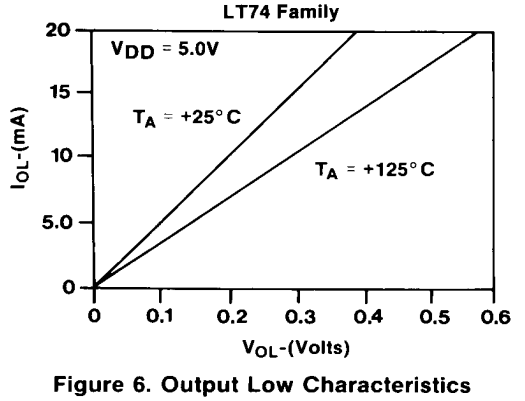


Figure 6. Output Low Characteristics

AC CHARACTERISTICS

The propagation delays of the LT74 series are comparable to LS74 logic. Figures 7 and 8 show the test waveforms used for propagation delay characterization. Maximum rise and fall times and propagation delays are functions of the process technology and package. Consult factory for further information.

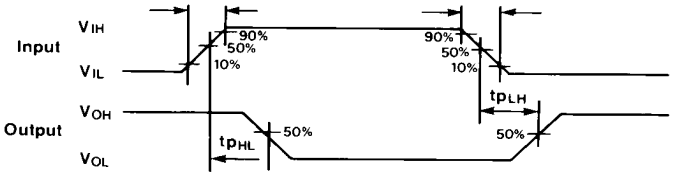


Figure 7. AC Waveforms

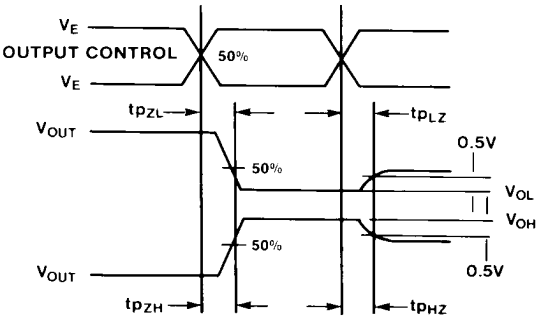


Figure 8. Voltage Waveforms Enable and Disable Times, 3-State Outputs

DC Characteristics (Ambient temperature 25°C, nominal supply voltages)

Parameter	Symbol	Test Conditions	VDD = 5.0V			VDD = 10V			Unit
			Min	Typ	Max	Min	Typ	Max	
Quiescent Power Speed Power Product	PDDQ S-PPDD	VI = VSS or VDD Operating inputs		1 1			12 2		nW/gate pJ/gate
Low Level Output Voltage	VOL	IOL≤1 µA IOL = -3.2mA		 0.22	0.05 0.40		 0.22	0.05 0.40	Volts
High Level Output Voltage	VOH	IOH≤1 µA IOH = 0.6mA	4.95 4.60			9.95 9.2			
Low Level Input Voltage	VII	TTL Input CMOS Input			0.8 1.5			 3.0	
High Level Input Voltage	VIH	TTL Input CMOS Input	2.0 3.5			 7.0			
Input Leakage Current	IIN	VI = VSS or VDD			±0.1			±1.0	µA
Three-State Output Leakage Current	IOZ	VO = VSS or VDD		±0.001	±1.0			±1.0	µA
Input Capacitance	CIN	Any Input		5.0			5.0		pF

All devices contain diodes to protect inputs against damage due to high static voltages or electrical fields; however, it is advised that precautions be taken not to exceed the maximum recommended input voltages. All unused inputs must be connected to an appropriate logic voltage level (either VDD or GND).

- 4mA standard outputs, 6mA bus drivers

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Limits	Unit
DC Supply Voltage[7]	VDD	+3 to +10	V
Operating & Ambient Temp. Range			
Commercial	TA	0 to 70	°C
Industrial	TA	-40 to 85	°C
Military	TA	-55 to 125	°C

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Limits	Unit
DC Supply Voltage	VDD	-0.5 to +12	V
Voltage on Any Pin	VI/O	-0.5 to VDD +0.5	V
DC Input Current	II	±10	mA
Storage Temp. (Ceramic)	TSTG	-65 to 125	°C
Storage Temp. (Plastic)	TSTG	-40 to 125	°C

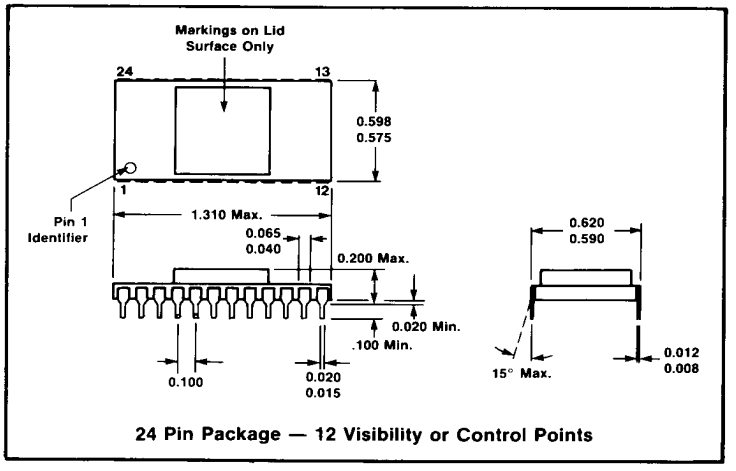
SMT Testability Chip Set Description and Specifications

Device Configuration Options

Configuration options of the LSTI Testability Chip Set are available as follows:

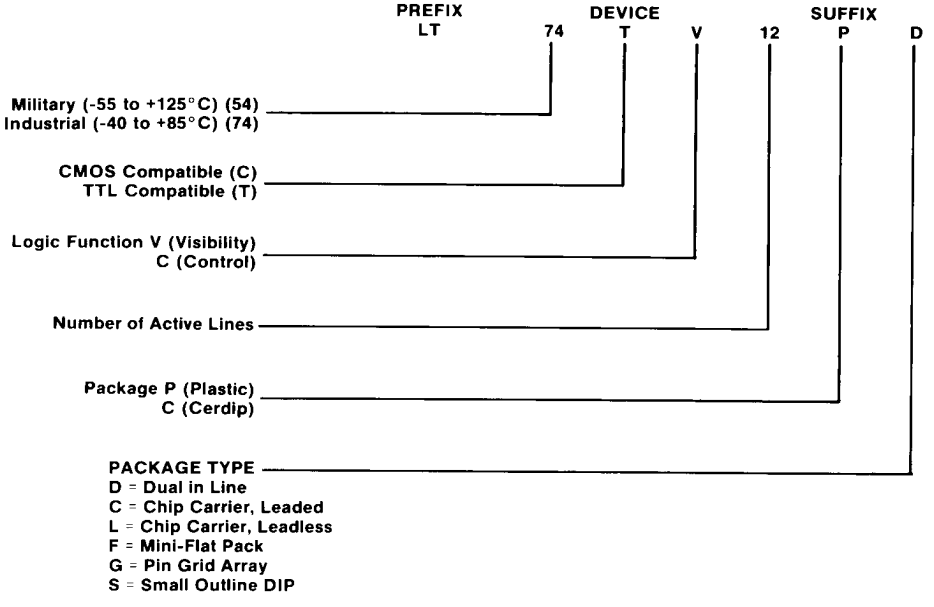
1. Operating temperature ranges: industrial (-40° to 85°C) and military (-55° to 125°C).
2. Logic level compatability: CMOS and TTL.
3. Number of active lines in either the control or visibility chip: 12, 16, 32, or 64.
4. Package material: plastic and cerdip.
5. Package type: Dual in line, leaded and leadless chip carrier, flat pack, and pin grid array.

These options are identified in the LSTI Testability Chip Set Part Numbering System.



24 Pin Package — 12 Visibility or Control Points

Testability Chip Set Part Numbering System



For more information on the economics, applications and package configurations available, order the complete LSTI SMT Testability Chip Set and Implementation Guide (data sheet available on request).

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