Product Description

The CL-FP6131 is an 11-channel buffer amplifier that provides a **single-chip solution** to the reference voltage requirements of the CL-FP6xxx signal driver architecture.

The CL-FP6131 supports 9 or 11 reference voltage systems. For 9 reference applications, the 2 unused amplifiers may be disabled to reduce power dissipation.

11-Channel Buffer Amplifier

Applications

SVGA Reference Buffer for CL-FP6830, CL-FP6530, and CL-FP6532

XGA Reference Buffer for CL-FP6840, CL-FP6540, and CL-FP6534
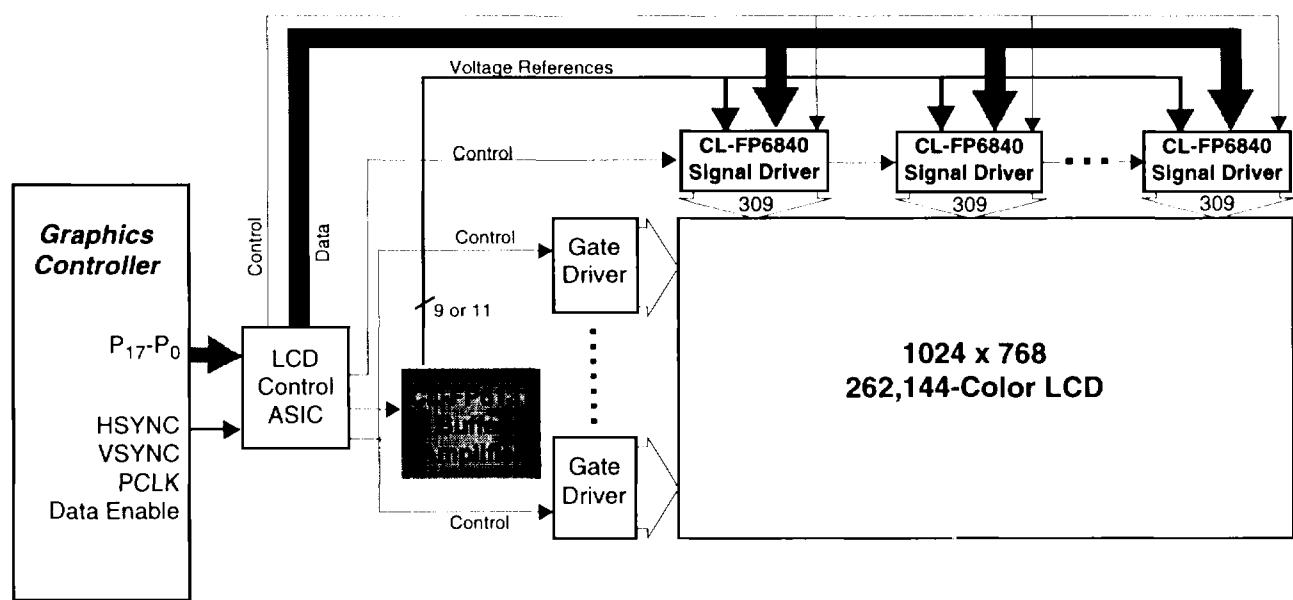
1. Features

Features	Benefits
• **High Integration**	• 11 high drive reference voltage outputs • Internal multiplexors allow polarity-dependent reference values to be selected via A/B_SEL input
• **Low Power Operation**	• Analog supply voltage: 3.3 V ± 0.3 V to 5.0 V ± 0.5 V • Low supply headroom allows wide output dynamic range and minimizes power dissipation • Low quiescent current of less than 0.5 mA per reference output (typical) • EN_11 pin (internally pulled-down) disables OUT_1 & OUT_11 amplifiers to reduce power dissipation in 9 reference amplifier applications. May be set to logic high to enable OUT_1 & OUT_11.
• **High Performance Amplifiers**	• Typical slew rate of 2V/μs with 0.24 μF load • Typically settles to within 50 mV of final value in 6μs with 0.24 μF load
• **Drives Large Load Capacitance**	• Maintains stable operation with load capacitance of 100 pF to 0.24 μF
• **Die Size: 2.25 x 4.5 mm**	• Small die size for chip-on-board applications
• **48-pin TSSOP Package**	• TSSOP package reduces cost and board space.

2. 48 Pin TSSOP Package Dimensions (dimensions in millimeters)

12.5 +/- 0.1
-A-

48   25

8.1

6.1 +/- 0.1
-B-

4.05

1   24

| △ | 0.2 | C | B | A |

ALL LEAD TIPS

| △ | 0.1 | C |

ALL LEAD TIPS

-C-

0.5 TYP   0.17 - 0.27 TYP

(0.90)

1.1 MAX

0.10 ± 0.05 TYP

SEE DETAIL A

0.09 - 0.20 TYP

DETAIL A

GAGE PLANE

0.25

0°-8°

0.60 +0.15 -0.10

SEATING PLANE

FIGURE 2-1

3
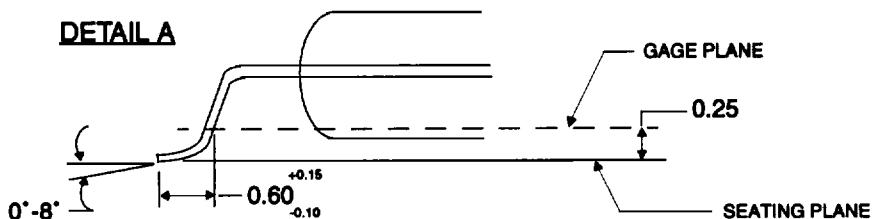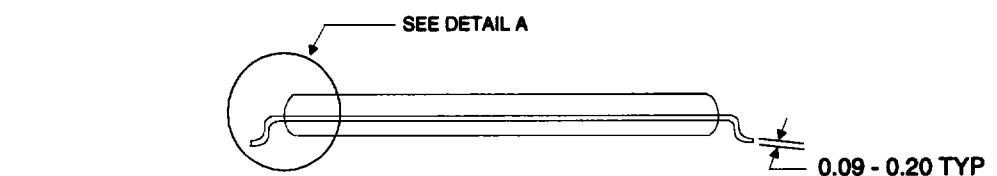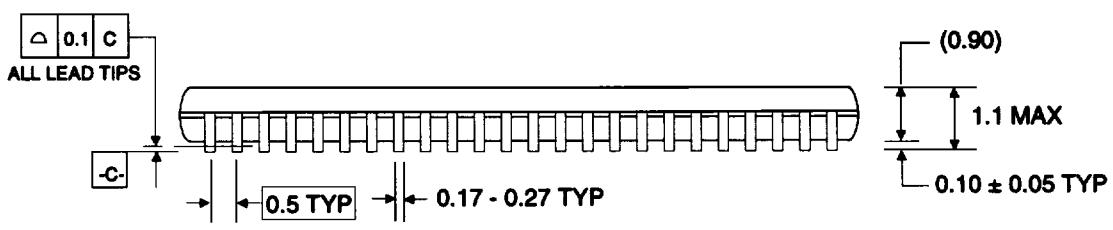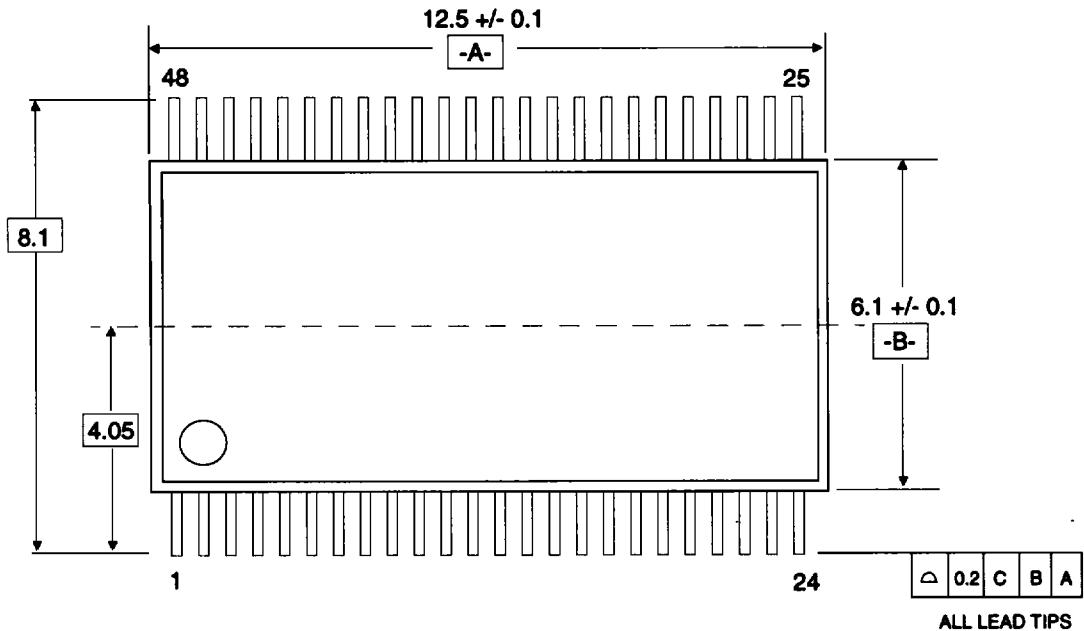
2.1. Die Size and Die Pad Coordinates
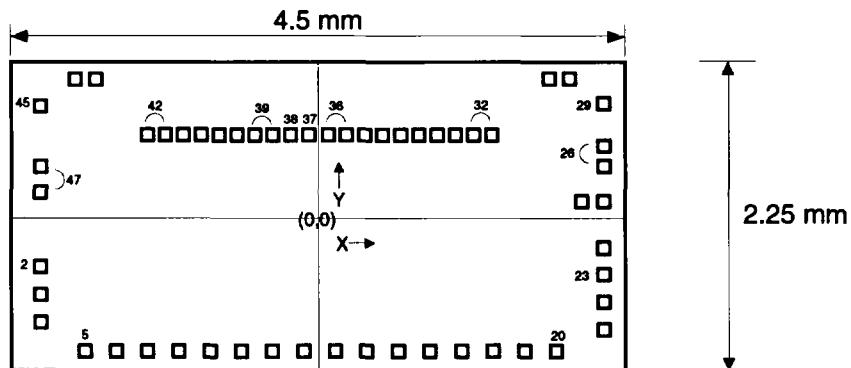

Figure 2-2: FP6131 Die Diagram

Pad	Signal	X	Y
2	I1_A	-2072.7	-365.9
3	I1_B	-2072.7	-563.7
4	I2_A	-2072.7	-763.7
5	I2_B	-1764.9	-904.2
6	I3_A	-1513.1	-904.2
7	I3_B	-1269.8	-904.2
8	I4_A	-1062.8	-904.2
9	I4_B	-846.2	-904.2
10	I5_A	-631.1	-904.2
11	I5_B	-372.6	-904.2
12	I6_A	-122.8	-904.2
13	I6_B	127.2	-904.2
14	I7_A	377.0	-904.2
15	I7_B	635.5	-904.2
16	I8_A	850.6	-904.2
17	I8_B	1067.2	-904.2
18	I9_A	1274.2	-904.2
19	I9_B	1517.5	-904.2
20	I10_A	1769.3	-904.2
21	I10_B	2072.7	-763.7
22	I11_A	2072.7	-563.7
23	I11_B	2072.7	-365.9
26.1	OUT11	2069.0	250.8
26.2	OUT11	2069.0	377.8
29	A/B_SEL	2069.0	647.5
30	V_{DDA}	1873.0	926.5
31	GND	1736.0	926.5

Table 2-1: Die Pad Coordinates

Pad	Signal	X	. Y
32.1	OUT10	1323.9	562.8
32.2	OUT10	1196.9	562.8
33.1	OUT9	1046.3	562.8
33.2	OUT9	919.3	562.8
34.1	OUT8	768.7	562.8
34.2	OUT8	641.7	562.8
35.1	OUT7	491.1	562.8
35.2	OUT7	364.1	562.8
36.1	OUT6	213.5	562.8
36.2	OUT6	86.5	562.8
37	GND	-70.3	562.8
38	V_{DDA}	-207.3	562.8
39.1	OUT5	-364.1	562.8
39.2	OUT5	-491.1	562.8
40.1	OUT4	-641.7	562.8
40.2	OUT4	-768.7	562.8
41.1	OUT3	-919.3	562.8
41.2	OUT3	-1046.3	562.8
42.1	OUT2	-1196.9	562.8
42.2	OUT2	-1323.9	562.8
43	GND	-1736.0	926.5
44	V_{DDA}	-1873.0	926.5
45	EN_11	-2069.0	647.5
47.1	OUT1	-2069.0	377.8
47.2	OUT1	-2069.0	250.8

Table 2-1: Die Pad Coordinates

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3. Function & Pin Information

Table 3–1   Mux Function

A/B_SEL	OUT_x
logic low	Ix_B
logic high	Ix_A

Table 3–2   EN_11 Function

EN_11	Outputs Enabled
logic low or n.c.	OUT_2..OUT_10
logic high	OUT_1..OUT_11

FIGURE 3-1

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CIRRUS LOGIC
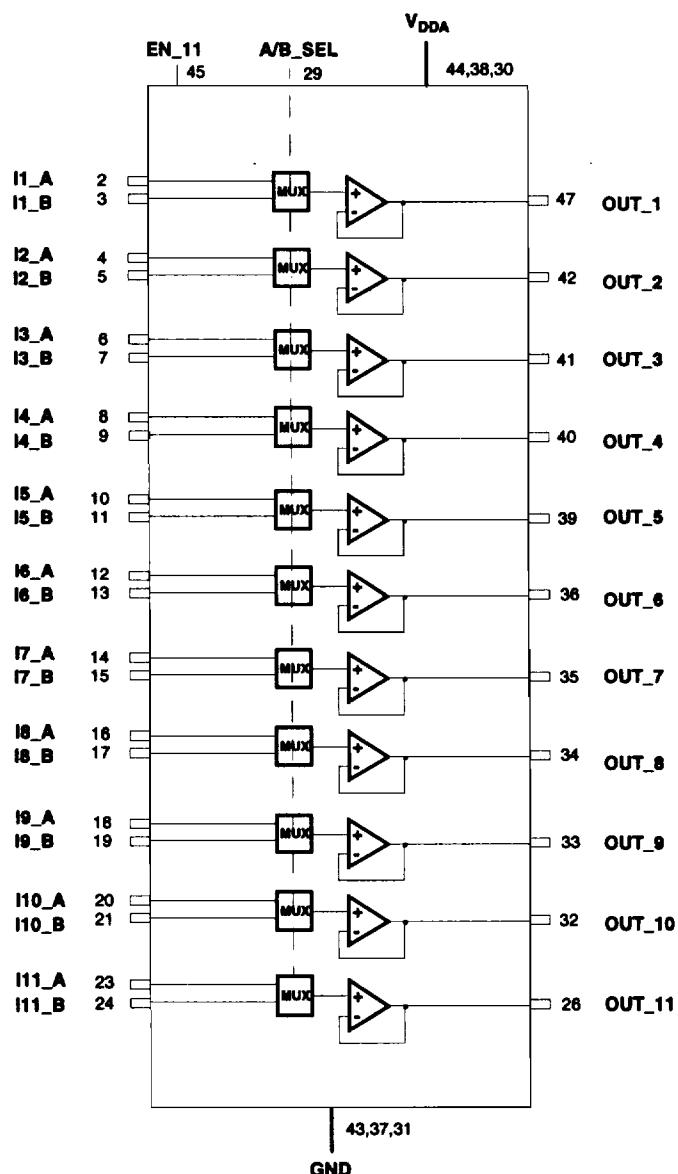
## 3.1. Application Information
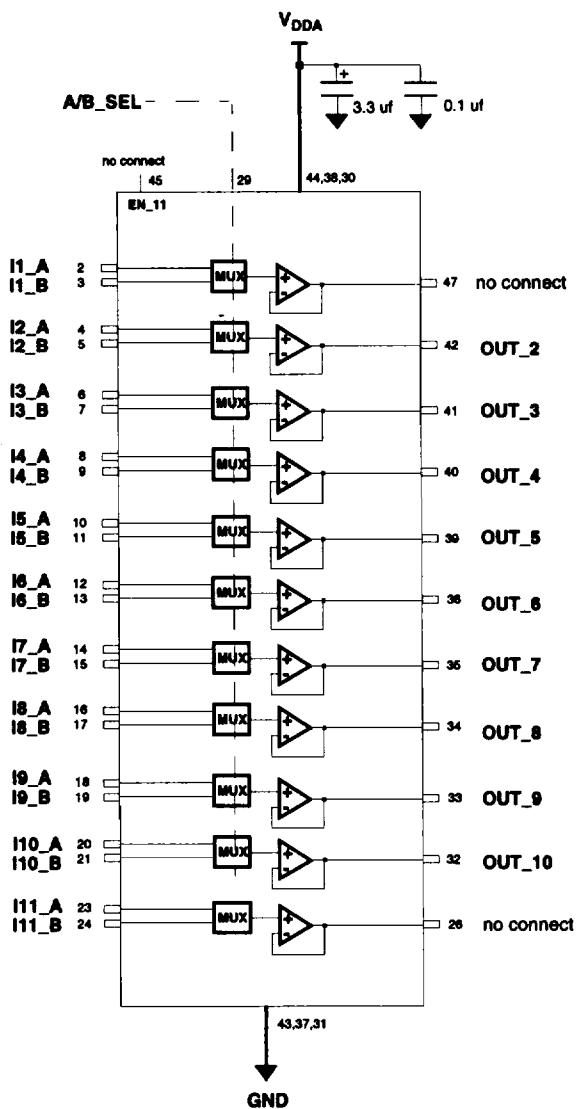
FIGURE 3-2: 9 References
(OUT_1 & OUT_11 disabled)
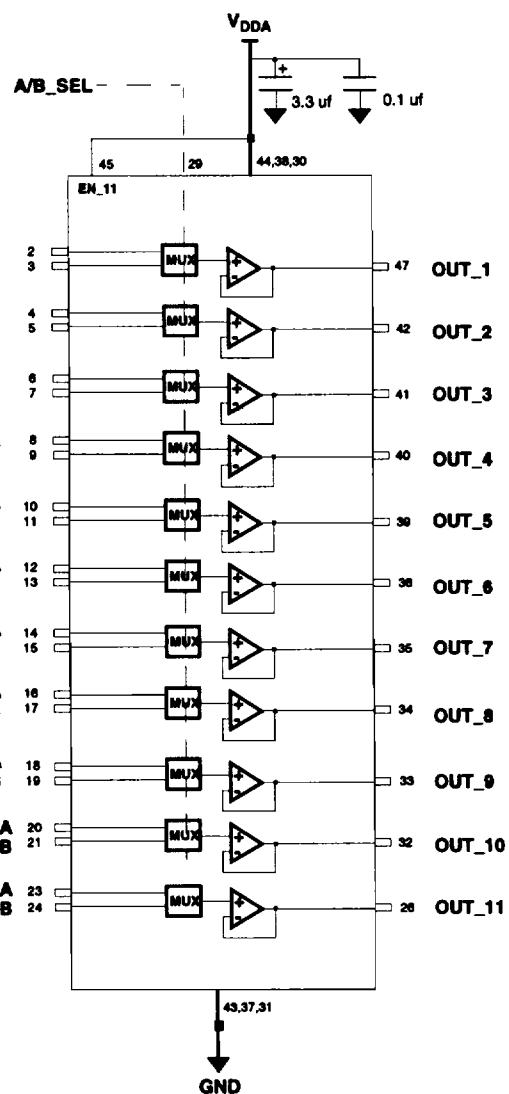
FIGURE 3-3: 11 References

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4. Specifications

4.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Notes
VIN	Input Voltage	-0.3	$V_{DDA} + 0.3$	Volts	1
V_{DDA}	Supply Voltage	-0.3	6.0	Volts	1
I_L	Injection Current	-100	100	mA	
T_J	Junction Temperature		150	°C	
T_A	Operating temperature	-20	85	°C	2
T_{STG}	Storage temperature	-30	85	°C	

Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

NOTES: 1) Voltages are with respect to ground (GND).
2) Ambient temperature under bias.

4.2 Recommended Operating Conditions (Preliminary data – subject to change)

Symbol	Parameter	Min	Typical	Max	Units	Notes
V_{DDA}	Analog supply voltage	3.0		5.5	Volts	1
T_A	Ambient air temperature	0	25	70	°C	
C_L	Output load capacitance			0.3	µF	

NOTES: 1) Voltages are with respect to GND.

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4.3. DC Characteristics (Preliminary data – subject to change)

$V_{DDA} = 5.0$ V, $T_A = 25°$ C.
All voltages are with respect to GND.

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions	Note
A_V	Large Signal Gain	0.985	1.0	1.015	V/V	Fig. 4-1	1
V_{IO}	Input Offset Voltage			20	mV	Fig. 4-1	1
V_{O1}	Output Voltage Range	0.2		4.8	V	Fig. 4-1	2
I_{SC}	Output Short Circuit Current	0.5			A	Fig. 4-3	3
I_{VDDA}	Analog Power Supply Current		5	9	mA	EN_11 high	
V_{IH}	Input Logic High	3.6			V		4
V_{IL}	Input logic low			0.8	V		4
I_{IN}	Input Leakage Current	-5.0		5.0	μA	$0 < V_{IN} < V_{DDA}$	5
I_{EN_11}	Input Current on EN_11 (high)			50	μA	$V_{IN} = V_{DDA}$	6

NOTES:
1) R_L = open and V_x = 0.0 V; R_S = 2 Ω; C_L = 0.24 uf, OUT_n = 2.5V
2) -75 mA < I_{OUTDC} < 75 mA. Applies to OUT_1 .. OUT_11
3) OUT_n = 2.5V.
4) Applies to A/B_SEL and EN_11 input pins
5) Applies to all input pins except EN_11 in high state
6) Applies to EN_11 pin when V_{IN} on EN_11 pin = V_{DDA}

4.4. AC Characteristics (Preliminary data – subject to change)

$V_{DDA} = 5.0$ V, $T_A = 25°$ C.
All voltages are with respect to GND.

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions	Note
T_{SET}	Settling Time			8.0	μsec	Fig. 4-2	1
SR+,SR-	Pos. & Neg. Slew Rate	0.8			V/μsec	Fig. 4-2	1,2

NOTES:
1) R_L/R_S< 5, -75 mA < I_{OUTDC} < 75 mA. C_L = 0.24 μF.
   Measured for a 4.4V step settling to within 50 mV of final value.
   Applies to OUT_1 .. OUT_11
2) Slew rate measured between 20% and 80% points of step.

4.5. DC Characteristics (Preliminary data – subject to change)

$V_{DDA} = 3.3$ V, $T_A = 25°$ C.
All voltages are with respect to GND.

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions	Note
A_V	Large Signal Gain	0.975	1.0	1.025	V/V	Fig. 4-1	1
V_{IO}	Input Offset Voltage			30	mV	Fig. 4-1	1
V_{01}	Output Voltage	0.2		3.1	V	Fig. 4-1	2
I_{SC}	Output Short Circuit Current	0.33			A	Fig. 4-3	3
I_{VDDA}	Analog Power Supply Current		4	8	mA	EN_11 high	
V_{IH}	Input Logic High	2.0			V		4
V_{IL}	Input logic low			0.8	V		4
I_{IN}	Input Leakage Current	-5.0		5.0	µA	$0 < V_{IN} < V_{DDA}$	5
I_{EN_11}	Input Current on EN_11 (high)			33	µA	$V_{IN} = V_{DDA}$	6

NOTES:
1) R_L = open and $V_X = 0.0$ V; $R_S = 2$ Ω; $C_L = 0.24$ uf, OUT_n = 1.65 V
2) -50 mA < I_{OUTDC} < 50 mA. Applies to OUT_1...OUT_11
3) OUT_n = 1.65 V
4) Applies to A/B_SEL and EN_11 input pins
5) Applies to all input pins except EN_11 in high state
6) Applies to EN_11 pin when V_{IN} on EN_11 pin = V_{DDA}

4.6. AC Characteristics (Preliminary data – subject to change)

$V_{DDA} = 3.3$ V, $T_A = 25°$ C.
All voltages are with respect to GND.

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions	Note
T_{SET}	Settling Time			8.0	µsec	Fig. 4-2	1
SR+, SR-	Pos. & Neg. Slew Rate	0.6			V/µsec	Fig. 4-2	1

NOTES:
1) $R_L/R_S < 5$, -50 mA < I_{OUTDC} < 50 mA. $C_L = 0.24$ µF.
Measured for a 2.6V step settling to within 30 mV of final value.
Applies to OUT_1 .. OUT_11
2) Slew rate measured between 20% and 80% points of step.
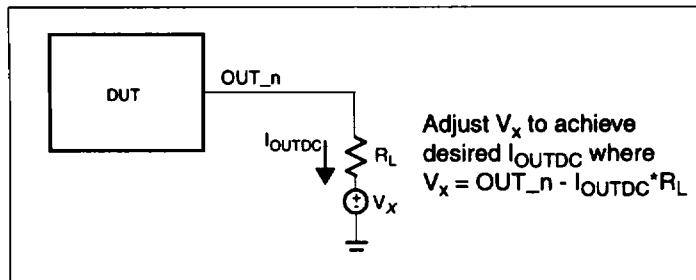
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Figure 4-1


Figure 4-2

Figure 4-3

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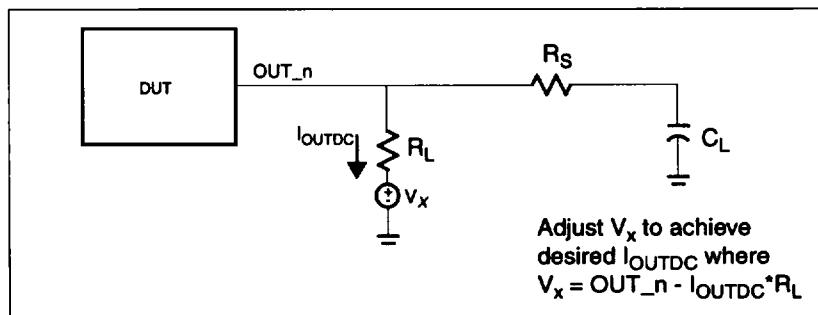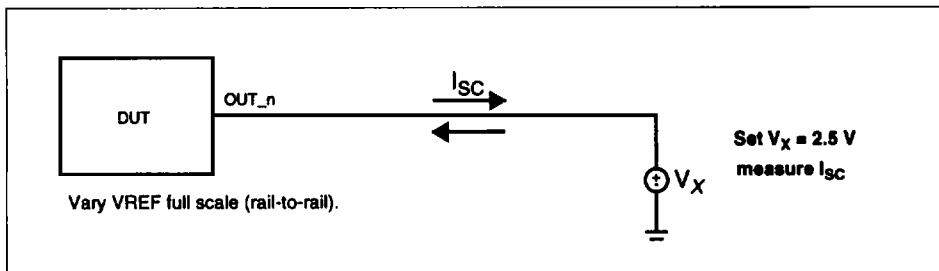
CIRRUS LOGIC

5. ORDERING INFORMATION

5.1 Package Marking Guide

FP6131GS – EP

└── Revision †

Flat Panel ┘

Part Number ───

Package Type ──
GS : 48 TSSOP
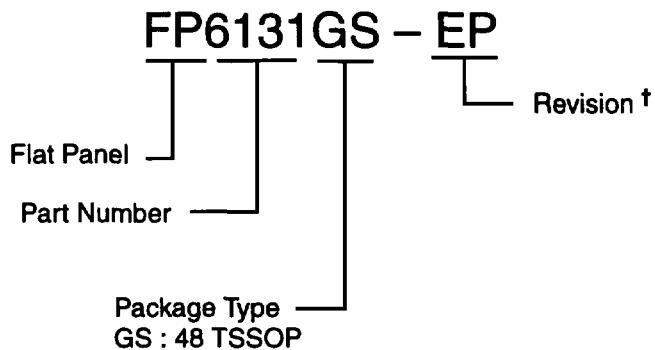
† Contact Cirrus Logic, Inc. for up-to-date information on revisions.

Updates from Previous Version

Date of Issue	Page	Description
June 10, 1996	4	Add Die Dimension & Pad Coordinates
	7	Change operating temp. range to -20 to 85 °C. Change storage temp range to -30 to 85 °C.
	8	Change step size in Section 4.4 note 1 from 4.6 Volts to 4.4 Volts. Add note 2 to Section 4.4
	9	Change maximum input offest error from 20 mV to 30 mV in section 4.5 Add note 2 to Section 4.6
	11	Change Suffix from EP1 to EP