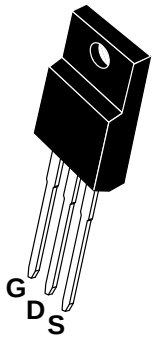
*Advanced N-Ch Power MOSFET*

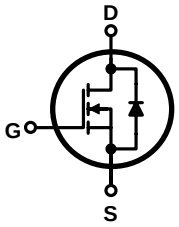
**PIN Connection TO-220F**




## Switchng Regulator Application

## Features

- High Voltage: $BV_{DSS}$=600V(Min.)
- Low $C_{rss}$ : $C_{rss}$=3.4F(Typ.)
- Low gate charge : Qg= 7.0nC(Typ.)
- Low $R_{DS(on)}$ :$R_{DS(on)}$=7.0Ω(Max.)




**Marking Diagram**


Y = Year
A = Assembly Location
WW = Work Week
FIR2N60F = Specific Device Code

## Absolute maximum ratings ($T_C$=25°C unless otherwise noted) Advanced N-Ch Power MOSFET

| Characteristic Symbol | | | Rating | Unit |
|---|---|---|---|---|
| Drain-source voltage | $V_{DSS}$ 600 | | | V |
| Gate-source voltage | $V_{GSS}$ | | ±20 | V |
| Drain current (DC) * | $I_D$ | (Tc=25℃) | 1.5 | A |
| | | (Tc=100℃) | 1 | A |
| Drain current (Pulsed) * | $I_{DM}$ 6.0 | | | A |
| Power dissipation | $P_D$19.1 | | | W |
| Avalanche current (Single) ② | $I_{AS}$ 2.0 | | | A |
| Single pulsed avalanche energy ② | $E_{AS}$ 88 | | | mJ |
| Avalanche current (Repetitive) ① | $I_{AR}$ 2.0 | | | A |
| Repetitive avalanche energy ① | $E_{AR}$ 8 | | | mJ |
| Junction temperature | $T_J$ | | 150 | °C |
| Storage temperature range | $T_{stg}$ | | -55~150 | |

* Limited by maximum junction temperature

| Characteristic Symbol | | | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Thermal resistance | Junction-case R | $_{th(J-C)}$ - | | 5.6 | °C/W |
| | Junction-ambient R | $_{th(J-A)}$ - | | 100 | |

## Electrical Characteristics ($T_C$=25°C unless otherwise noted)

| Characteristic Symbol | | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Drain-source breakdown voltage | $BV_{DSS}$ | $I_D$=250uA, $V_{GS}$=0 600 | | - | - | V |
| Gate threshold voltage | $V_{GS(th)}$ | $I_D$=250uA, $V_{DS}$=$V_{GS}$ | 2.0 | 3.0 | 4.0 | |
| Drain-source cut-off current | $I_{DSS}$ | $V_{DS}$=600V, $V_{GS}$=0V - | | - | 25 | uA |
| Gate leakage current | $I_{GSS}$ | $V_{DS}$=0V, $V_{GS}$=±30V | - - | | ±100 | nA |
| Drain-source on-resistance | $R_{DS(ON)}$ | $V_{GS}$=10V, $I_D$=1.0A - | | 7.0 | 8.0 | Ω |
| Forward transfer conductance | $g_{fs}$ | $V_{DS}$=10V, $I_D$=1.0A | - | 5 | - | S |
| Input capacitance | Ciss - | $V_{GS}$=0V, $V_{DS}$=25V, f=1MHz | | 170 | - | pF |
| Output capacitance | Coss | | - | 27 | - | |
| Reverse transfer capacitance | Crss | | - | 5 | - | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD}$=300V, $I_D$=1.5A $R_G$=4.7Ω | - | 8 | - | ns |
| Rise time | $t_r$ - | | | 30 | - | |
| Turn-off delay time | $t_{d(off)}$ | | - | 22 | - | |
| Fall time | $t_f$ | | - 55 | | - | |
| Total gate charge | $Q_g$ - | - $V_{DS}$=480V, $V_{GS}$=10V $I_D$=1.5A | | 7.5 | | nC |
| Gate-source charge | $Q_{gs}$ - | | | 1.7 | - | |
| Gate-drain charge | $Q_{gd}$ | | - 4. | 0 | - | |

## Source-Drain Diode Ratings and Characteristics ($T_C$=25°C unless otherwise noted)

| Characteristic Symbol | | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Source current (DC) | $I_S$ | Integral reverse diode in the MOSFET | - | - | 1.5 | A |
| Source current (Pulsed) | $I_{SM}$ | | - - | | 6.0 | |
| Forward voltage | $V_{SD}$ | $V_{GS}$=0V, $I_S$=1.5A - | | - | 1.5 | V |
| Reverse recovery time | $t_{rr}$ | $I_S$=1.5A, $V_{GS}$=0V $dI_F/dt$=100A/us | - | 250 | - | ns |
| Reverse recovery charge | $Q_{rr}$ | | - | 550 - | | nC |

Note ;

① Repetitive rating : Pulse width limited by maximum junction temperature

② L=10.0mH, $I_{AS}$=1.5A, $V_{DD}$=50V, $R_G$=25Ω, Starting $T_J$=25℃

③ Pulse Test : Pulse width≤300us, Duty cycle≤2%

④ Essentially independent of operating temperature

# Electrical Characteristic Curves

**Fig. 1 $I_D$ - $V_{DS}$**

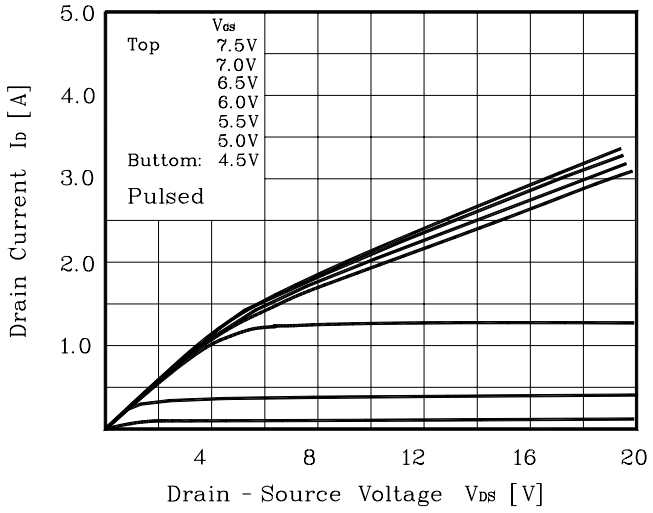



**Fig. 2 $I_D$ - $V_{GS}$**

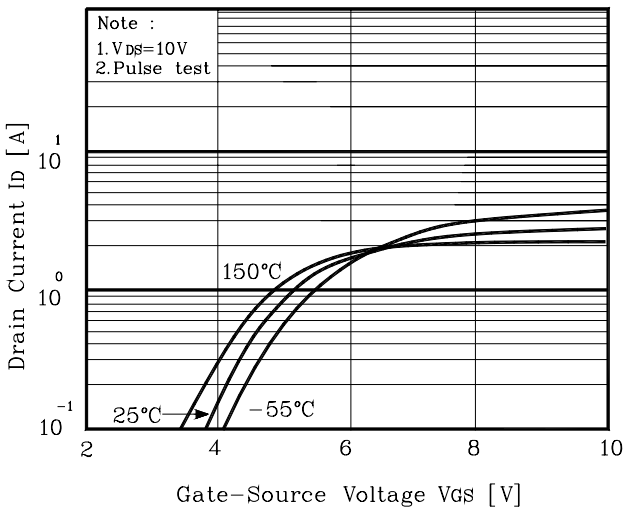



**Fig. 3 $R_{DS(on)}$ - $I_D$**

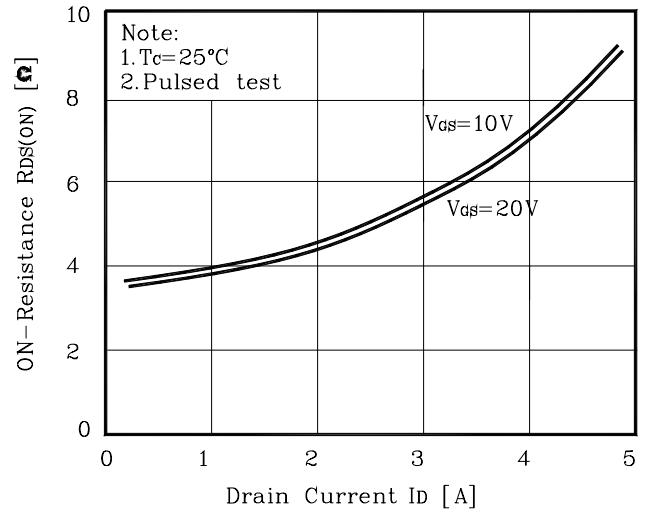



**Fig. 4 $I_S$ - $V_{SD}$**

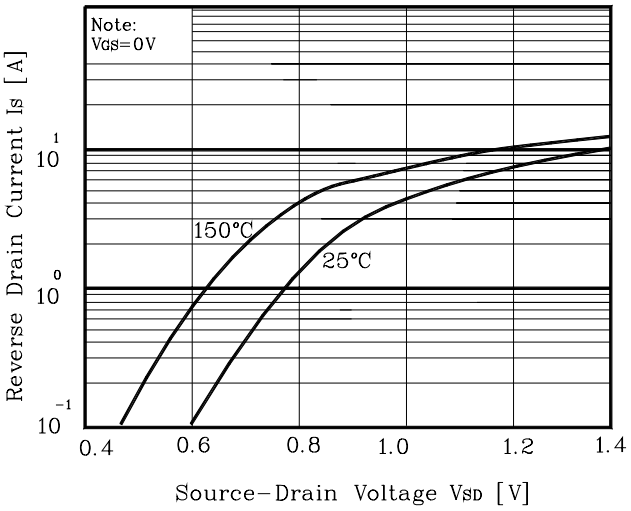



**Fig. 5 Capacitance - $V_{DS}$**

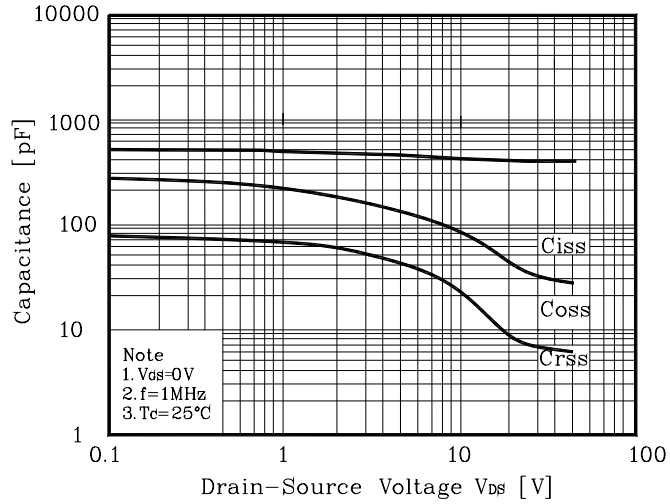
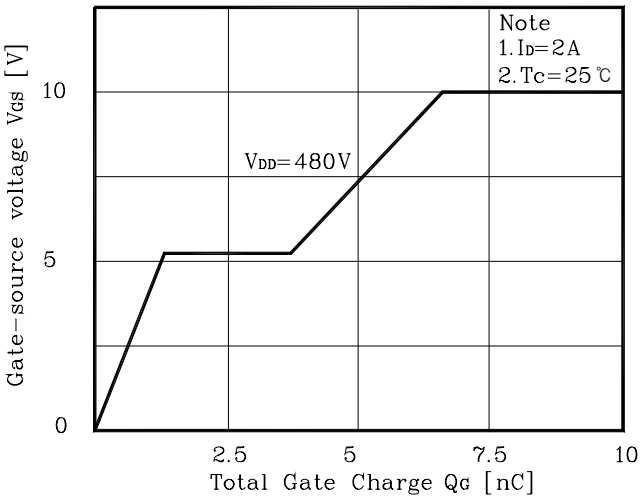



**Fig. 6 $V_{GS}$ - $Q_G$**



# Electrical Characteristic Curves

**Fig. 7 $V_{DSS}$ - $T_J$**

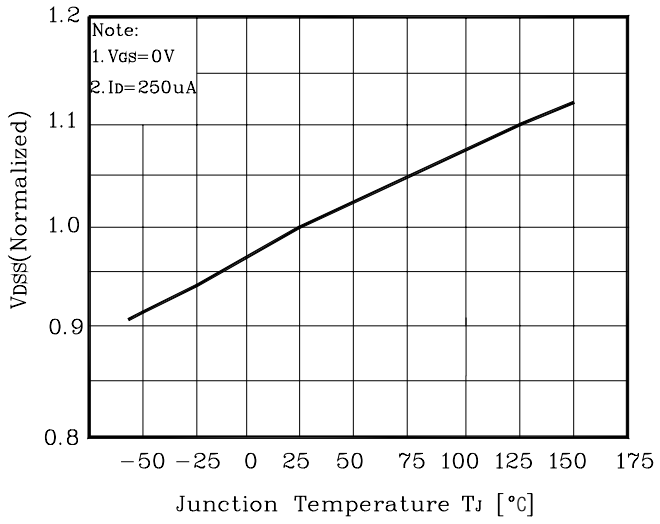



**Fig. 8 $R_{DS(on)}$ - $T_J$**

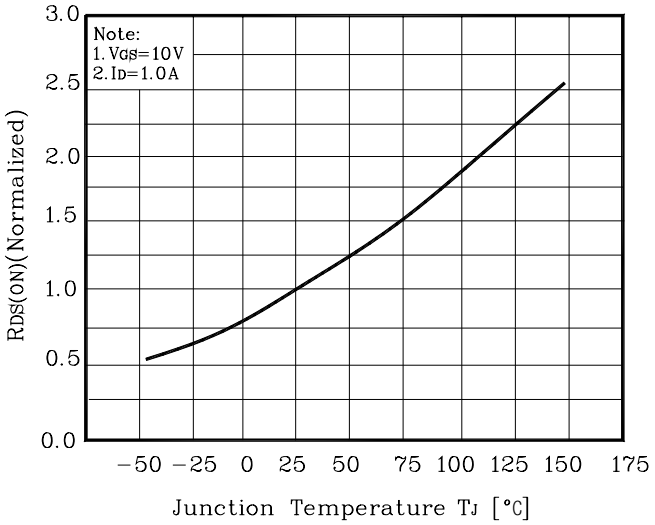
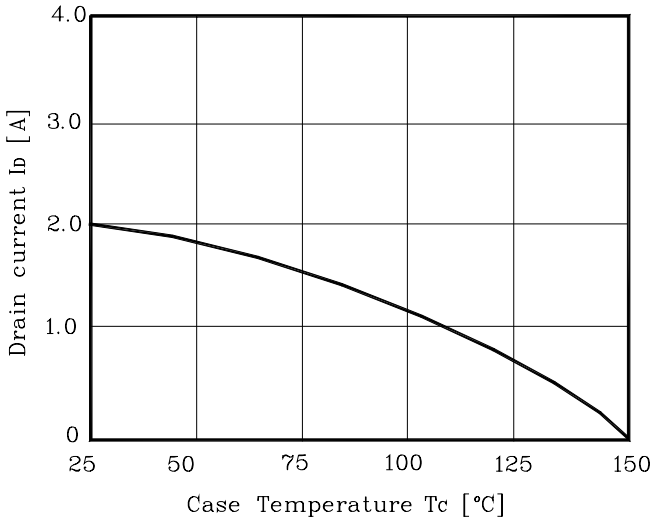



**Fig. 9 $I_D$ - $T_C$**




**Fi g. 10 Safe Operating Area**

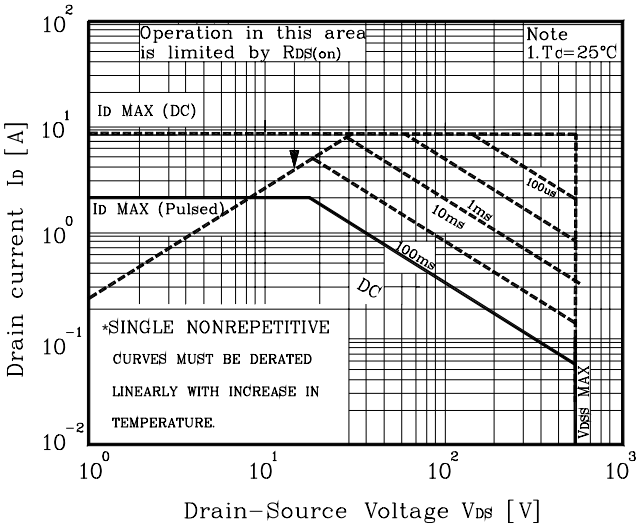
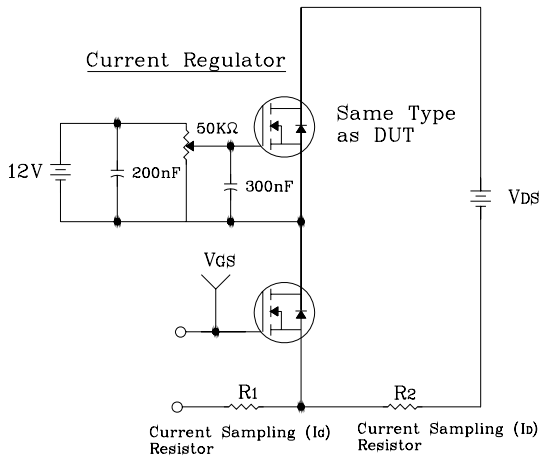


**Fig. 11 Gate Charge Test Circuit & Waveform**



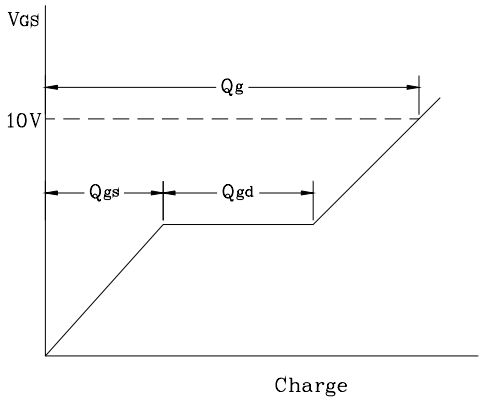
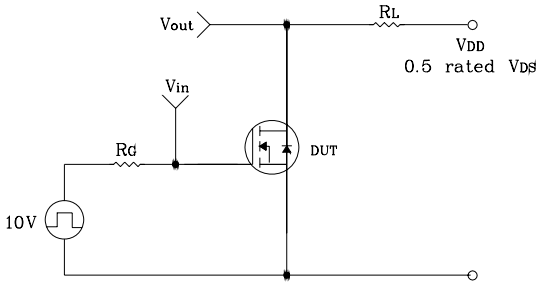




**Fig. 12 Resistive Switching Test Circuit & Waveform**



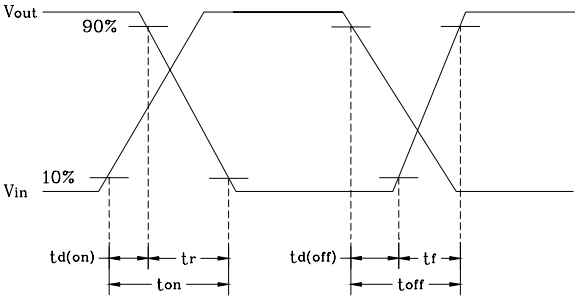
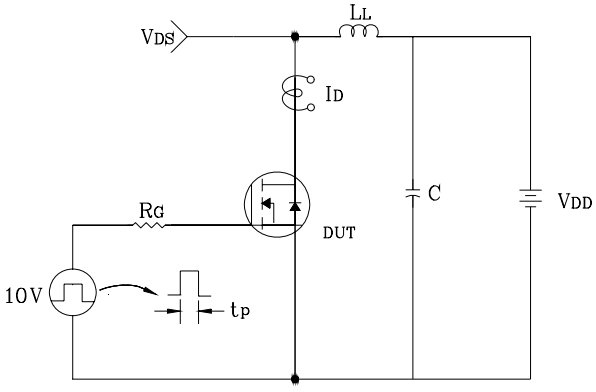




**Fig. 13 $E_{AS}$ Test Circuit & Waveform**



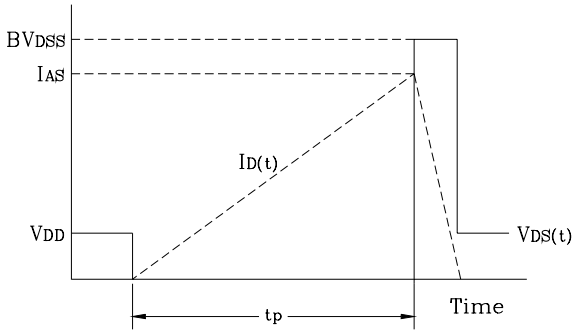
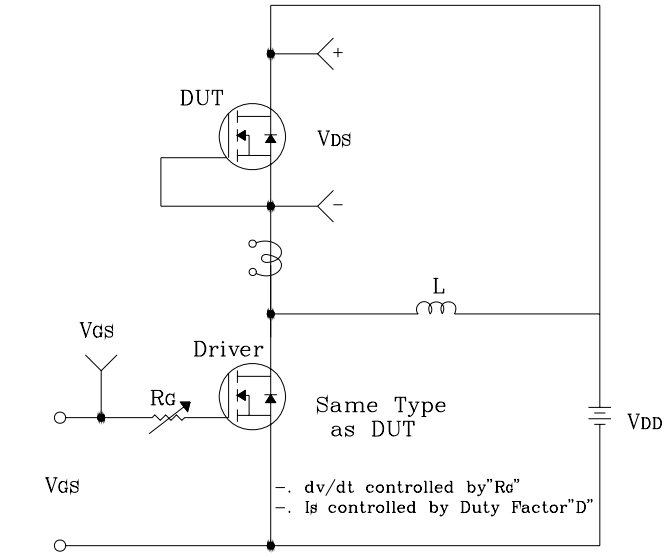
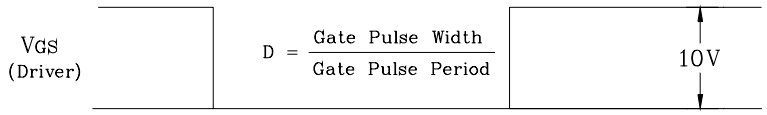
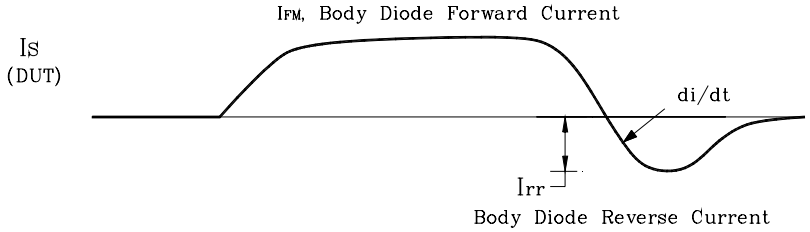
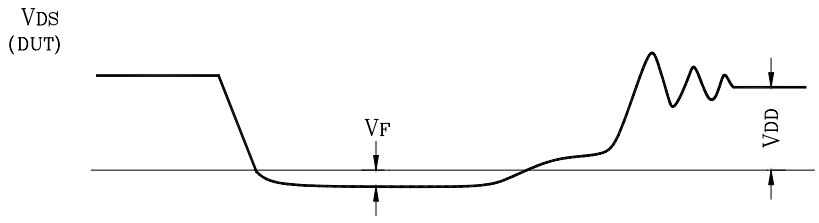



**Fig. 14 Diode Reverse Recovery Time Test Circuit & Waveform**



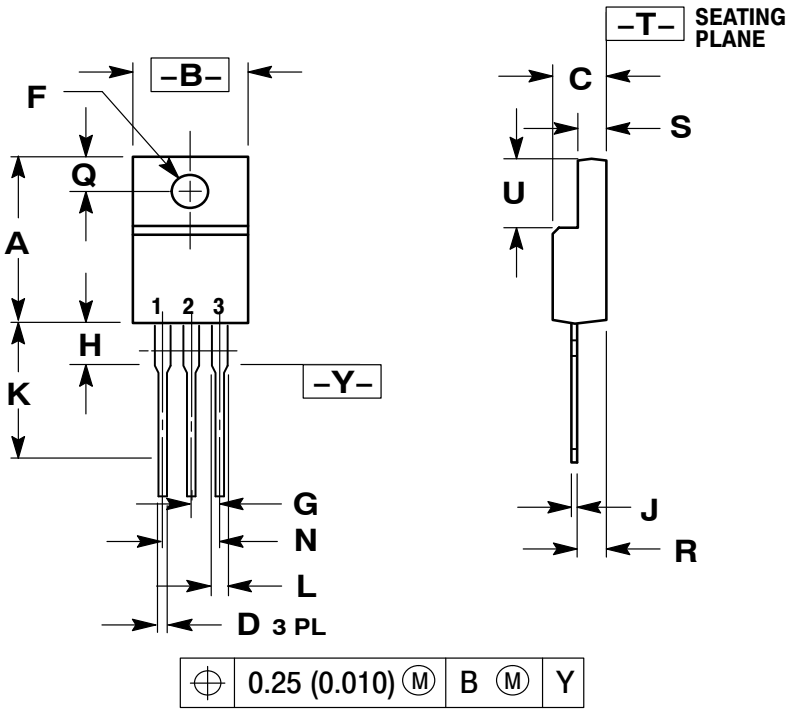



## Package Dimensions

TO-220F




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH
3. 221D-01 THRU 221D-02 OBSOLETE, NEW STANDARD 221D-03.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.617 | 0.635 | 15.67 | 16.12 |
| B | 0.392 | 0.419 | 9.96 | 10.63 |
| C | 0.177 | 0.193 | 4.50 | 4.90 |
| D | 0.024 | 0.039 | 0.60 | 1.00 |
| F | 0.116 | 0.129 | 2.95 | 3.28 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.118 | 0.135 | 3.00 | 3.43 |
| J | 0.018 | 0.025 | 0.45 | 0.63 |
| K | 0.503 | 0.541 | 12.78 | 13.73 |
| L | 0.048 | 0.058 | 1.23 | 1.47 |
| N | 0.200 BSC | | 5.08 BSC | |
| Q | 0.122 | 0.138 | 3.10 | 3.50 |
| R | 0.099 | 0.117 | 2.51 | 2.96 |
| S | 0.092 | 0.113 | 2.34 | 2.87 |
| U | 0.239 | 0.271 | 6.06 | 6.88 |