EPSON

S1C88816

8-bit Single Chip Microcomputer

Low Voltage Operation Products

- Original Architecture Core CPU
- Large Capacity ROM (116K bytes)
- Low Current Consumption
- Wide-range Operating Voltage (1.8V to 5.5V)
- Built-in Melody Generator and A/D Converter

■ DESCRIPTION

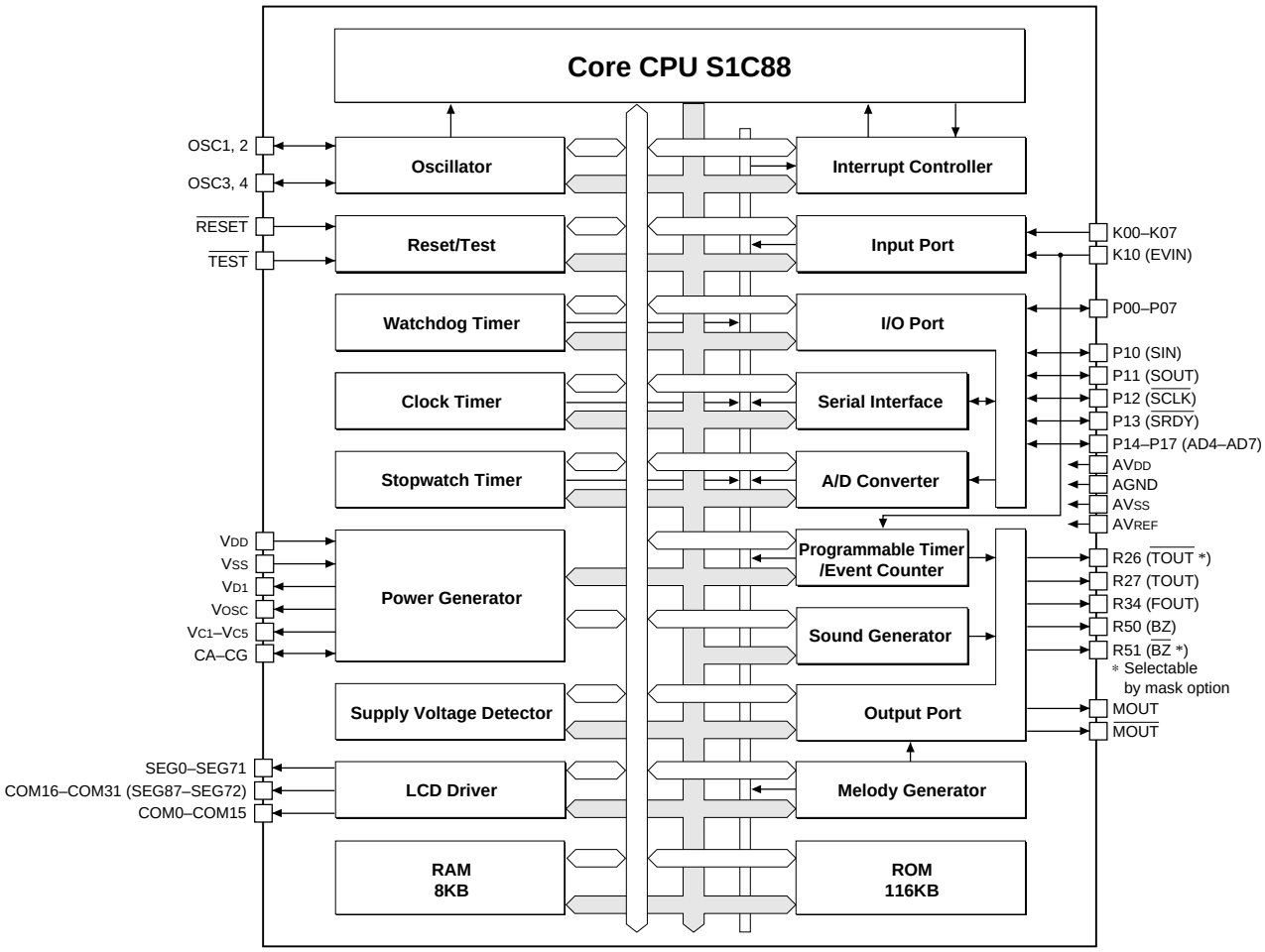
The S1C88816 microcomputer features the S1C88 (MODEL 3) CMOS 8-bit core CPU along with a 116K bytes of ROM, an 8K bytes of RAM, three different timers, a serial interface with optional asynchronization or clock synchronization, a melody generator and an A/D converter. The S1C88816 has large capacity of ROM and RAM and fully operable over a wide range of voltages. Furthermore, it can perform high speed operations even at low voltage. Like all the equipment in the S1C Family, these microcomputers have low power consumption.

■ FEATURES

- Core CPU ..... S1C88 (MODEL3) CMOS 8-bit core CPU
- OSC1 Oscillation circuit ..... Crystal oscillation circuit/CR oscillation circuit/external clock input 32.768 kHz (Typ.)
- OSC3 Oscillation circuit ..... Crystal oscillation circuit/ceramic oscillation circuit/CR oscillation circuit/ external clock input 8.2 MHz (Max.)
- Instruction set ..... 608 types (usable for multiplication and division instructions)
- Min. instruction execution time .. 0.244 µsec/8.2 MHz (2 clock)
- Internal ROM capacity ..... 116K bytes
- Internal RAM capacity ..... 8K bytes/RAM, 4224 bits/display memory, 512 bytes/melody RAM
- Input port ..... 9 bits (1 bit can be set for event counter external clock input)
- Output port ..... 7 bits (can be set for BZ, $\overline{BZ}$, TOUT, $\overline{TOUT}$ and FOUT output)
- I/O port ..... 16 bits (P10–P13 and P14–P17 can be set for serial I/F input/output and A/D converter input, respectively)
- Serial interface ..... 1ch (Optional clock synchronous system or asynchronous system)
- Timer ..... Programmable timer (8 bits): 2ch
  (1ch can be set as a an event counter or 2ch as a 16 bits programmable timer for 1ch)
  Clock timer (8 bits): 1ch
  Stopwatch timer (8 bits): 1ch
- Power supply circuit to drive liquid crystals .. Built-in (booster type, 5 potentials/4 potentials)
- LCD driver ..... Dot matrix type (compatible with 5 × 8 or 5 × 5 fonts)
  72 segments × 32 common (1/5 bias)
  88 segments × 16 common (1/5 bias or 1/4 bias)
  88 segments × 8 common (1/5 bias or 1/4 bias)
- Sound generator ..... Envelope function, equipped with volume control
- Watchdog timer ..... Built-in
- Supply voltage detection (SVD) circuit .. Can detect up to 16 different voltage levels
- Melody generator ..... 1 sound source (scale: 3 octaves, note: 8 types, tempo: 16 types)
  Note and scale data are stored into the melody RAM (allows the CPU to read and write)
- A/D converter ..... Successive-approximation type, resolution: 10 bits, input: 4ch (shared with P14–P17)

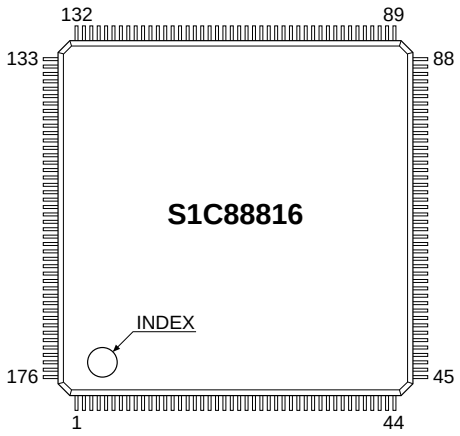
- Interrupt ..... External interrupt: Input interrupt 2 systems (3 types)
  Internal interrupt: Timer interrupt 3 systems (9 types)
  Serial interface interrupt 1 system (3 types)
  Melody interrupt 1 system (1 type)
  A/D converter interrupt 1 system (1 type)
- Supply voltage ..... Normal mode: 2.4 V–5.5 V (Max. 4.2 MHz)
  Low power mode: 1.8 V–5.5 V (Max. 80 kHz)
  High speed mode: 3.5 V–5.5 V (Max. 8.2 MHz)
- Con-sumed current ..... SLEEP: 0.45µA
  HALT (32.768 kHz): 1.5µA
  In operation (32.768 kHz): 7µA
  In operation (4 MHz): 0.9mA
- Supply form ..... QFP18-176pin, or chip

■ BLOCK DIAGRAM



■ PIN CONFIGURATION

QFP18-176pin



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	N.C.	45	N.C.	89	N.C.	133	N.C.
2	N.C.	46	SEG56	90	N.C.	134	N.C.
3	SEG16	47	SEG57	91	V_{C3}	135	P01
4	SEG17	48	SEG58	92	V_{C2}	136	P00
5	SEG18	49	SEG59	93	V_{C1}	137	MOUT
6	SEG19	50	SEG60	94	OSC3	138	$\overline{\text{MOUT}}$
7	SEG20	51	SEG61	95	OSC4	139	R26/$\overline{\text{TOUT}}$
8	SEG21	52	SEG62	96	V_{D1}	140	R27/TOUT
9	SEG22	53	SEG63	97	V_{DD}	141	R34/FOUT
10	SEG23	54	SEG64	98	V_{SS}	142	R50/BZ
11	SEG24	55	SEG65	99	V_{OSC}	143	R51/$\overline{\text{BZ}}$
12	SEG25	56	SEG66	100	OSC1	144	COM0
13	SEG26	57	SEG67	101	OSC2	145	COM1
14	SEG27	58	SEG68	102	$\overline{\text{TEST}}$	146	COM2
15	SEG28	59	SEG69	103	$\overline{\text{RESET}}$	147	COM3
16	SEG29	60	SEG70	104	K10/EVIN	148	COM4
17	SEG30	61	SEG71	105	K07	149	COM5
18	SEG31	62	COM31/SEG72	106	K06	150	COM6
19	SEG32	63	COM30/SEG73	107	K05	151	COM7
20	SEG33	64	COM29/SEG74	108	K04	152	COM8
21	SEG34	65	COM28/SEG75	109	K03	153	COM9
22	SEG35	66	COM27/SEG76	110	K02	154	COM10
23	SEG36	67	COM26/SEG77	111	K01	155	COM11
24	SEG37	68	COM25/SEG78	112	K00	156	COM12
25	SEG38	69	COM24/SEG79	113	P17/AD7	157	COM13
26	SEG39	70	COM23/SEG80	114	P16/AD6	158	COM14
27	SEG40	71	COM22/SEG81	115	P15/AD5	159	COM15
28	SEG41	72	COM21/SEG82	116	P14/AD4	160	SEG0
29	SEG42	73	COM20/SEG83	117	P13/$\overline{\text{SRDY}}$	161	SEG1
30	SEG43	74	COM19/SEG84	118	P12/$\overline{\text{SCLK}}$	162	SEG2
31	SEG44	75	COM18/SEG85	119	P11/SOUT	163	SEG3
32	SEG45	76	COM17/SEG86	120	P10/SIN	164	SEG4
33	SEG46	77	COM16/SEG87	121	AV_{DD}	165	SEG5
34	SEG47	78	CG	122	AGND	166	SEG6
35	SEG48	79	CF	123	AV_{SS}	167	SEG7
36	SEG49	80	CE	124	AV_{REF}	168	SEG8
37	SEG50	81	CD	125	P07	169	SEG9
38	SEG51	82	CC	126	P06	170	SEG10
39	SEG52	83	CB	127	P05	171	SEG11
40	SEG53	84	CA	128	P04	172	SEG12
41	SEG54	85	V_{C5}	129	P03	173	SEG13
42	SEG55	86	V_{C4}	130	P02	174	SEG14
43	N.C.	87	N.C.	131	N.C.	175	SEG15
44	N.C.	88	N.C.	132	N.C.	176	N.C.

N.C.: No Connection

■ PIN DESCRIPTION

Pin name	Pin No.	In/Out	Function
V_{DD}	97	–	Power supply (+) terminal
V_{SS}	98	–	Power supply (-) terminal
V_{D1}	96	–	Regulated voltage for internal circuit
V_{OSC}	99	–	Regulated voltage for OSC1 oscillation circuit
V_{C1}–V_{C5}	93–91, 86, 85	O	LCD drive voltage output terminals
CA–CG	84–78	–	Voltage boost/reduce-capacitor connection terminals for LCD
OSC1	100	I	OSC1 oscillation input terminal (select crystal oscillation/CR oscillation/external clock input by mask option)
OSC2	101	O	OSC1 oscillation output terminal
OSC3	94	I	OSC3 oscillation input terminal (select crystal/ceramic/CR oscillation/external clock input by mask option)
OSC4	95	O	OSC3 oscillation output terminal
K00–K07	112–105	I	Input terminals (K00–K07)
K10/EVIN	104	I	Input terminal (K10) or event counter external clock input terminal (EVIN)
R26/$\overline{\text{TOUT}}$	139	O	Output terminal (R26) or programmable timer underflow signal inverted output terminal ($\overline{\text{TOUT}}$) (selectable by mask option)
R27/TOUT	140	O	Output terminal (R27) or programmable timer underflow signal output terminal (TOUT)
R34/FOUT	141	O	Output terminal (R34) or clock output terminal (FOUT)
R50/BZ	142	O	Output terminal (R50) or buzzer output terminal (BZ)
R51/$\overline{\text{BZ}}$	143	O	Output terminal (R51) or buzzer inverted output terminal ($\overline{\text{BZ}}$) (selectable by mask option)
P00–P07	136, 135, 130–125	I/O	I/O terminals (P00–P07)
P10/SIN	120	I/O	I/O terminal (P10) or serial I/F data input terminal (SIN)
P11/SOUT	119	I/O	I/O terminal (P11) or serial I/F data output terminal (SOUT)
P12/$\overline{\text{SCLK}}$	118	I/O	I/O terminal (P12) or serial I/F clock I/O terminal ($\overline{\text{SCLK}}$)
P13/$\overline{\text{SRDY}}$	117	I/O	I/O terminal (P13) or serial I/F ready signal output terminal ($\overline{\text{SRDY}}$)
P14/AD4	116	I/O	I/O terminal (P14) or A/D converter input terminal (AD4)
P15/AD5	115	I/O	I/O terminal (P15) or A/D converter input terminal (AD5)
P16/AD6	114	I/O	I/O terminal (P16) or A/D converter input terminal (AD6)
P17/AD7	113	I/O	I/O terminal (P17) or A/D converter input terminal (AD7)
MOUT	137	O	Melody output terminal
$\overline{\text{MOUT}}$	138	O	Melody inverted output terminal
COM0–COM15	144–159	O	LCD common output terminals
COM16–COM31 /SEG87–SEG72	77–62	O	LCD common output terminals (when 1/32 duty is selected) or LCD segment output terminal (when 1/16 or 1/8 duty is selected)
SEG0–SEG71	160–175, 3–42, 46–61	O	LCD segment output terminals
$\overline{\text{RESET}}$	103	I	Initial reset input terminal
$\overline{\text{TEST}}$ *1	102	I	Test input terminal
AV_{DD}	121	–	Analog system power supply (+) terminal
AV_{SS}	123	–	Analog system power supply (–) terminal
AGND	122	–	Analog system ground terminal
AV_{REF}	124	I	Analog system reference voltage input terminal

*1 $\overline{\text{TEST}}$ is the terminal used for shipping inspection of the IC. For normal operation be sure it is connected to V_{DD}.

■ OPTION LIST

S5U1C88816P Option List

A OSC1 SYSTEM CLOCK
- ☐ 1. Internal Clock (32.768 kHz)
- ☐ 2. User Clock

B OSC3 SYSTEM CLOCK
- ☐ 1. Internal Clock (4.9152 MHz)
- ☐ 2. User Clock

S1C88816 Mask Option List

1 OSC1 SYSTEM CLOCK
- ☐ 1. Crystal
- ☐ 2. External Clock
- ☐ 3. CR
- ☐ 4. Crystal (with Gate Capacity)

2 OSC3 SYSTEM CLOCK
- ☐ 1. Crystal
- ☐ 2. Ceramic
- ☐ 3. CR
- ☐ 4. External Clock

3 MULTIPLE KEY ENTRY RESET
- COMBINATION ..... ☐ 1. Not Use
  - ☐ 2. Use K00, K01
  - ☐ 3. Use K00, K01, K02
  - ☐ 4. Use K00, K01, K02, K03

4 SVD RESET
- ☐ 1. Not Use
- ☐ 2. Use

5 INPUT PORT PULL UP RESISTOR

• K00	☐ 1. With Resistor	☐ 2. Gate Direct
• K01	☐ 1. With Resistor	☐ 2. Gate Direct
• K02	☐ 1. With Resistor	☐ 2. Gate Direct
• K03	☐ 1. With Resistor	☐ 2. Gate Direct
• K04	☐ 1. With Resistor	☐ 2. Gate Direct
• K05	☐ 1. With Resistor	☐ 2. Gate Direct
• K06	☐ 1. With Resistor	☐ 2. Gate Direct
• K07	☐ 1. With Resistor	☐ 2. Gate Direct
• K10	☐ 1. With Resistor	☐ 2. Gate Direct
• $\overline{\text{RESET}}$	☐ 1. With Resistor	☐ 2. Gate Direct

6 I/O PORT PULL UP RESISTOR

• P00	☐ 1. With Resistor	☐ 2. Gate Direct
• P01	☐ 1. With Resistor	☐ 2. Gate Direct
• P02	☐ 1. With Resistor	☐ 2. Gate Direct
• P03	☐ 1. With Resistor	☐ 2. Gate Direct
• P04	☐ 1. With Resistor	☐ 2. Gate Direct
• P05	☐ 1. With Resistor	☐ 2. Gate Direct
• P06	☐ 1. With Resistor	☐ 2. Gate Direct
• P07	☐ 1. With Resistor	☐ 2. Gate Direct

- P10 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- P11 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- P12 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- P13 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- P14 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- P15 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- P16 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- P17 ..... ☐ 1. With Resistor ☐ 2. Gate Direct

7 LCD DRIVE DUTY

☐ 1. 1/32 & 1/16 Duty
☐ 2. 1/8 Duty

8 LCD POWER SUPPLY

☐ 1. Internal TYPE A (V_{C2} Standard, 1/5 Bias, 4.5 V)
☐ 2. External
☐ 3. Internal TYPE B (V_{C2} Standard, 1/5 Bias, 5.5 V)
☐ 4. Internal TYPE C (V_{C2} Standard, 1/4 Bias, 4.5 V)
☐ 5. Internal TYPE D (V_{C1} Standard, 1/4 Bias, 4.5 V)

9 $\overline{BZ}$ OUTPUT (R51)

☐ 1. Use
☐ 2. Not Use

10 $\overline{TOUT}$ OUTPUT (R26)

☐ 1. Use
☐ 2. Not Use

11 CPU MODE

☐ 1. Maximum Mode
☐ 2. Minimum Mode

12 MODE DURING BUZZER OUTPUT

☐ 1. Normal Mode
☐ 2. Heavy Load Protection Mode

13 MODE DURING MELODY OUTPUT

☐ 1. Normal Mode
☐ 2. Heavy Load Protection Mode

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS}=0V)

Item	Symbol	Condition	Rated value	Unit	Note
Power voltage	V_{DD}		-0.3 to +7.0	V	
Liquid crystal power voltage	V_{C5}		-0.3 to +7.0	V	
Input voltage	V_I		-0.3 to V_{DD} + 0.3	V	
Output voltage	V_O		-0.3 to V_{DD} + 0.3	V	1
High level output current	I_{OH}	1 terminal	-5	mA	
		Total of all terminals	-20	mA	
Low level output current	I_{OL}	1 terminal	5	mA	
		Total of all terminals	20	mA	
Permitted loss	P_D		200	mW	2
Operating temperature	Topr		-40 to +85	°C	
Storage temperature	Tstg		-65 to +150	°C	
Soldering temperature / time	Tsol		260°C, 10sec (lead section)	–	

Note) 1 Case that to Nch open drain output by the mask option is included.
2 In case of plastic package.

● Recommended Operating Conditions

(V_{SS}=0V, Ta=-40 to 85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Operating power voltage (Normal mode)	V_{DD}		2.4		5.5	V	
Operating power voltage (Low power mode)	V_{DD}		1.8		5.5	V	
Operating power voltage (High speed mode)	V_{DD}		3.5		5.5	V	
Analog power voltage	AV_{DD}	$AV_{DD} \geq 2.7$ V	V_{DD}-0.05		V_{DD}+0.05	V	
Operating frequency (Normal mode)	f_{OSC1}	V_{DD} = 2.4 to 5.5 V	30.000	32.768	80.000	kHz	1
	f_{OSC3}		0.03		4.2	MHz	1
Operating frequency (Low power mode)	f_{OSC1}	V_{DD} = 1.8 to 5.5 V	30.000	32.768	80.000	kHz	1
Operating frequency (High speed mode)	f_{OSC1}	V_{DD} = 3.5 to 5.5 V	30.000	32.768	80.000	kHz	1
	f_{OSC3}		0.03		8.2	MHz	1
Liquid crystal power voltage	V_{C5}	$V_{C5} \geq V_{C4} \geq V_{C3} \geq V_{C2} \geq V_{C1} \geq V_{SS}$			6.0	V	2
Capacitor between V_{D1} and V_{SS}	C_1			0.1		µF	
Capacitor between V_{C1} and V_{SS}	C_2			0.1		µF	3
Capacitor between V_{C2} and V_{SS}	C_3			0.1		µF	3
Capacitor between V_{C3} and V_{SS}	C_4			0.1		µF	3
Capacitor between V_{C4} and V_{SS}	C_5			0.1		µF	3
Capacitor between V_{C5} and V_{SS}	C_6			0.1		µF	3
Capacitor between CA and CB	C_7			0.1		µF	3
Capacitor between CA and CC	C_8			0.1		µF	3
Capacitor between CD and CE	C_9			0.1		µF	3
Capacitor between CF and CG	C_{10}			0.1		µF	3

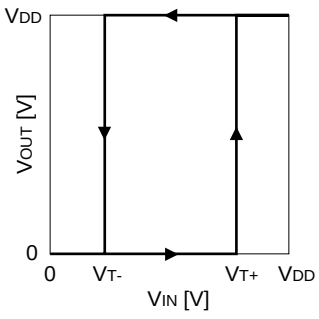
Note) 1 When an external clock is input from the OSC1 terminal by the mask option, leave the OSC2 terminal open, and when an external clock is input from the OSC3 terminal, leave the OSC4 terminal open.
2 When external power supply is selected by the mask option.
3 When LCD drive power is not used, the capacitor is not necessary. In this case, leave the V_{C1} to V_{C5} and CA to CG terminals open.

● DC Characteristics

(Unless otherwise specified: V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=-40 to 85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
High level input voltage (1)	V_{IH1}	Kxx, Pxx	0.8V_{DD}		V_{DD}	V	
Low level input voltage (1)	V_{IL1}	Kxx, Pxx	0		0.2V_{DD}	V	
High level input voltage (2) (Normal mode)	V_{IH2}	OSC3	1.6		V_{DD}	V	1
High level input voltage (2)	V_{IH2}	OSC1	1.0		V_{DD}	V	1
High level input voltage (2) (High speed mode)	V_{IH2}	OSC3	2.4		V_{DD}	V	1
Low level input voltage (2) (Normal mode)	V_{IL2}	OSC3	0		0.6	V	1
Low level input voltage (2)	V_{IL2}	OSC1	0		0.3	V	1
Low level input voltage (2) (High speed mode)	V_{IL2}	OSC3	0		0.9	V	1
High level schmitt input voltage	V_{T+}	$\overline{RESET}$	0.5V_{DD}		0.9V_{DD}	V	
Low level schmitt input voltage	V_{T-}	$\overline{RESET}$	0.1V_{DD}		0.5V_{DD}	V	
High level output current	I_{OH}	Pxx, Rxx, V_{OH} = 0.9V_{DD}			-0.5	mA	
Low level output current	I_{OL}	Pxx, Rxx, V_{OL} = 0.1V_{DD}	0.5			mA	
Input leak current	I_{LI}	Kxx, Pxx, $\overline{RESET}$	-1		1	µA	
Output leak current	I_{LO}	Pxx, Rxx	-1		1	µA	
Input pull-up resistance	R_{IN}	Kxx, Pxx, $\overline{RESET}$	100	300	500	kΩ	2
Input terminal capacitance	C_{IN}	Kxx, Pxx, V_{IN} = 0V, f = 1MHz, Ta = 25°C		7	15	pF	
Segment/Common output current	I_{SEGH}	SEGxx, COMxx, V_{SEGH} = V_{C5}-0.1V			-5	µA	
	I_{SEGL}	SEGxx, COMxx, V_{SEGL} = 0.1V	5			µA	

Note) 1 When external clock is selected by mask option.
2 When pull-up resistor is added by mask option.



● LCD Driver

The Typ. values of the LCD drive voltage shown in the following table shift in difference of panel load (panel size, drive duty, display segment number). Therefore, these should be evaluated by connecting to the actual panel to be used.

(Unless otherwise specified: V_{DD}=V_{C2} (LCX=FH) + 0.1 to 5.5V, V_{SS}=0V, Ta=25°C, C_1–C_{10}=0.1µF)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Note
LCD drive voltage (V_{C2} standard)	V_{C2}	When 1 MΩ load resistor is connected between V_{SS} and V_{C2} (no panel load)			0.412V_{C5}		V	
	V_{C5} TYPE A (4.5V)	When 1 MΩ load resistor is connected between V_{SS} and V_{C5} (no panel load)	LCX = 0H		3.52		V	1
			LCX = 1H		3.64		V	
			LCX = 2H		3.76		V	
			LCX = 3H		3.88		V	
			LCX = 4H		4.00		V	
			LCX = 5H		4.12		V	
			LCX = 6H		4.24		V	
			LCX = 7H	Typ×0.94	4.37	Typ×1.06	V	
			LCX = 8H		4.51		V	
			LCX = 9H		4.63		V	
			LCX = AH		4.75		V	
			LCX = BH		4.87		V	
			LCX = CH		5.00		V	
			LCX = DH		5.12		V	
			LCX = EH		5.24		V	
			LCX = FH		5.36		V	
	V_{C5} TYPE B (5.5V)	When 1 MΩ load resistor is connected between V_{SS} and V_{C5} (no panel load)	LCX = 0H		4.20		V	1
			LCX = 1H		4.34		V	
			LCX = 2H		4.49		V	
			LCX = 3H		4.63		V	
			LCX = 4H		4.78		V	
			LCX = 5H		4.92		V	
			LCX = 6H		5.07		V	
			LCX = 7H	Typ×0.94	5.21	Typ×1.06	V	
			LCX = 8H		5.36		V	
			LCX = 9H		5.50		V	
			LCX = AH		5.65		V	
			LCX = BH		5.80		V	
			LCX = CH		5.94		V	
			LCX = DH		6.09		V	
			LCX = EH		6.23		V	
			LCX = FH		6.38		V	
	V_{C5} TYPE C (5.5V)	When 1 MΩ load resistor is connected between V_{SS} and V_{C5} (no panel load)	LCX = 0H		3.34		V	1
			LCX = 1H		3.54		V	
			LCX = 2H		3.66		V	
			LCX = 3H		3.78		V	
			LCX = 4H		3.90		V	
			LCX = 5H		4.02		V	
			LCX = 6H		4.14		V	
			LCX = 7H	Typ×0.94	4.26	Typ×1.06	V	
			LCX = 8H		4.38		V	
			LCX = 9H		4.49		V	
			LCX = AH		4.61		V	
			LCX = BH		4.73		V	
			LCX = CH		4.85		V	
			LCX = DH		4.97		V	
			LCX = EH		5.09		V	
			LCX = FH		5.21		V	
LCD drive voltage (V_{C1} standard)	V_{C1}	When 1 MΩ load resistor is connected between V_{SS} and V_{C1} (no panel load)			0.260V_{C5}		V	
	V_{C5} TYPE D (4.5V)	When 1 MΩ load resistor is connected between V_{SS} and V_{C5} (no panel load)	LCX = 0H		3.80		V	1
			LCX = 1H		3.88		V	
			LCX = 2H		3.96		V	
			LCX = 3H		4.03		V	
			LCX = 4H		4.15		V	
			LCX = 5H		4.22		V	
			LCX = 6H		4.30		V	
			LCX = 7H	Typ×0.94	4.38	Typ×1.06	V	
			LCX = 8H		4.45		V	
			LCX = 9H		4.53		V	
			LCX = AH		4.65		V	
			LCX = BH		4.72		V	
			LCX = CH		4.80		V	
			LCX = DH		4.88		V	
			LCX = EH		4.95		V	
			LCX = FH		5.07		V	

Note) 1 Fixing the LCD contrast is not recommended. A contrast adjustment function should be included in the software.

● SVD Circuit

(Unless otherwise specified: V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
SVD voltage	V_{SVD}	Level 1 → Level 0	Typ×0.92	1.82	Typ×1.08	V	1
		Level 2 → Level 1		2.00		V	1
		Level 3 → Level 2		2.18		V	1
		Level 4 → Level 3		2.36		V	2
		Level 5 → Level 4		2.54		V	2
		Level 6 → Level 5		2.72		V	2
		Level 7 → Level 6		2.90		V	3
		Level 8 → Level 7		3.08		V	3
		Level 9 → Level 8		3.26		V	3
		Level 10 → Level 9	Typ×0.88	3.45	Typ×1.12	V	4
		Level 11 → Level 10		3.65		V	4
		Level 12 → Level 11		3.85		V	4
		Level 13 → Level 12		4.00		V	4
		Level 14 → Level 13		4.15		V	4
		Level 15 → Level 14		4.35		V	4

$V_{SVD\ (Level\ 0)}$ < $V_{SVD\ (Level\ 1)}$ < $V_{SVD\ (Level\ 2)}$ < $V_{SVD\ (Level\ 3)}$ < $V_{SVD\ (Level\ 4)}$ < $V_{SVD\ (Level\ 5)}$ < $V_{SVD\ (Level\ 6)}$ < $V_{SVD\ (Level\ 7)}$
< $V_{SVD\ (Level\ 8)}$ < $V_{SVD\ (Level\ 9)}$ < $V_{SVD\ (Level\ 10)}$ < $V_{SVD\ (Level\ 11)}$ < $V_{SVD\ (Level\ 12)}$ < $V_{SVD\ (Level\ 13)}$ < $V_{SVD\ (Level\ 14)}$ < $V_{SVD\ (Level\ 15)}$

Note) 1 Low power operating mode only
2 Low power operating mode or Normal operating mode only
3 Normal operating mode only
4 Normal operating mode or High speed operating mode only

● Current Consumption

(Unless otherwise specified: V_{DD}=Within the operating voltage in each operating mode, V_{SS}=0V, Ta=25°C, OSC1=32.768kHz crystal oscillation, C_G=25pF, OSC3=crystal/ceramic oscillation, Non heavy load protection mode, C_1–C_{10}=0.1µF, No panel load)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Power current (Normal mode)	I_{DD1}	In SLEEP status *1		0.45	1.6	µA	
	I_{DD2}	In HALT status *2		1.5	3.5	µA	
	I_{DD3}	CPU is in operating (32.768 kHz) *3		7	10	µA	
	I_{DD4}	CPU is in operating (4 MHz) *4		0.9	1.1	mA	
Power current (Low power mode)	I_{DD1}	In SLEEP status *1		0.30	1	µA	
	I_{DD2}	In HALT status *2		1	2.5	µA	
	I_{DD3}	CPU is in operating (32.768 kHz) *3		5	7	µA	
Power current (High speed mode)	I_{DD1}	In SLEEP status *1		1	3	µA	
	I_{DD2}	In HALT status *2		2	5	µA	
	I_{DD3}	CPU is in operating (32.768 kHz) *3		12	16	µA	
	I_{DD4}	CPU is in operating (8 MHz) *5		3.3	3.9	mA	
LCD drive circuit current	I_{LCDN}			6	10	µA	1
	I_{LCDH}	In heavy load protection mode		37	45	µA	2
SVD circuit current	I_{SVDN}	V_{DD} = 3.0 V		27	40	µA	3
OSC1 CR oscillation current (R_{CR1} = 500 kΩ)	I_{CR1}	In HALT status (50 kHz)		10	15	µA	4

*1 OSC1: Stop, OSC3 = Stop, CPU, ROM, RAM: SLEEP status, Clock timer: Stop, Others: Stop status
*2 OSC1: Oscillating, OSC3 = Stop, CPU, ROM, RAM: HALT status, Clock timer: Operating, Others: Stop status
*3 OSC1: Oscillating, OSC3 = Stop, CPU, ROM, RAM: Operating in 32.768 kHz, Clock timer: Operating, Others: Stop status
*4 OSC1: Oscillating, OSC3 = Oscillating, CPU, ROM, RAM: Operating in 4 MHz, Clock timer: Operating, Others: Stop status
*5 OSC1: Oscillating, OSC3 = Oscillating, CPU, ROM, RAM: Operating in 8 MHz, Clock timer: Operating, Others: Stop status

Note) 1 The LCD drive circuit current varies according to the display patterns.
2 Heavy load protection circuit current in heavy load protection mode
When the OSC3 oscillation circuit is turned ON, the IC always enters heavy load protection mode.
The mode while the buzzer or melody signals are being output can be selected by mask option.
When using a bipolar transistor as the example of the R50 terminal shown in "■ BASIC EXTERNAL CONNECTION DIAGRAM", select heavy load protection mode. When direct driving a piezoelectric buzzer as the example of the MOUT and /$\overline{MOUT}$ terminals, select normal mode.
3 The value in x V can be found by the following expression: I_{SVDN} (V_{DD} = x V) = ($x \times 20$) - 30 (Typ. value),
I_{SVDN} (V_{DD} = x V) = ($x \times 30$) - 30 (Max. value)
4 When OSC1 CR oscillation circuit is selected by the mask option.

● AC Characteristics

External memory access

(Condition: V_{DD}=Within the operating voltage in each operating mode, V_{SS}=0V, Ta=-40 to 85°C)

Item	Item	Condition	Min.	Typ.	Max.	Unit	Note
Operating frequency (Normal mode)	f_{OSC1}	V_{DD} = 2.4 to 5.5 V	30.000	32.768	80.000	kHz	
	f_{OSC3}		0.03		4.2	MHz	
Operating frequency (Low power mode)	f_{OSC1}	V_{DD} = 1.8 to 5.5 V	30.000	32.768	80.000	kHz	
Operating frequency (High speed mode)	f_{OSC1}	V_{DD} = 3.5 to 5.5 V	30.000	32.768	80.000	kHz	
	f_{OSC3}		0.03		8.2	MHz	
Instruction execution time (during operation with OSC1 clock)	tcy	1-cycle instruction	25	61	67	µS	
		2-cycle instruction	50	122	133	µS	
		3-cycle instruction	75	183	200	µS	
		4-cycle instruction	100	244	267	µS	
		5-cycle instruction	125	305	333	µS	
		6-cycle instruction	150	366	400	µS	
Instruction execution time Normal mode (during operation with OSC3 clock)	tcy	1-cycle instruction	0.5		66.7	µS	
		2-cycle instruction	1.0		133.3	µS	
		3-cycle instruction	1.4		200.0	µS	
		4-cycle instruction	1.9		266.7	µS	
		5-cycle instruction	2.4		333.3	µS	
		6-cycle instruction	2.9		400.0	µS	
Instruction execution time High speed mode (during operation with OSC3 clock)	tcy	1-cycle instruction	0.2		66.7	µS	
		2-cycle instruction	0.5		133.3	µS	
		3-cycle instruction	0.7		200.0	µS	
		4-cycle instruction	1.0		266.7	µS	
		5-cycle instruction	1.2		333.3	µS	
		6-cycle instruction	1.5		400.0	µS	

Serial interface

• Clock synchronous master mode (Normal operating mode)

(Condition: V_{DD}=2.4 to 5.5V, V_{SS}=0V, Ta=-40 to 85°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitting data output delay time	tsmd			200	nS	
Receiving data input set-up time	tsms	500			nS	
Receiving data input hold time	tsmh	200			nS	

• Clock synchronous master mode (High speed operating mode)

(Condition: V_{DD}=3.5 to 5.5V, V_{SS}=0 V, Ta=-40 to 85°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitting data output delay time	tsmd			100	nS	
Receiving data input set-up time	tsms	250			nS	
Receiving data input hold time	tsmh	200			nS	

• Clock synchronous master mode (Low power operating mode)

(Condition: V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=-40 to 85°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitting data output delay time	tsmd			5	µS	
Receiving data input set-up time	tsms	10			µS	
Receiving data input hold time	tsmh	5			µS	

• Clock synchronous slave mode (Normal operating mode)

(Condition: V_{DD}=2.4 to 5.5V, V_{SS}=0V, Ta=-40 to 85°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitting data output delay time	tssd			500	nS	
Receiving data input set-up time	tsss	200			nS	
Receiving data input hold time	tssh	200			nS	

• Clock synchronous slave mode (High speed operating mode)

(Condition: V_{DD}=3.5 to 5.5V, V_{SS}=0V, Ta=-40 to 85°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitting data output delay time	tssd			250	nS	
Receiving data input set-up time	tsss	100			nS	
Receiving data input hold time	tssh	100			nS	

• Clock synchronous slave mode (Low power operating mode)

(Condition: V_{DD}=1.8 to 5.5V, V_{SS}=0 V, Ta=-40 to 85°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitting data output delay time	tssd			10	µS	
Receiving data input set-up time	tsss	5			µS	
Receiving data input hold time	tssh	5			µS	

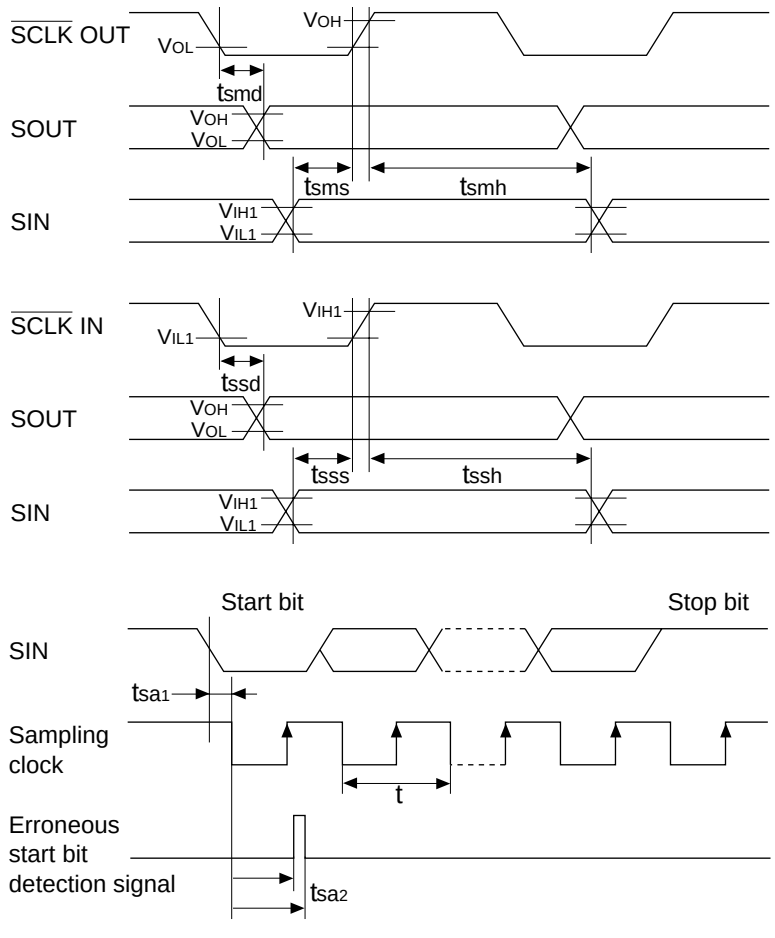
• Asynchronous system (All operating mode)

(Condition: V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=-40 to 85°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Start bit detection error time	t_{sa1}	0		t/16	S	1
Erroneous start bit detection range time	t_{sa2}	9t/16		10t/16	S	2

Note) 1 Start bit detection error time is a logical delay time from inputting the start bit until internal sampling begins operating. (Time as far as AC is excluded.)

2 Erroneous start bit detection range time is a logical range to detect whether a LOW level (start bit) has been input again after a start bit has been detected and the internal sampling clock has started. When a HIGH level is detected, the start bit detection circuit is reset and goes into a wait status until the next start bit. (Time as far as AC is excluded.)



Input clock

• OSC1, OSC3 external clock (Normal operating mode)

(Condition: V_{DD}=2.4 to 5.5V, V_{SS}=0V, Ta=-40 to 85°C, V_{IH2}=1.6 V, V_{IL2}=0.6V)

Item		Symbol	Min.	Typ.	Max.	Unit	Note
OSC1 input clock time	Cycle time	t_{O1CY}	12		32	µS	
	"H" pulse width	t_{O1H}	6		16	µS	
	"L" pulse width	t_{O1L}	6		16	µS	
OSC3 input clock time	Cycle time	t_{O3CY}	250		32,000	nS	
	"H" pulse width	t_{O3H}	125		16,000	nS	
	"L" pulse width	t_{O3L}	125		16,000	nS	
Input clock rising time		t_{OSR}			25	nS	
Input clock falling time		t_{OSF}			25	nS	

• OSC1, OSC3 external clock (High speed operating mode)

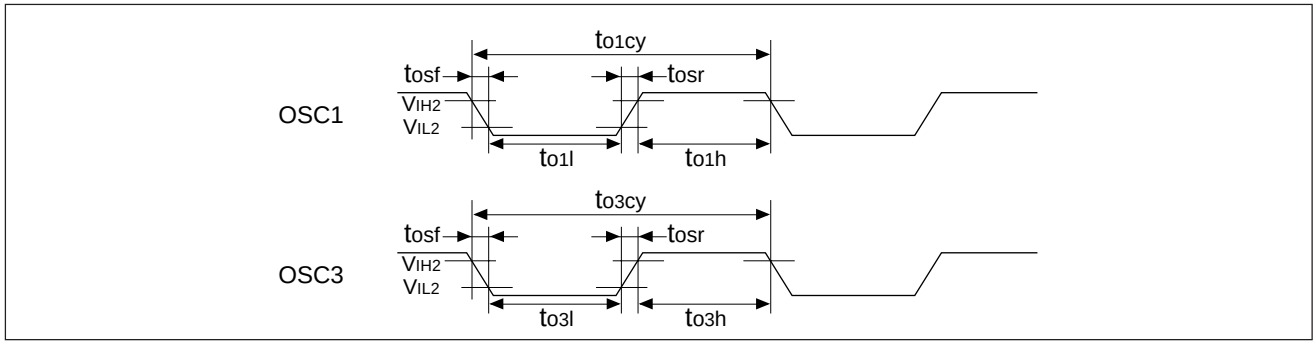
(Condition: V_{DD}=3.5 to 5.5V, V_{SS}=0V, Ta=-40 to 85°C, V_{IH2}=1.6V, V_{IL2}=0.6V)

Item		Symbol	Min.	Typ.	Max.	Unit	Note
OSC1 input clock	Cycle time	t_{O1CY}	12		32	µS	
	"H" pulse width	t_{O1H}	6		16	µS	
	"L" pulse width	t_{O1L}	6		16	µS	
OSC3 input clock time	Cycle time	t_{O3CY}	125		32,000	nS	
	"H" pulse width	t_{O3H}	62.5		16,000	nS	
	"L" pulse width	t_{O3L}	62.5		16,000	nS	
Input clock rising time		t_{OSR}			25	nS	
Input clock falling time		t_{OSF}			25	nS	

• OSC1 external clock (Low power operating mode)

(Condition: V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=-40 to 85°C, V_{IH2}=1.0V, V_{IL2}=0.3V)

Item		Symbol	Min.	Typ.	Max.	Unit	Note
OSC1 input clock time	Cycle time	t_{O1CY}	12		32	µS	
	"H" pulse width	t_{O1H}	6		16	µS	
	"L" pulse width	t_{O1L}	6		16	µS	
Input clock rising time		t_{OSR}			25	nS	
Input clock falling time		t_{OSF}			25	nS	



• $\overline{\text{SCLK}}$, EVIN input clock (Normal operating mode)

(Condition: V_{DD}=2.4 to 5.5V, V_{SS}=0V, Ta=-40 to 85°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD})

Item		System	Min.	Typ.	Max.	Unit	Note
$\overline{\text{SCLK}}$ input clock time	Cycle time	t_{SCCY}	4			µS	
	"H" pulse width	t_{SCH}	2			µS	
	"L" pulse width	t_{SCL}	2			µS	
EVIN input clock time (With noise rejector)	Cycle time	t_{EVCY}	64/f_{OSC1}			S	
	"H" pulse width	t_{EVH}	32/f_{OSC1}			S	
	"L" pulse width	t_{EVL}	32/f_{OSC1}			S	
EVIN input clock time (Without noise rejector)	Cycle time	t_{EVCY}	4			µS	
	"H" pulse width	t_{EVH}	2			µS	
	"L" pulse width	t_{EVL}	2			µS	
Input clock rising time		t_{CKR}			25	nS	
Input clock falling time		t_{CKF}			25	nS	

• $\overline{\text{SCLK}}$, EVIN input clock (High speed operating mode)

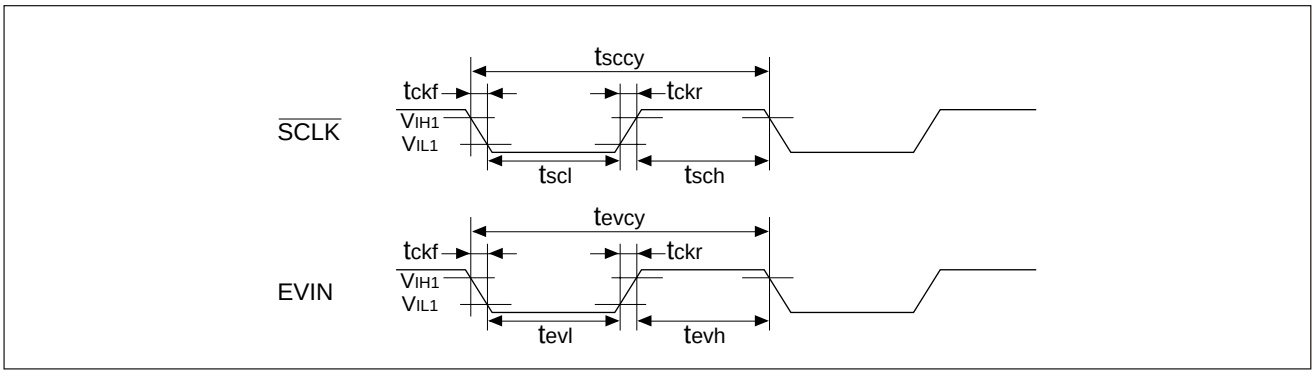
(Condition: V_{DD}=3.5 to 5.5V, V_{SS}=0V, Ta=-40 to 85°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD})

Item		System	Min.	Typ.	Max.	Unit	Note
$\overline{\text{SCLK}}$ input clock time	Cycle time	tsccy	2			µS	
	"H" pulse width	tsch	1			µS	
	"L" pulse width	tscl	1			µS	
EVIN input clock time (With noise rejector)	Cycle time	tevcy	64/f_{OSC1}			S	
	"H" pulse width	tevh	32/f_{OSC1}			S	
	"L" pulse width	tevl	32/f_{OSC1}			S	
EVIN input clock time (Without noise rejector)	Cycle time	tevcy	2			µS	
	"H" pulse width	tevh	1			µS	
	"L" pulse width	tevl	1			µS	
Input clock rising time		tckr			25	nS	
Input clock falling time		tckf			25	nS	

• $\overline{\text{SCLK}}$, EVIN input clock (Low power operating mode)

(Condition: V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=-40 to 85°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD})

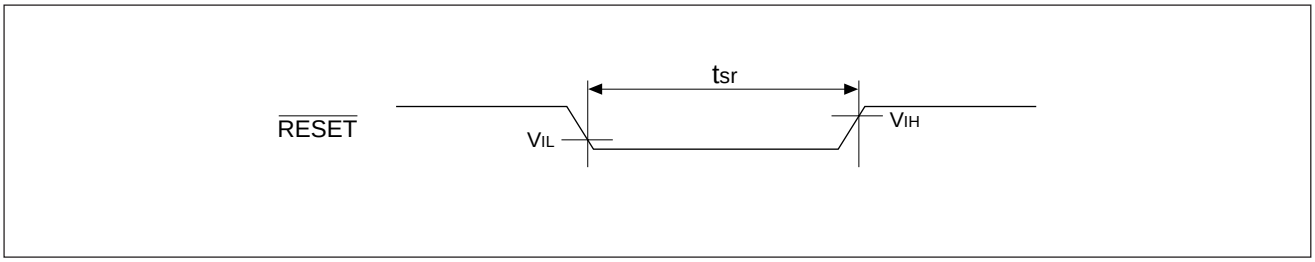
Item		Symbol	Min.	Typ.	Max.	Unit	Note
$\overline{\text{SCLK}}$ input clock time	Cycle time	tsccy	100			µS	
	"H" pulse width	tsch	50			µS	
	"L" pulse width	tscl	50			µS	
EVIN input clock time (With noise rejector)	Cycle time	tevcy	64/f_{OSC1}			S	
	"H" pulse width	tevh	32/f_{OSC1}			S	
	"L" pulse width	tevl	32/f_{OSC1}			S	
EVIN input clock time (Without noise rejector)	Cycle time	tevcy	100			µS	
	"H" pulse width	tevh	50			µS	
	"L" pulse width	tevl	50			µS	
Input clock rising time		tckr			25	nS	
Input clock falling time		tckf			25	nS	



• $\overline{\text{RESET}}$ input clock (All operating mode)

(Condition: V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=-40 to 85°C, V_{IH}=0.5V_{DD}, V_{IL}=0.1V_{DD})

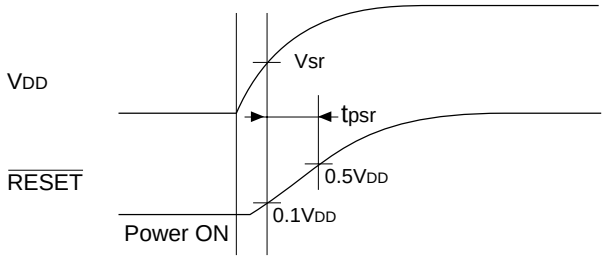
Item	Symbol	Min.	Typ.	Max.	Unit	Note
$\overline{\text{RESET}}$ input time	tsr	100			µS	

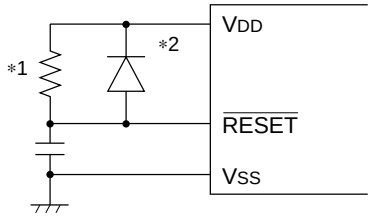


Power ON reset

(Condition: V_{SS}=0V, Ta=-40 to 85°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Operating power voltage	Vsr	2.4			V	
$\overline{RESET}$ input time	tpsr	10			mS	





*1 When the built-in pull up resistor is not used.
*2 Because the potential of the $\overline{RESET}$ terminal not reached V_{DD} level or higher.

Operating mode switching

(Condition: V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=-40 to 85°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Stabilization time	tvdc	5			mS	1

Note) 1 Stabilization time is the time from switching on the operating mode until operating mode is stabilized. For example, when turning the OSC3 oscillation circuit on, stabilization time is needed after the operating mode is switched on.

● Oscillation Characteristics

Oscillation characteristics change depending on conditions (board pattern, components used, etc.). Use the following characteristics as reference values. In particular, when a ceramic oscillator is used for OSC3, use the oscillator manufacturer's recommended values for constants such as capacitance and resistance. The oscillation start time is important because it becomes the wait time when OSC3 clock is used. (If OSC3 is used as CPU clock before oscillation stabilizes, the CPU may malfunction.)

OSC1 (Crystal)

(Unless otherwise specified: V_{DD}=Within the operating voltage in each operating mode, V_{SS}=0V, Ta=25°C, Crystal oscillator=Q12C2*, C_{G1}=25pF (external), C_{D1}=Built-in)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time	tsta				3	S	
External gate capacitance	C_{G1}	Including board capacitance	5		30	pF	1
Built-in gate capacitance	C_{G1}	In case of the chip		12		pF	2
Built-in drain capacitance	C_{D1}	In case of the chip		12		pF	
Frequency/IC deviation	∂f/∂IC	V_{DD} = constant	-10		10	ppm	
Frequency/power voltage deviation	∂f/∂V				1	ppm/V	
Frequency adjustment range	∂f/∂C_G	V_{DD} = constant, C_G = 5 to 30 pF	25	55		ppm	1
Frequency/operating mode deviation	∂f/∂MD	V_{DD} = constant			20	ppm	

* Q12C2 Made by Seiko Epson corporation

Note) 1 When crystal oscillation (external gate capacitor type) is selected by mask option.
2 When crystal oscillation (gate capacitor built-in type) is selected by mask option.

OSC1 (CR)

(Unless otherwise specified: V_{DD}=2.4 to 5.5V, V_{SS}=0V, Ta=-40 to 85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time	tsta				3	mS	
Frequency/IC deviation	∂f/∂IC	R_{CR} = constant	-25		25	%	

OSC3 (Crystal)

(Unless otherwise specified: V_{DD}=Within the operating voltage in each operating mode, V_{SS}=0V, Ta=25°C, Crystal oscillator=Q21CA301xxx*, R_F=1MΩ, C_{G2}=C_{D2}=15pF)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time (Normal mode)	tsta	4.0 MHz crystal oscillator			20	mS	1
Oscillation start time (High speed mode)	tsta	8.0 MHz crystal oscillator			20	mS	1

* Q21CA301xxx Made by Seiko Epson corporation

Note) 1 The crystal oscillation start time changes by the crystal oscillator to be used, C_{G2} and C_{D2}.

OSC3 (Ceramic)

(Unless otherwise specified: V_{DD}=Within the operating voltage in each operating mode, V_{SS}=0V, Ta=25°C, Ceramic oscillator=CSA4.00MG / CSA8.00MTZ*, R_F=1MΩ, C_{G2}=C_{D2}=30pF)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time (Normal mode)	tsta	4.0 MHz ceramic oscillator			5	mS	
Oscillation start time (High speed mode)	tsta	8.0 MHz ceramic oscillator			5	mS	

* CSA4.00MG / CSA8.00MTZ Made by Murata Mfg. corporation

OSC3 (CR)

(Unless otherwise specified: V_{DD}=Within the operating voltage in each operating mode, V_{SS}=0V, Ta=-40 to 85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time (Normal mode)	tsta				1	mS	
Oscillation start time (High speed mode)	tsta				1	mS	
Frequency/IC deviation (Normal mode)	∂f/∂IC	R_{CR} = constant	-25		25	%	
Frequency/IC deviation (High speed mode)	∂f/∂IC	R_{CR} = constant	-25		25	%	

● A/D Converter Characteristics

The following characteristics apply to the plastic package model only.

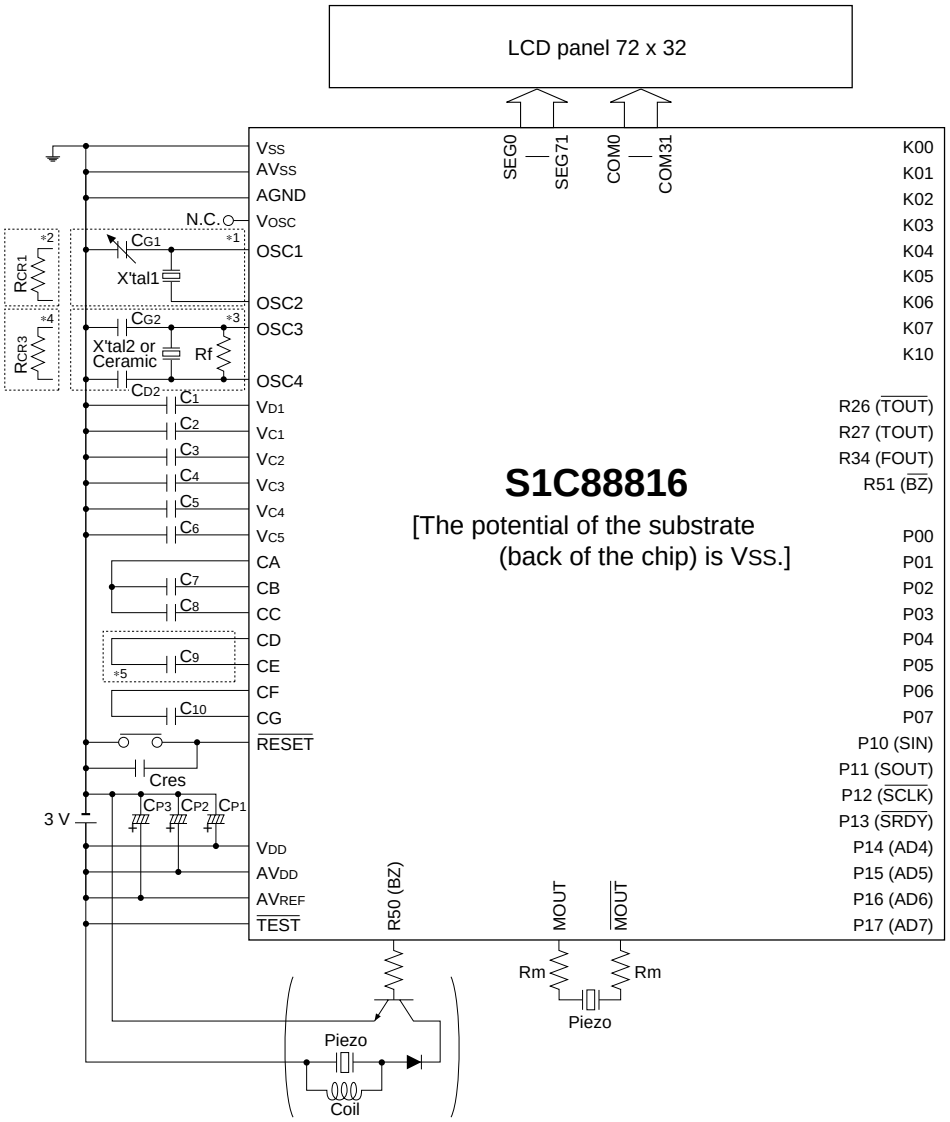
(Unless otherwise specified: V_{DD}=AV_{DD}=AV_{REF}=5.0V, V_{SS}=AV_{SS}=AGND=0V, f_{OSC1}=32.768kHz, f_{OSC3}=4.0MHz, Ta=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Zero-scale error	Ezs	V_{DD}=AV_{DD}=AV_{REF}=2.7 to 5.5V, ADCLK=2MHz, Ta=25°C	-1.50		1.50	LSB	
Full-scale error	Efs		-1.50		1.50	LSB	
Non-linearity error	El		-1.50		1.50	LSB	
Total error	Et		-3.00		3.00	LSB	
A/D converter current consumption	I_{AD}	V_{DD}=AV_{DD}=AV_{REF}=3.0V, ADCLK=2MHz, Ta=25°C AV_{REF} and ADCLK divider current not included		0.50	1.00	mA	
		V_{DD}=AV_{DD}=AV_{REF}=5.0V, ADCLK=2MHz, Ta=25°C AV_{REF} and ADCLK divider current not included		1.80	3.50	mA	
Input clock frequency	f	V_{DD}=AV_{DD}=AV_{REF}=2.7 to 3.0 V, Ta=25°C			2	MHz	
		V_{DD}=AV_{DD}=AV_{REF}=3.0 to 5.5 V, Ta=25°C			4	MHz	

* Zero-scale error: Ezs = deviation from the ideal value at zero point
* Full-scale error: Efs = deviation from the ideal value at the full scale point
* Non-linearity error: El = deviation of the real conversion curve from the end point line
* Total error: Et = max(Ezs, Efs, Eabs), Eabs = deviation from the ideal line (including quantization error)

■ BASIC EXTERNAL CONNECTION DIAGRAM

● **When V_{C2} standard and 1/5 bias are selected**



Recommended values for external parts

Symbol	Name	Recommended value
X'tal1	Crystal oscillator	32.768 kHz, CI(Max.)=35 kΩ
C_{G1}	Trimmer capacitor	5–30 pF
R_{CR1}	Resistor for CR oscillation	1 MΩ
X'tal2	Crystal oscillator	4 MHz
Ceramic	Ceramic oscillator	4 MHz
Rf	Feedback resistor	1 MΩ
C_{G2}	Gate capacitor	15 pF (Crystal oscillator) 30 pF (Ceramic oscillator)
C_{D2}	Drain capacitor	15 pF (Crystal oscillator) 30 pF (Ceramic oscillator)
R_{CR3}	Resistor for CR oscillation	20 kΩ

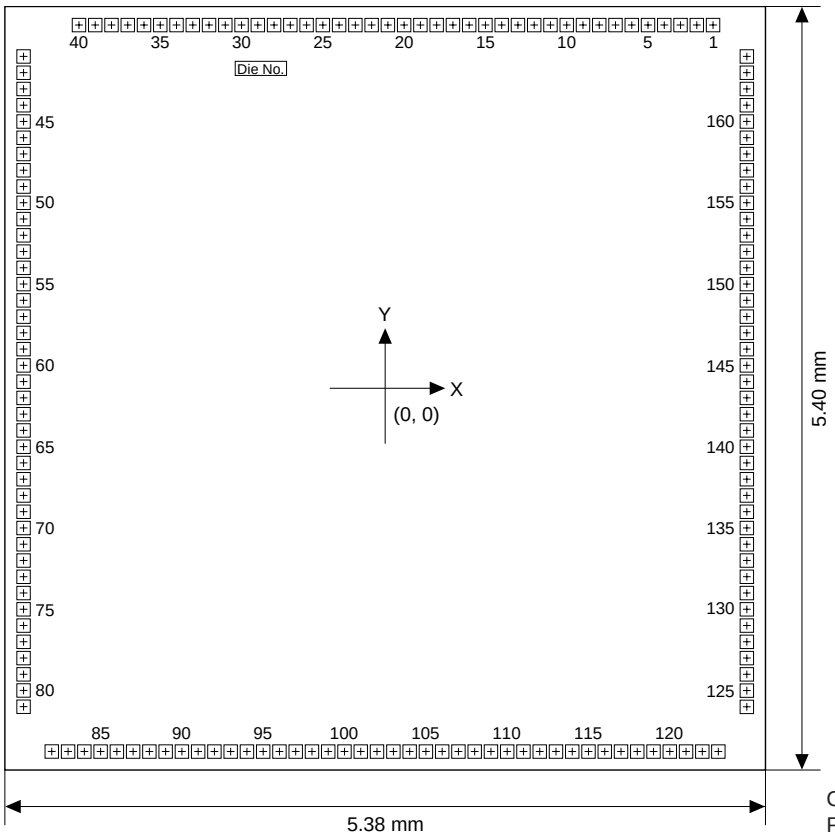
Symbol	Name	Recommended value
C_1	Capacitor between V_{SS} and V_{D1}	0.1 µF
C_2	Capacitor between V_{SS} and V_{C1}	0.1 µF
C_3	Capacitor between V_{SS} and V_{C2}	0.1 µF
C_4	Capacitor between V_{SS} and V_{C3}	0.1 µF
C_5	Capacitor between V_{SS} and V_{C4}	0.1 µF
C_6	Capacitor between V_{SS} and V_{C5}	0.1 µF
C_7–C_{10}	Booster/reducer capacitors	0.1 µF
C_{P1}–C_{P3}	Capacitors for power supply	3.3 µF
Cres	Capacitor for $\overline{\text{RESET}}$ terminal	0.47 µF
Rm	Protective resistors for piezo	100 Ω

∗ The connection diagram shown above is an example of when mask option settings are as follows:
LCD power source: Internal power supply, $\overline{\text{RESET}}$ terminal: With pull-up resistor,
R51 specification: General-purpose output port

∗1 OSC1 = Crystal oscillation, ∗2 OSC1 = CR oscillation, ∗3 OSC3 = Crystal/Ceramic oscillation, ∗4 OSC3 = CR oscillation,
∗5 Unnecessary for 1/4 bias drive

Note: The above table is simply an example, and is not guaranteed to work.

■ DIAGRAM OF PAD LAYOUT



Chip thickness: 0.4 mm
Pad opening: 95 µm

■ PAD COORDINATES

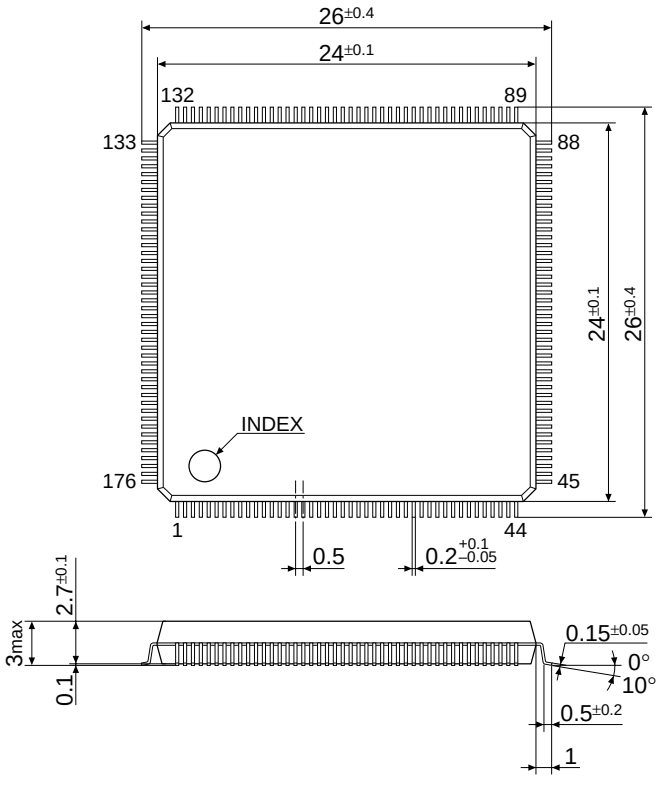
Pad No.	Pad name	X	Y	Pad No.	Pad name	X	Y	Pad No.	Pad name	X	Y
1	V_{C3}	2,319	2,569	27	P13/$\overline{SRDY}$	-671	2,569	53	COM3	-2,558	-2,558
2	V_{C2}	2,204	2,569	28	P12/$\overline{SCLK}$	-786	2,569	54	COM4	-2,558	-2,558
3	V_{C1}	2,089	2,569	29	P11/SOUT	-901	2,569	55	COM5	-2,558	-2,558
4	OSC3	1,974	2,569	30	P10/SIN	-1,016	2,569	56	COM6	2,558	622
5	OSC4	1,859	2,569	31	AV_{DD}	-1,131	2,569	57	COM7	-2,558	507
6	V_{D1}	1,744	2,569	32	AGND	-1,246	2,569	58	COM8	-2,558	392
7	V_{DD}	1,629	2,569	33	AV_{SS}	-1,361	2,569	59	COM9	-2,558	277
8	V_{SS}	1,514	2,569	34	AV_{REF}	-1,476	2,569	60	COM10	-2,558	162
9	V_{OSC}	1,399	2,569	35	P07	-1,591	2,569	61	COM11	-2,558	47
10	OSC1	1,284	2,569	36	P06	-1,706	2,569	62	COM12	-2,558	-68
11	OSC2	1,169	2,569	37	P05	-1,821	2,569	63	COM13	-2,558	-183
12	$\overline{TEST}$	1,054	2,569	38	P04	-1,936	2,569	64	COM14	-2,558	-298
13	$\overline{RESET}$	939	2,569	39	P03	-2,051	2,569	65	COM15	-2,558	-413
14	K10/EVIN	824	2,569	40	P02	-2,166	2,569	66	SEG0	-2,558	-528
15	K07	709	2,569	41	P01	-2,558	-2,558	67	SEG1	-2,558	-643
16	K06	594	2,569	42	P00	-2,558	-2,558	68	SEG2	-2,558	-758
17	K05	479	2,569	43	MOUT	-2,558	-2,558	69	SEG3	-2,558	-873
18	K04	364	2,569	44	$\overline{MOUT}$	-2,558	-2,558	70	SEG4	-2,558	-988
19	K03	249	2,569	45	R26/$\overline{TOUT}$	-2,558	-2,558	71	SEG5	-2,558	-1,103
20	K02	134	2,569	46	R27/TOUT	-2,558	-2,558	72	SEG6	-2,558	-1,218
21	K01	19	2,569	47	R34/FOUT	-2,558	-2,558	73	SEG7	-2,558	-1,333
22	K00	-96	2,569	48	R50/BZ	-2,558	-2,558	74	SEG8	-2,558	-1,448
23	P17/AD7	-211	2,569	49	R51/$\overline{BZ}$	-2,558	-2,558	75	SEG9	-2,558	-1,563
24	P16/AD6	-326	2,569	50	COM0	-2,558	-2,558	76	SEG10	-2,558	-1,678
25	P15/AD5	-441	2,569	51	COM1	-2,558	-2,558	77	SEG11	-2,558	-1,793
26	P14/AD4	-556	2,569	52	COM2	-2,558	-2,558	78	SEG12	-2,558	-1,908

Pad No.	Pad name	X	Y	Pad No.	Pad name	X	Y	Pad No.	Pad name	X	Y
79	SEG13	-2,558	-2,023	108	SEG41	633	-2,569	137	SEG69	2,558	-758
80	SEG14	-2,558	-2,137	109	SEG42	748	-2,569	138	SEG70	2,558	-643
81	SEG15	-2,558	-2,252	110	SEG43	863	-2,569	139	SEG71	2,558	-528
82	*	*	*	111	SEG44	978	-2,569	140	COM31/SEG72	2,558	-413
83	SEG16	-2,243	-2,569	112	SEG45	1,093	-2,569	141	COM30/SEG73	2,558	-298
84	SEG17	-2,128	-2,569	113	SEG46	1,208	-2,569	142	COM29/SEG74	2,558	-183
85	SEG18	-2,013	-2,569	114	SEG47	1,323	-2,569	143	COM28/SEG75	2,558	-68
86	SEG19	-1,898	-2,569	115	SEG48	1,438	-2,569	144	COM27/SEG76	2,558	47
87	SEG20	-1,783	-2,569	116	SEG49	1,553	-2,569	145	COM26/SEG77	2,558	162
88	SEG21	-1,668	-2,569	117	SEG50	1,668	-2,569	146	COM25/SEG78	2,558	277
89	SEG22	-1,553	-2,569	118	SEG51	1,783	-2,569	147	COM24/SEG79	2,558	392
90	SEG23	-1,438	-2,569	119	SEG52	1,898	-2,569	148	COM23/SEG80	2,558	507
91	SEG24	-1,323	-2,569	120	SEG53	2,013	-2,569	149	COM22/SEG81	2,558	622
92	SEG25	-1,208	-2,569	121	SEG54	2,128	-2,569	150	COM21/SEG82	2,558	737
93	SEG26	-1,093	-2,569	122	SEG55	2,243	-2,569	151	COM20/SEG83	2,558	852
94	SEG27	-978	-2,569	123	*	*	*	152	COM19/SEG84	2,558	967
95	SEG28	-863	-2,569	124	SEG56	2,558	2,253	153	COM18/SEG85	2,558	1,082
96	SEG29	-748	-2,569	125	SEG57	2,558	-2,138	154	COM17/SEG86	2,558	1,197
97	SEG30	-633	-2,569	126	SEG58	2,558	-2,023	155	COM16/SEG87	2,558	1,312
98	SEG31	-518	-2,569	127	SEG59	2,558	-1,908	156	CG	2,558	1,427
99	SEG32	-403	-2,569	128	SEG60	2,558	-1,793	157	CF	2,558	1,542
100	SEG33	-288	-2,569	129	SEG61	2,558	-1,678	158	CE	2,558	1,657
101	SEG34	-173	-2,569	130	SEG62	2,558	-1,563	159	CD	2,558	1,772
102	SEG35	-58	-2,569	131	SEG63	2,558	-1,448	160	CC	2,558	1,887
103	SEG36	58	-2,569	132	SEG64	2,558	-1,333	161	CB	2,558	2,002
104	SEG37	173	-2,569	133	SEG65	2,558	-1,218	162	CA	2,558	2,117
105	SEG38	288	-2,569	134	SEG66	2,558	-1,103	163	V_{C5}	2,558	2,232
106	SEG39	403	-2,569	135	SEG67	2,558	-988	164	V_{C4}	2,558	2,347
107	SEG40	518	-2,569	136	SEG68	2,558	-873				

* Do not bond No.82 and 123 pads since they are used for factory inspection at shipment.

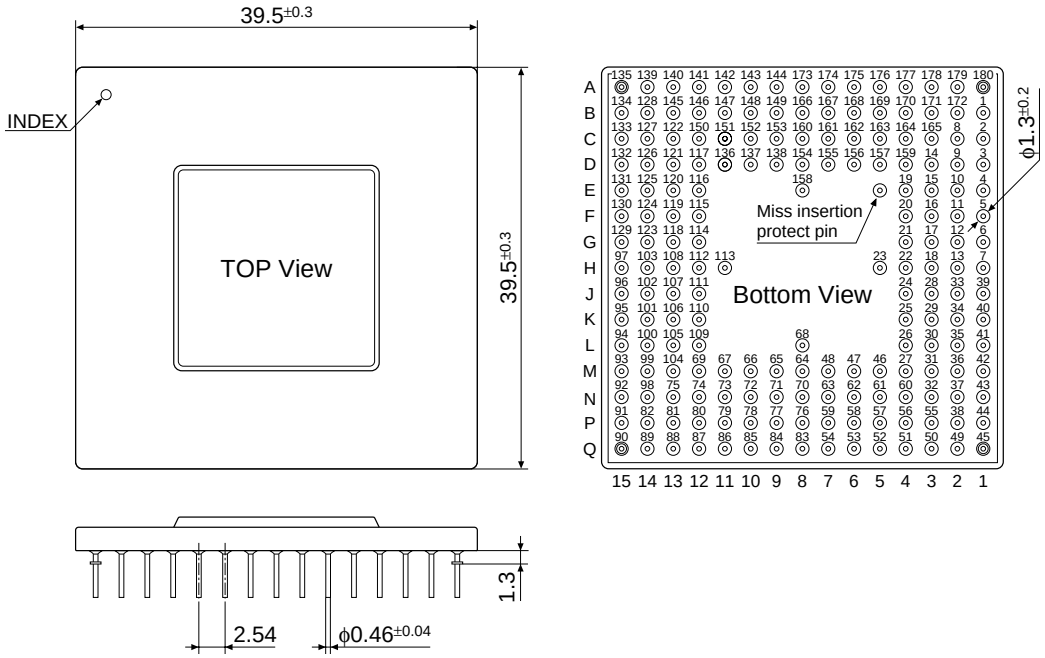
■ PACKAGE DIMENSIONS

Plastic QFP18-176pin



Unit: mm

Ceramic PGA-181pin



Unit: mm

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	N.C.	37	SEG49	73	COM22/SEG81	109	K06	145	R50/BZ
2	N.C.	38	SEG50	74	COM21/SEG82	110	K05	146	R51/$\overline{BZ}$
3	N.C.	39	SEG51	75	COM20/SEG83	111	K04	147	COM0
4	SEG16	40	SEG52	76	COM19/SEG84	112	K03	148	COM1
5	SEG17	41	SEG53	77	COM18/SEG85	113	K02	149	COM2
6	SEG18	42	SEG54	78	COM17/SEG86	114	K01	150	COM3
7	SEG19	43	SEG55	79	COM16/SEG87	115	K00	151	COM4
8	SEG20	44	N.C.	80	CG	116	P17/AD7	152	COM5
9	SEG21	45	N.C.	81	CF	117	P16/AD6	153	COM6
10	SEG22	46	N.C.	82	CE	118	P15/AD5	154	COM7
11	SEG23	47	N.C.	83	CD	119	P14/AD4	155	COM8
12	SEG24	48	SEG56	84	CC	120	P13/$\overline{SRDY}$	156	COM9
13	SEG25	49	SEG57	85	CB	121	P12/$\overline{SCLK}$	157	COM10
14	SEG26	50	SEG58	86	CA	122	P11/SOUT	158	COM11
15	SEG27	51	SEG59	87	V_{C5}	123	P10/SIN	159	COM12
16	SEG28	52	SEG60	88	V_{C4}	124	AV_{DD}	160	COM13
17	SEG29	53	SEG61	89	N.C.	125	AGND	161	COM14
18	SEG30	54	SEG62	90	N.C.	126	AV_{SS}	162	COM15
19	SEG31	55	SEG63	91	N.C.	127	AV_{REF}	163	SEG0
20	SEG32	56	SEG64	92	N.C.	128	P07	164	SEG1
21	SEG33	57	SEG65	93	N.C.	129	P06	165	SEG2
22	SEG34	58	SEG66	94	V_{C3}	130	P05	166	SEG3
23	SEG35	59	SEG67	95	V_{C2}	131	P04	167	SEG4
24	SEG36	60	SEG68	96	V_{C1}	132	P03	168	SEG5
25	SEG37	61	SEG69	97	OSC3	133	P02	169	SEG6
26	SEG38	62	SEG70	98	OSC4	134	N.C.	170	SEG7
27	SEG39	63	SEG71	99	V_{D1}	135	N.C.	171	SEG8
28	SEG40	64	COM31/SEG72	100	V_{DD}	136	N.C.	172	SEG9
29	SEG41	65	COM30/SEG73	101	V_{SS}	137	N.C.	173	SEG10
30	SEG42	66	COM29/SEG74	102	V_{OSC}	138	P01	174	SEG11
31	SEG43	67	COM28/SEG75	103	OSC1	139	P00	175	SEG12
32	SEG44	68	COM27/SEG76	104	OSC2	140	MOUT	176	SEG13
33	SEG45	69	COM26/SEG77	105	$\overline{TEST}$	141	$\overline{MOUT}$	177	SEG14
34	SEG46	70	COM25/SEG78	106	$\overline{RESET}$	142	R26/$\overline{TOUT}$	178	SEG15
35	SEG47	71	COM24/SEG79	107	K10/EVIN	143	R27/TOUT	179	N.C.
36	SEG48	72	COM23/SEG80	108	K07	144	R34/FOUT	180	N.C.

N.C.: No Connection

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