10 bit PWM controller
/ 48 Channel Output LED DRIVER

LD71D1048C

Data Sheet

2005. 1

DESCRIPTION

The LD71D1048C is LED driver / controller IC for LED display panel. This is consisted of 48 channel LED driver , 10Bit PWM controller and 48 bit shift register. Also it is very convenient to application because all display data can be transferred by serial method.

MQFP-128

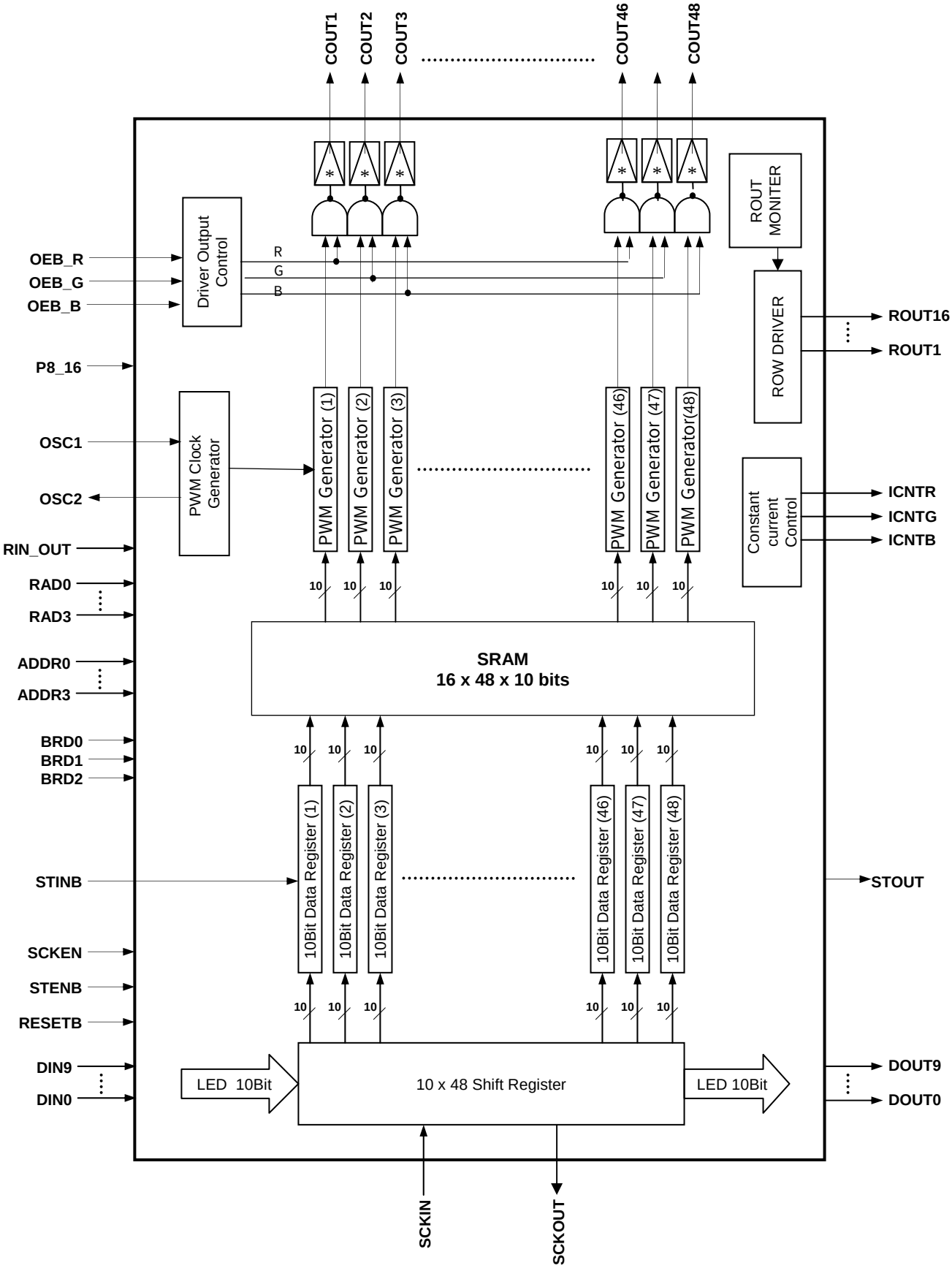
FEATURES

- **DRIVER OUTPUT CIRCUITS**
  - 48 Column Driver Outputs : N-ch Open Drain MOS Transistor Output
  - 16 Row Driver Outputs : CMOS Output
  - LED Driving Voltage : Max. 5V (When Transistor Off)
  - LED Driving Current : Max. 60mA
  - LED Driving Current Control
  - Outputs are 10Bit PWM controlled
  - ROUT Monitoring
  - ROUT External selectable
  - A Little change of Output Current

OUT-GND VOLTAGE	A LITTLE CHANGE OF CHANNEL	IOUT (mA)
≧ 0.7V	± 4%	5mA ~30mA
≧ 1.0V		5mA ~60mA

- **DATA INTERFACE**
  - 48bit Shift Register for 10Bit data input
  - 10Bit parallel data format selectable
- **DISPLAY DATA MEMORY**
  - 7,680 bit SRAM
- **PWM CONTROLLER**
  - 10Bit PWM control (1024 Gray scale)
  - 3bit Brightness control
  - PWM pulse width control
- **ON CHIP OPAMP FOR LED DRIVING CURRENT CONTROL**
- **LOW POWER CONSUMPTION**
- **PACKAGE TYPE**
  - 128 pin HMQFP(Heat Sink Package)
    Continuous Power Dissipation = 2W
  - 128 pin MQFP
    Continuous Power Dissipation = 0.5W

BLOCK DIAGRAM



PIN CONNECTIONS(MQFP)

PIN DESCRIPTION

PIN No. (MQFP)	PIN NAME	DESCRIPTION
56, 121	VDD	5V Power supply terminal.
11, 16, 21, 40, 43, 48, 53, 73, 76,81, 86, 108, 113, 118	GND	GND terminals for LED Drivers and control logic. All GND terminals must be connected to GND level. Do not leave any GND terminal to NC.
99	RESETB	Reset input terminal (Low active). This Pin reset all register except RAM Area.
8,7, 6, 5, 4, 3, 2,1 128,127	DIN0 ~ DIN9	Data input terminals for 10Bit R, G, B data. Shift register accepts R, G, B data from these terminals. (at rising edge of SCKIN)
25,26,27,28 29,30,31,32, 33,34	DOUT0 ~ DOUT9	Output terminals of shift register output data for next DIN9 ~ DIN0 terminals.
126	SCKIN	Shift register clock input terminal.
24	SCKOUT	Shift register clock out terminal.
125	STINB	Strobe signal input terminal. At falling edge of strobe signal, 48 channels of 10 bit data registers copy R, G, B data from shift register.
100	STOUT	Strobe signal output terminal.
97	STENB	STINB enable signal input terminal (Low active).
98	SCKEN	SCKIN enable signal input terminal (High active).
35, 36, 37	OEB_R OEB_G OEB_B	Output enable signal input terminal. The device outputs data when OEB = “L”. When OEB = “H” all R, G, B output terminals hold high-impedance state. OEB_R, OEB_G, OEB_B work indepantant respectively. R pin : COUT1,4,7,10,13,16,19,22,25,28,31,34,37,40,43,46 G pin : COUT2,5,8,11,14,17,20,23,26,29,32,35,38,41,44,47 B pin : COUT3,6,9,12,15,18,21,24,27,30,33,36,39,42,45,48
39	OSC1	PWM generator reference clock input terminal.
38	OSC2	PWM generator reference clock output terminal.

PIN DESCRIPTION (continued)

PIN No. (MQFP)	PIN NAME	DESCRIPTION
62,63,64	BRD0 ~ BRD2	Brightness control input selection terminal.
93,94,95,96	ADDR0 ~ 3	SRAM address
122,123,124	INCTR INCTG INCTB	R,G,B current control pin. It is connected GND with resistor R pin : COUT1,4,7,10,13,16,19,22,25,28,31,34,37,40,43,46 G pin : COUT2,5,8,11,14,17,20,23,26,29,32,35,38,41,44,47 B pin : COUT3,6,9,12,15,18,21,24,27,30,33,36,39,42,45,48
92	P8_16	P8_16=0, ROUT1 ~ ROUT8 Enable, P8_16 = 1, ROUT1~ROUT16 Enable when RIN_OUT = “L”
9,10,12,13, 14,15,17,18, 19,20,22,23, 41,42,44,45, 46,47,49,50, 51,52,54,55, 74,75,77,78, 79,80,82,83, 84,85,87,88, 106,107,109,110, 111,112,114,115, 116,117,119,120	COUT1 ~ 48	LED driver output terminals.
57,58,59,60 61,70,71,72 89,90,91,101 102,103,104,105	ROUT1 ~ 16	Row driver control output signal
66,67,68,69	RAD0 ~ RAD3	ROUT active selection pins
65	RIN_OUT	External or internal ROUT control selection. RIN_OUT = “L” ROUT is doing internal RIN_OUT = “ H” ROUT is dependent on RAD0~3

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

PARAMETER		SYMBOL	RATING	UNIT
Supply Voltage		V_{DD}	0 ~ 7.0	V
Output Voltage (R, G, B)		V_{OUT}	-0.5 ~ 5	V
Output Current (R, G, B)		I_{OUT}	80	mA
Input Voltage		V_{IN}	-0.4 ~ V_{DD} + 0.4	V
GND terminal Current		I_{GND}	1440	mA
Clock Frequency	SCKIN	F_{SCKMAX}	10	MHz
	OSC	F_{OSC}	10	MHz
Power Dissipation		P_D	1.78	W
Operating Temperature		T_{OPR}	-40 ~85	°C
Storage Temperature		T_{STG}	-55 ~ 150	°C

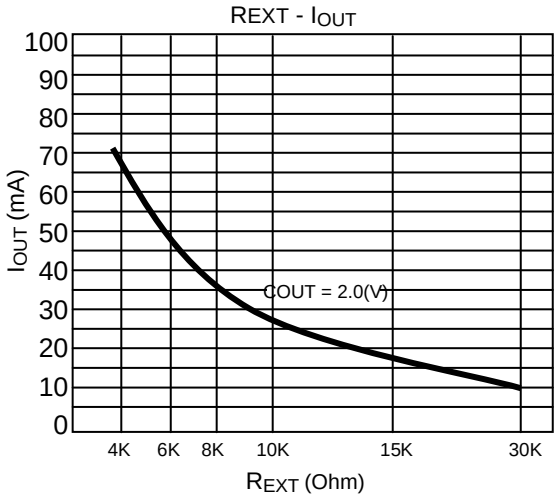
RECOMMENDED OPERATING CONDITION (Ta = 25°C)

PARAMETER		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage		V_{DD}	-	4.5	5.0	5.5	V
Output Voltage (COUT1~48)		V_{OUT}	-	-	-	5.5	V
Output Current	COUT1~ 48	I_{OUT}	-	-	-	60	mA
	DOUT, SCKOUT, STOUT	I_{OH}	-	-	-	-1.0	
		I_{OL}	-	-	-	1.0	
	ROUT1~16	I_{OH}	-	-	-	-1.5	
		I_{OL}	-	-	-	1.5	
Input Voltage		V_{IN}	-	0	-	V_{DD}	V
DIN Data Setup Time		$t_{setup\ (D)}$	-	40	-	-	ns
DIN Data Hold Time		$t_{hold\ (D)}$	-	60	-	-	ns
STINB Setup Time		$t_{STB\ setup}$	-	60	-	-	ns
STINB Hold Time		$t_{STB\ hold}$	-	100	-	-	ns
STINB Width Time		t_{WSL}	-	100	-	-	ns
Pulse Width SCKIN, OSC1		T_{WH}	-	50	-	-	ns
		T_{WL}	-	50	-	-	ns
Clock Frequency	SCKIN	F_{SR}	-	-	-	10	MHz
	OSC	F_{osc}	-	-	-	10	MHz
Power Dissipation(HMQFP)		P_{DH}	-	-	2		W
Power Dissipation(MQFP)		P_{DN}	-	-	0.5		W

ELECTRICAL CHARACTERISTICS (Ta = 25°C unless otherwise noted) (continued)

PARAMETER		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage	"H" Level	V_{IH}	-	-	$0.7V_{DD}$	-	V_{DD}	V
	"L" Level	V_{IL}	-	-	GND	-	$0.3V_{DD}$	
Output Leakage current		I_{OZ}	-	V_{OH} = 6.0V		-	1	uA
Output Voltage	DOUT	V_{OL}	-	-	-	-	$0.2V_{DD}$	V
		V_{OH}	-	-	$0.8V_{DD}$	-	-	
Output Current1		I_{OL1}	-	REXT = 8 kΩ	34	37.0	40.0	mA
	Delta IOUT	I_{OL1}	-	REXT = 16 kΩ IOUT = 40mA, V_{OUT} = 1V	-	± 1.5	± 6.0	%
Output Current2		I_{OL2}	-	REXT = 4.0 kΩ	65.0	69.0	74	mA
	Delta IOUT	I_{OL2}	-	R_{EXT} = 4.0 kΩ I_{OUT} = 69mA, V_{OUT} = 1V	-	± 1.5	± 6.0	%
Supply Voltage Regulation		$\%/V_{DD}$	-	R_{EXT}= 16 kW	-	1.5	5.0	%/V
Reference Voltage		V_{ref}	-	R_{EXT}=4 kΩ ,Ta =-40~85°C	-	1.26	-	V
Pull up resistor		R_{IN}(up)	-	-	100	200	400	kΩ
Pull down resistor		R_{IN}(down)	-	-	100	200	400	
Supply current		Irext(1)	-	R_{EXT} = OPEN, OUTn = OFF	-	-	-	u
		Irext(2)	-	R_{EXT} = 16 kΩ OUTn = OFF	70	74.0	78	uA
		Irext(3)	-	R_{EXT} = 8 kΩ OUTn = OFF	130	140.0	150	

ELECTRICAL CHARACTERISTICS (Ta = 25°C unless otherwise noted)
Relation COUT with REXT



REXT	IOUT
4 kOhm	64mA
6kOhm	46mA
8kOhm	35mA
10 kOhm	29mA
15 kOhm	20mA
30 kOhm	10mA

SWITCHING CHARACTERISTICS (Ta = 25°C)

PARAMETER		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time ("L to "H")	SCKIN-DOUT	t_{PLH}	V_{DD} = 5.0V V_{OUT} = 0.4V V_{CON} = V_{DD} V_{IH} = V_{DD} V_{IL} = GND F_{PWM} = 10MHz I_{OUT} = 40mA	-	5		ns
	SCKIN-SCKOUT			-	5		
	STINB-STOUT			-	5		
	OEB-COUT			-	10		
Propagation Delay Time ("H to "L")		t_{PHL}		-	5		ns
	SCKIN-SCKOUT			-	5		
	STINB-STOUT			-	5		
	OEB-COUT(*1)			-	40	-	
	OEB-COUT(*2)			-	50	-	
	OEB-COUT(*3)			-	60		
	OEB-COUT(*4)			-	100	-	
	OEB-COUT(*5)			-	120	-	
Maximum Clock Frequency	SCKIN	F_{SCKMAX}		-		10	MHz
				-		10	
Minimum Pulse Width	SCKIN	TW_H TW_L		-	50	-	ns
	OSC1			-	50	-	
	STINB	TW_L		-	100	-	
Data Set Up Time		$t_{setup\ (D)}$		-	40		ns
Data Hold Time		$t_{hold\ (D)}$		-	60	-	
STINB Set up Time	LH	t_{STB} setup		50			ns
	HL			50			
STROBE Hold Time	LH	t_{STB} hold		-	100		ns
	HL			-	100		
Maximum SCKIN Rising Time		t_R		-	-	10	us
Maximum SCKIN Falling Time		t_F		-	-	10	
COUT Output Rising Time		t_{OR}		40	50	120	ns
COUT Output Falling Time		t_{OF}		-	10	-	

*1 : When REXT = 4KOhm

*2 : When REXT = 6KOhm

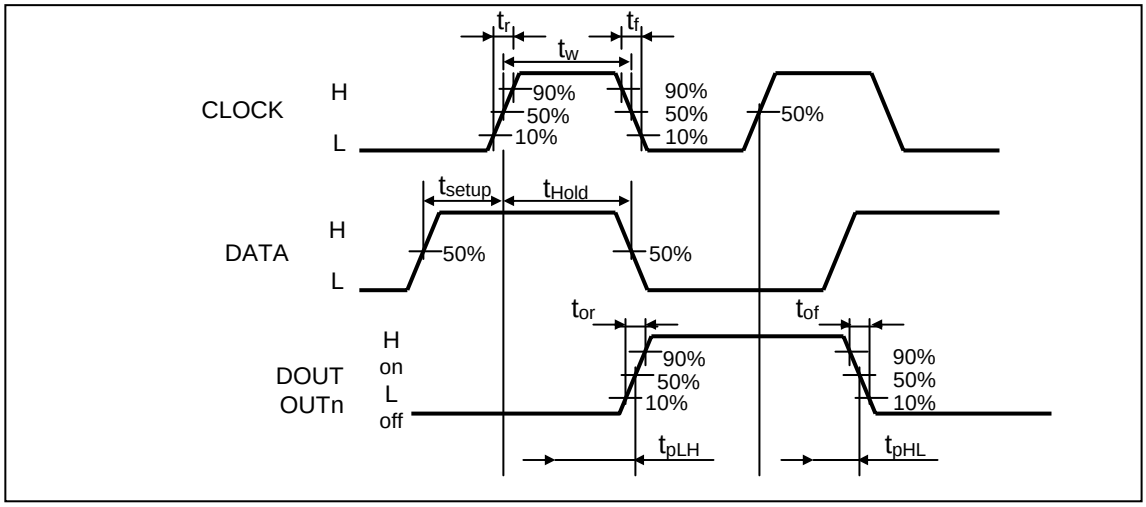
*3 : When REXT = 8KOhm

*4 : When REXT = 15KOhm

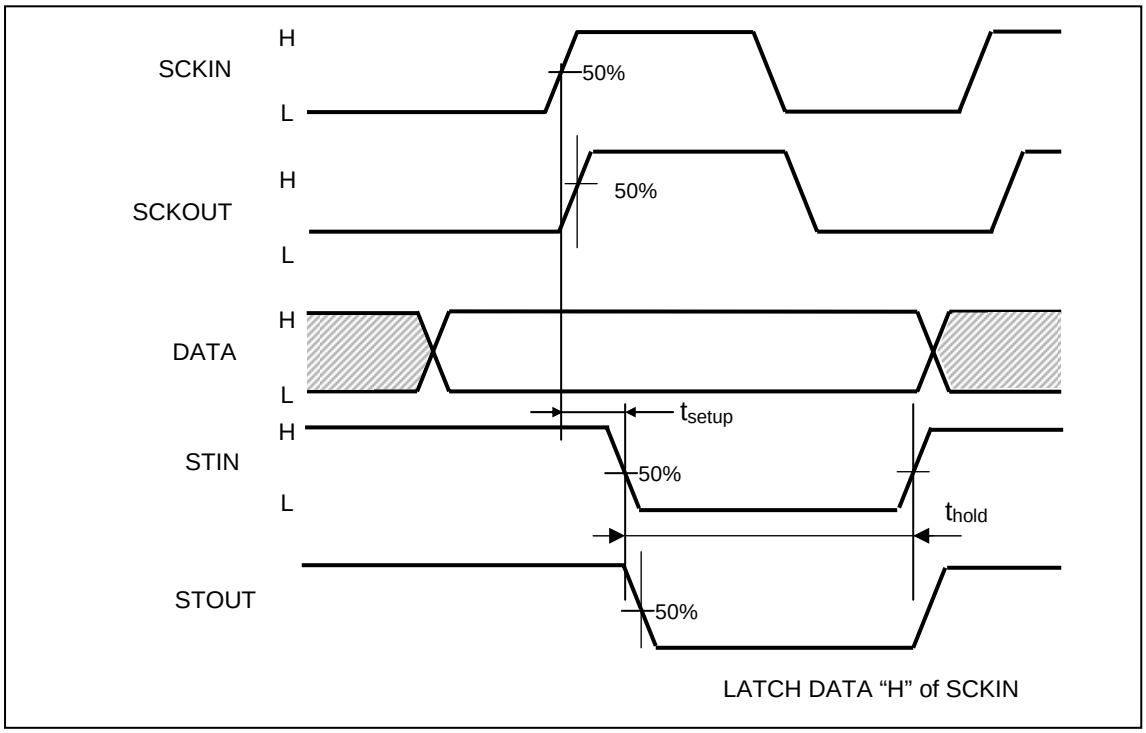
*5 : When REXT = 30KOhm

TIMING WAVE FORM

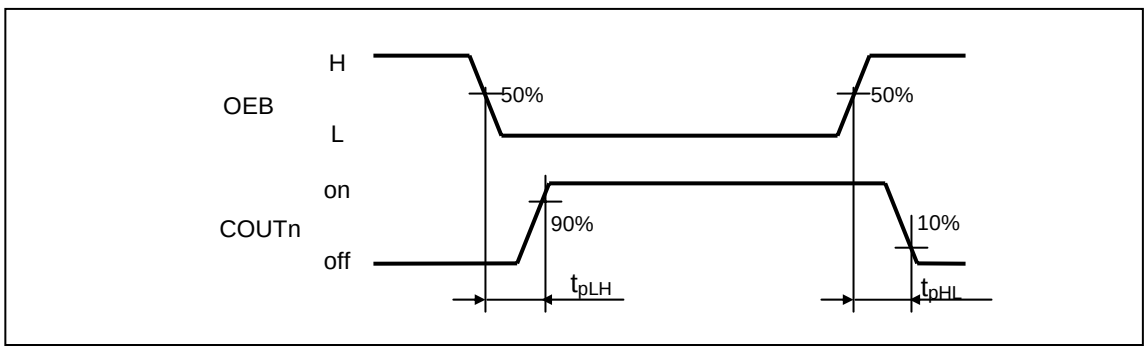
SCKIN-DOUT, OUTn



SCKIN-STIN



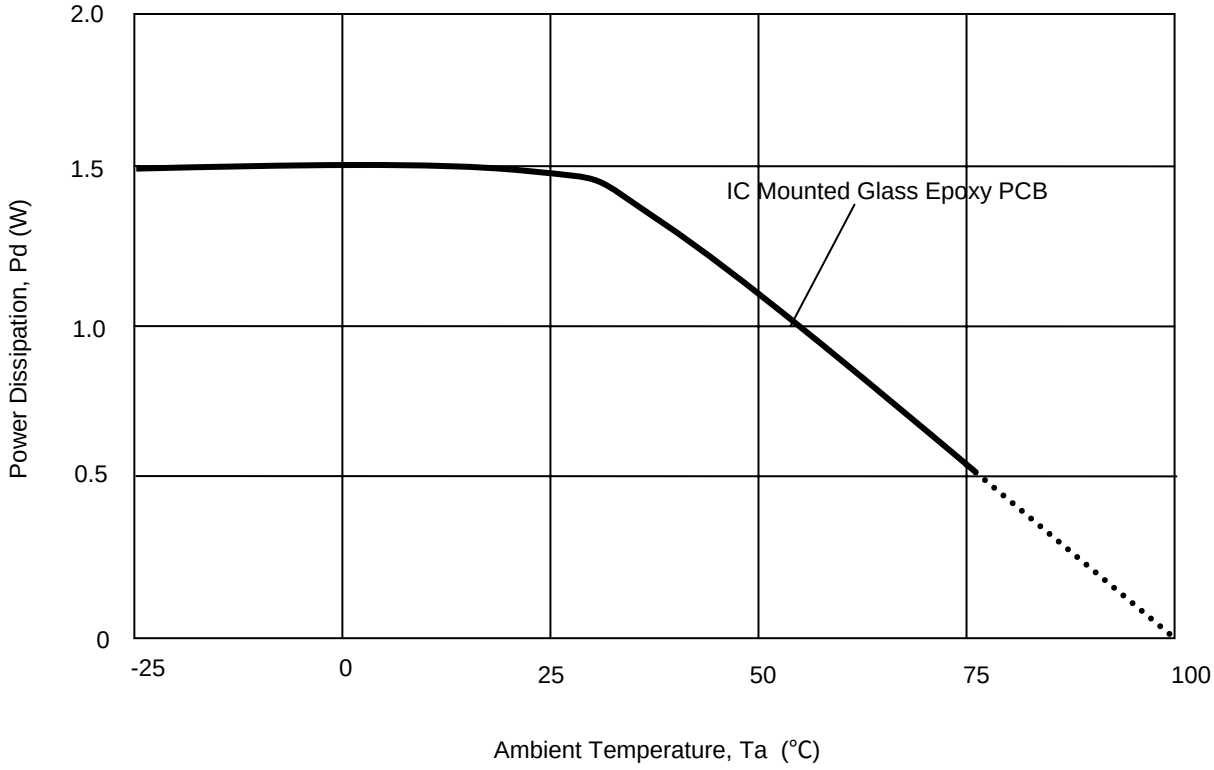
OEB



Package Power Dissipation

The maximum allowable package power dissipation is determined as $P_D(max) = (Tj-Ta)/Rth(j-a)$,
When 48 output channels are tuned on simultaneously, the actual package dissipation is
$P_D(act) = (I_{DD} \times V_{DD}) + (Iout \times V_{DS} \times 48)$
Therefore to keep $P_D(act) <= P_D(max)$, the allowable maximum output current is
$I_{OUT} = \{ [(Tj-Ta) / Rth(j-a)] - (I_{DD} \times V_{DD}) \} / V_{DS} / 48$
Where Tj=150'C

Max. Power Dissipation at Various Ambient Temperature

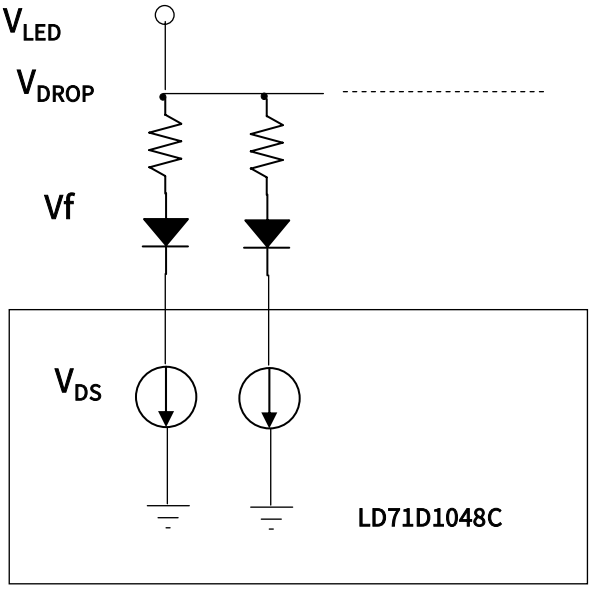


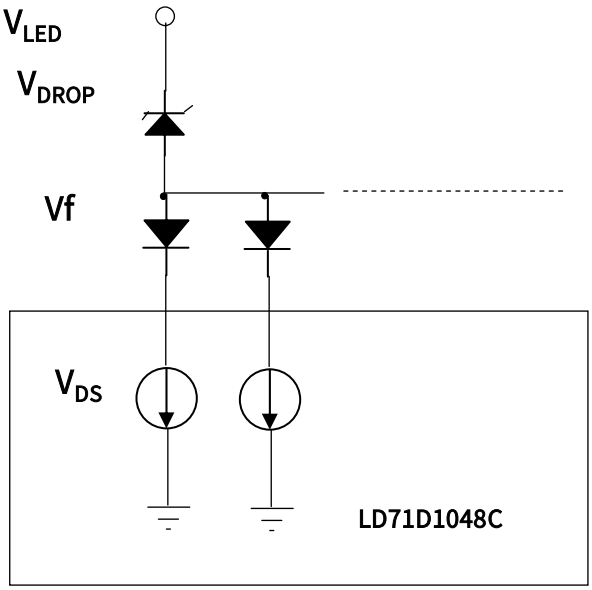
Load Supply Voltage (V_{LED})

LD71D1048C are disigned to operate with V_{DS} ranging from 0.7V to 1.5V considering the package power dissipating limits. V_{DS} may be higher enough to make $P_{D(act)} > P_{D(max)}$ When V_{LED} = 5V and V_{DS} –Vf , in whitch V_{LED} is the load supply voltage. In this case, it is recommended to use the lowest possible supply voltage or to set an external voltage reducer (V_{DROP}).

A Voltage reduce lets $V_{DS} = (V_{LED} - Vf) - V_{DROP}$.

Resisters, or Zener diode can be used in the applications as the following figures.





FUNCTIONAL DESCRIPTION

SYSTEM INTERFACE

- SCKENEnable Input
  if SCKEN is high, LD71D1048C receive SCKIN signal and DIN<9:0>

- STENB enables STINB.
  If STENB is Low , LD71D1048C receive STINB and Transfer Shift register Data to Memory

- **Output Enable Input**
  The LD71D1048C has 3 output enable pin (OEB_R, OEB_G, OEB_B). If the OEB = 1, output are off and if OEB = 0 then all output pins are PWM output. Refer to timing diagram.

- **Data Input / Output**
  The LD71D1048C has 10bit data input pins (DIN[9:0]) and 10Bit data output pins (DOUT[9:0]). The output data is out after 48 times SCKIN from input data. If DOUT[9:0] pins are connected to next device DIN[9:0] pins, the first device 48bit input data can shift the next device 48bit input data by SCKIN. It can transfer display data to serial method so it makes device to connect directly. The 10Bit input data are inputted 10Bit COUT1 and next 10Bit COUT2 and next 10Bit COUT3 … COUT48 input data by SCKIN. Refer to timing diagram.

- **PWM Function**
  The LD71D1048C has 10 bit PWM function. PWM 10 bit data is received by DIN[9:0] pins. It can control LED driver brightness by 1024 gray scale. Refer to column driver timing diagram.

- **Row Control**
  The LD71D1048C has 16 bit row control pins (ROUT[16:1]). The signal of row controller is using for scanning. RIN_OUT pin is “L”, ROUT signals are generated by internal clock. If RIN_OUT pin is “H”, ROUT signals are generated by RAD0 ~ RAD3 and ROUT[16:1] signals are available . If RIN_OUT pin is “L” and P8_16 is “L”, ROUT[8:1] signals are available. P8_16 is “H”, ROUT[16:1] signals are available. Refer to row driver timing diagram.

- **SRAM Function**
  The LD71D1048C has 7,680 bits SRAM memory. The 7,680 bits SRAM store 10 bits PWM data of 16 row and 48 column. Refer to timing diagram.

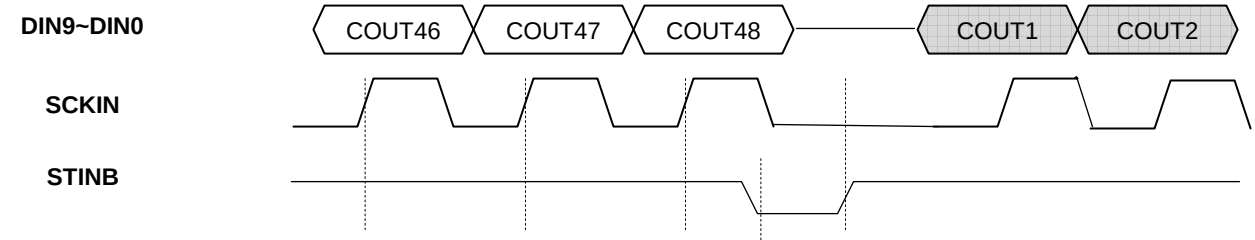
- **ROUT Monitor Function**
  This is display off function when ROUT signal are halted at 0.3 second if ROUT is not change during 0.3 sec. It is including watch dog timer in the LD71D1048C.

- **RC Oscillation**
  The LD71D1048C is consisted of internal RC oscillation circuit. So oscillation frequency is changed by external resistor . The external resistor is connected with OSC1,OSC2 pins. Refer to RC Oscillation diagram.

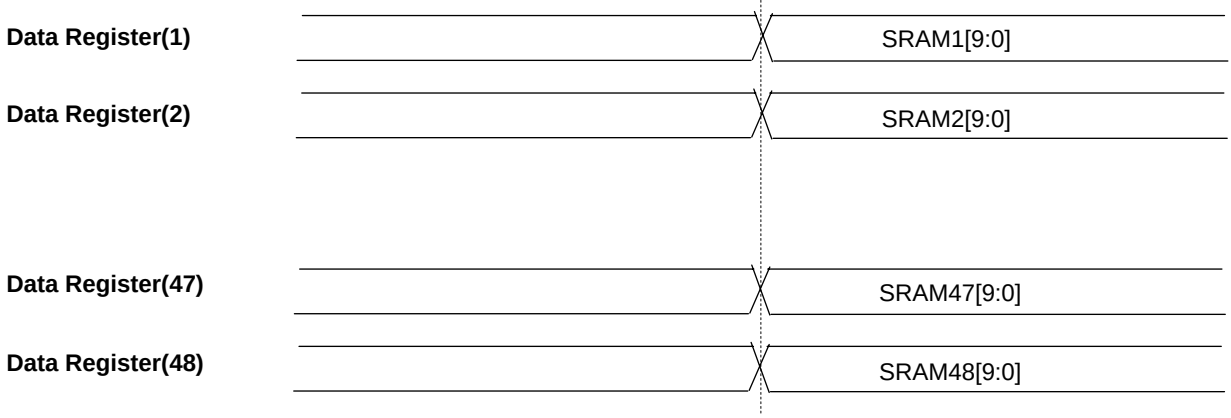
FUNCTIONAL DESCRIPTION (continued)

INPUT TIMING DIAGRAM

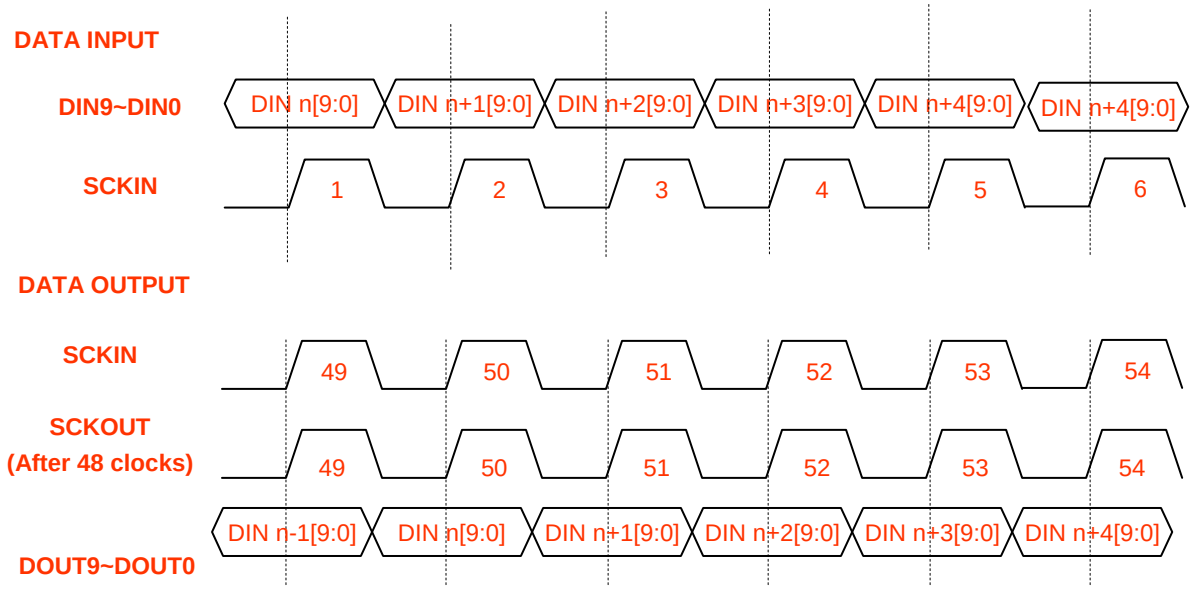
Data Input



Data Register DATA (internal)



DOUT TIMING DIAGRAM



FUNCTIONAL DESCRIPTION (continued)

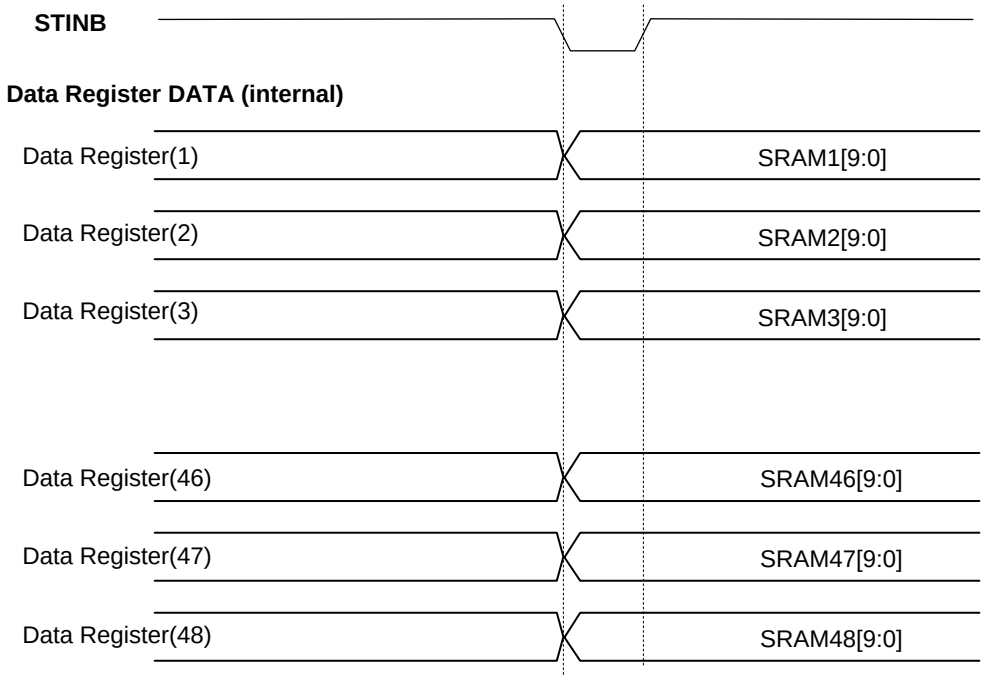
SRAM MAP

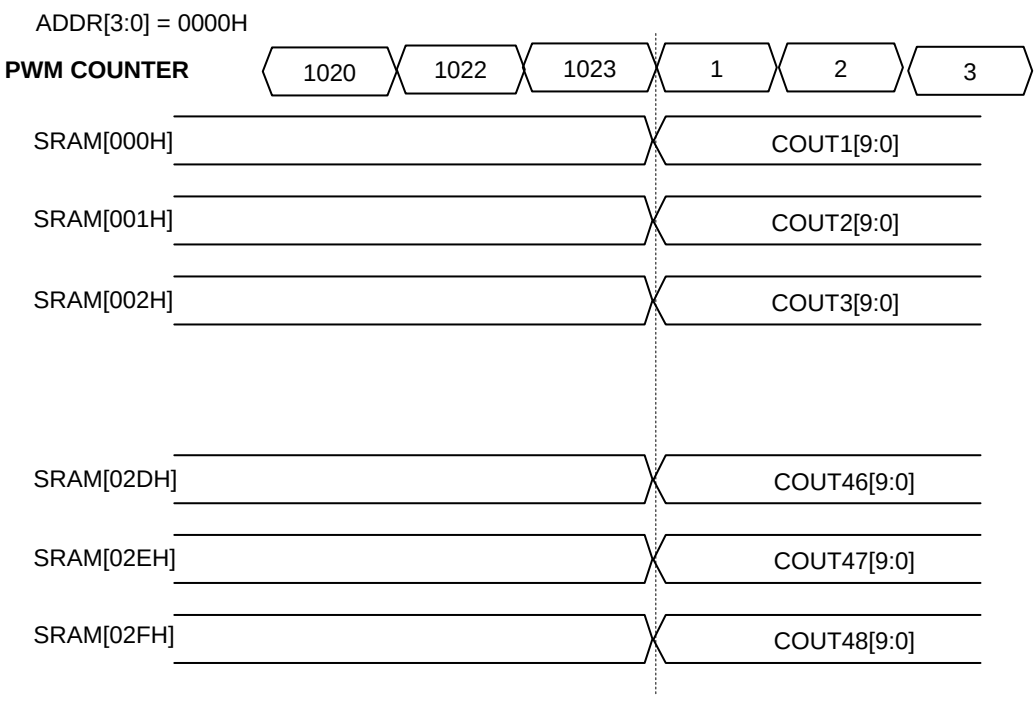
ADDRESS		COUT1	COUT2	COUT3	COUT4	●●●	COUT46	COUT47	COUT48
		00	01	02	03	●●●	2D	2E	2F
ADDR0 ~ 3	0	000H	001H	002H	003H	●●●	02D	02E	02F
	1	100H	101H	102H	103H	●●●	12D	12E	12F
	2	200H	201H	202H	203H	●●●	22D	22E	22F
	3	300H	301H	302H	303H	●●●	32D	32E	32F
	4	400H	401H	402H	403H	●●●	42D	42E	42F
	5	500H	501H	502H	503H	●●●	52D	52E	52F
	6	600H	601H	602H	603H	●●●	62D	62E	62F
	7	700H	701H	702H	703H	●●●	72D	72E	72F
	8	800H	801H	802H	803H	●●●	82D	82E	82F
	9	900H	901H	902H	903H	●●●	92D	92E	92F
	A	A00H	A01H	A02H	A03H	●●●	A2D	A2E	A2F
	B	B00H	B01H	B02H	B03H	●●●	B2D	B2E	B2F
	C	C00H	C01H	C02H	C03H	●●●	C2D	C2E	C2F
	D	D00H	D01H	D02H	D03H	●●●	D2D	D2E	D2F
	E	E00H	E01H	E02H	E03H	●●●	E2D	E2E	E2F
	F	F00H	F01H	F02H	F03H	●●●	F2D	F2E	F2F

48 address of SRAM the address 000H ~ 02FH are simultaneous writing data.

FUNCTIONAL DESCRIPTION (continued)

SRAM WRITE TIMING DIAGRAM

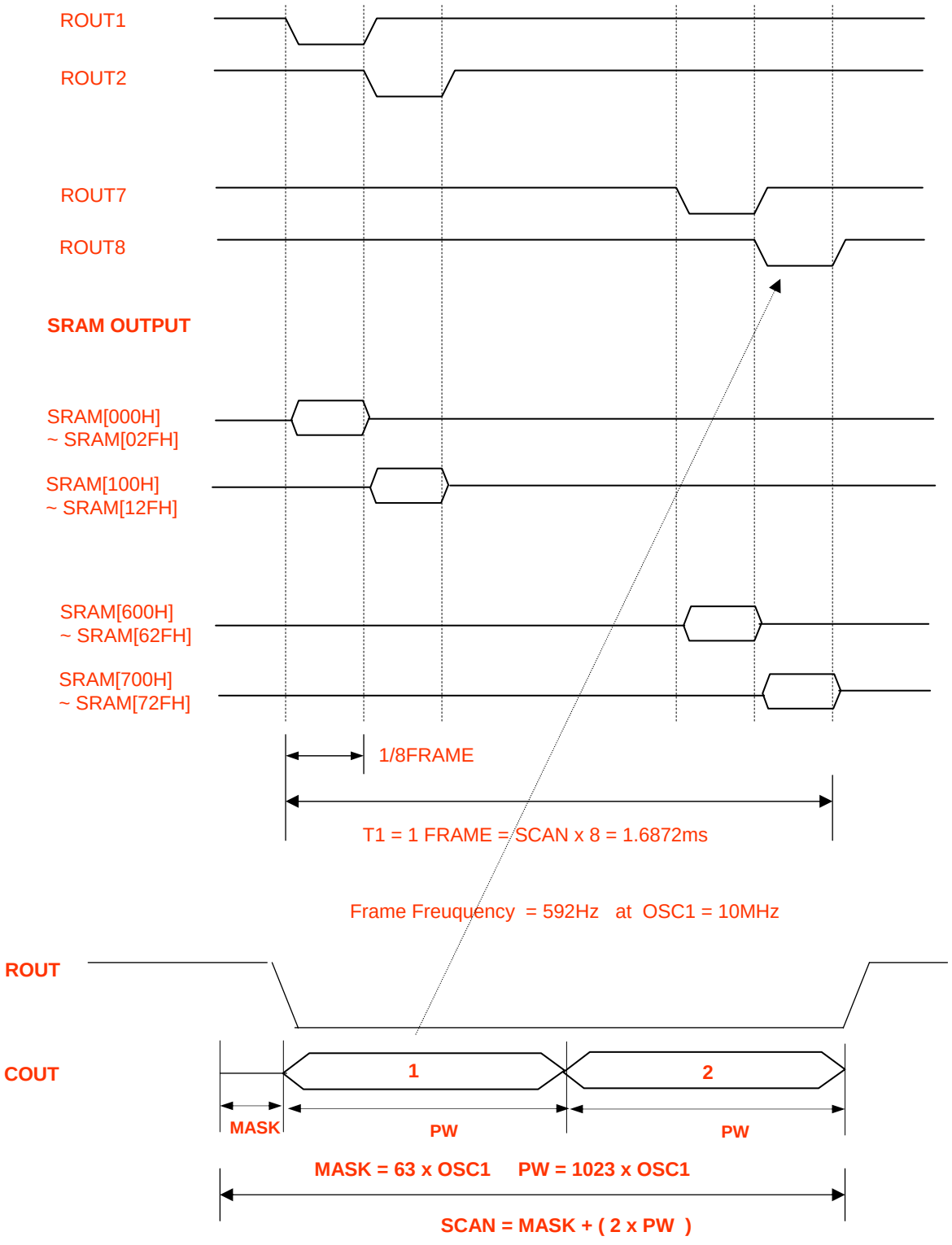




FUNCTIONAL DESCRIPTION (continued)

ROW DRIVER TIMING DIAGRAM(1)

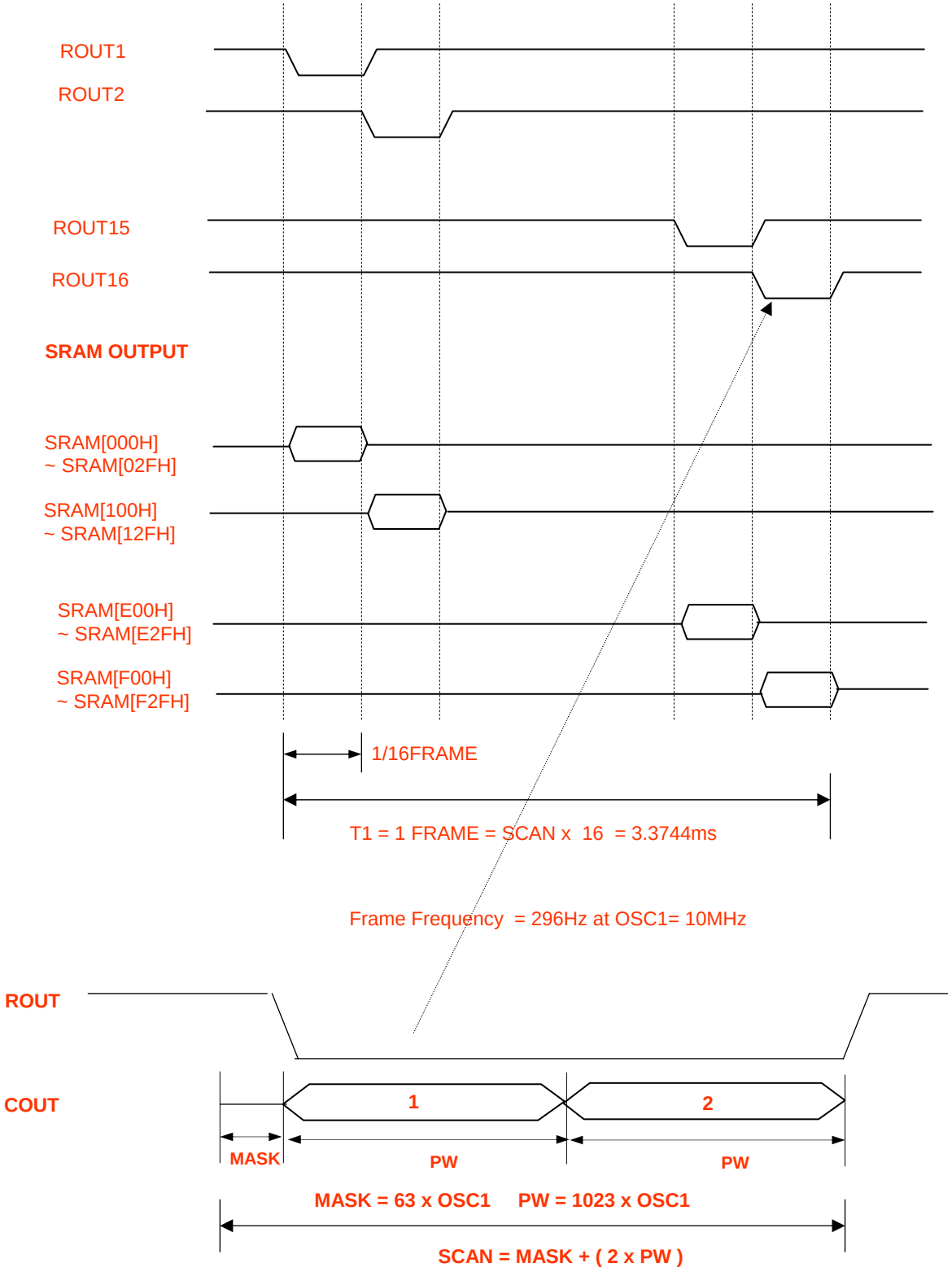
ROW Driver Internal Controlled Signal (P8/16 = 0, RIN_OUT = 0)



FUNCTIONAL DESCRIPTION (continued)

ROW DRIVER TIMING DIAGRAM(2)

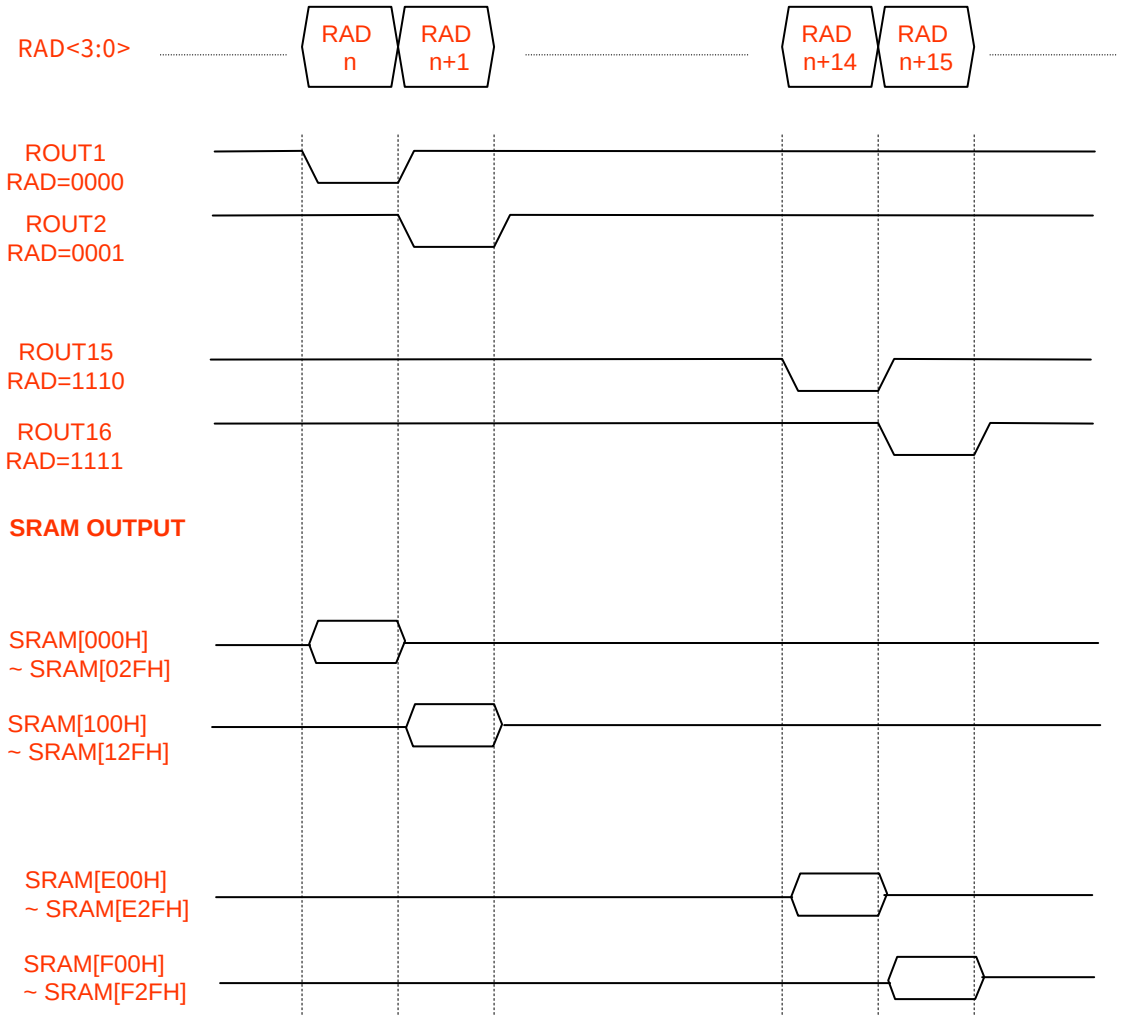
ROW Driver Internal Controlled Signal (P8/16 = 1, RIN_OUT =0)



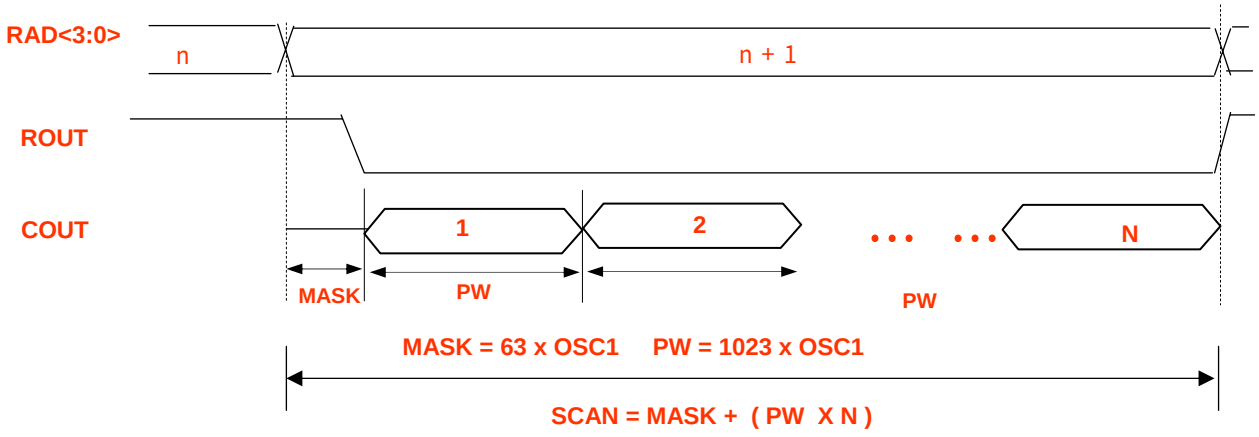
FUNCTIONAL DESCRIPTION (continued)

ROW DRIVER TIMING DIAGRAM(3)

ROW Driver External Controlled Signal (RIN_OUT = 1)



SCAN = [MASK + (PW x N)] x OSC1

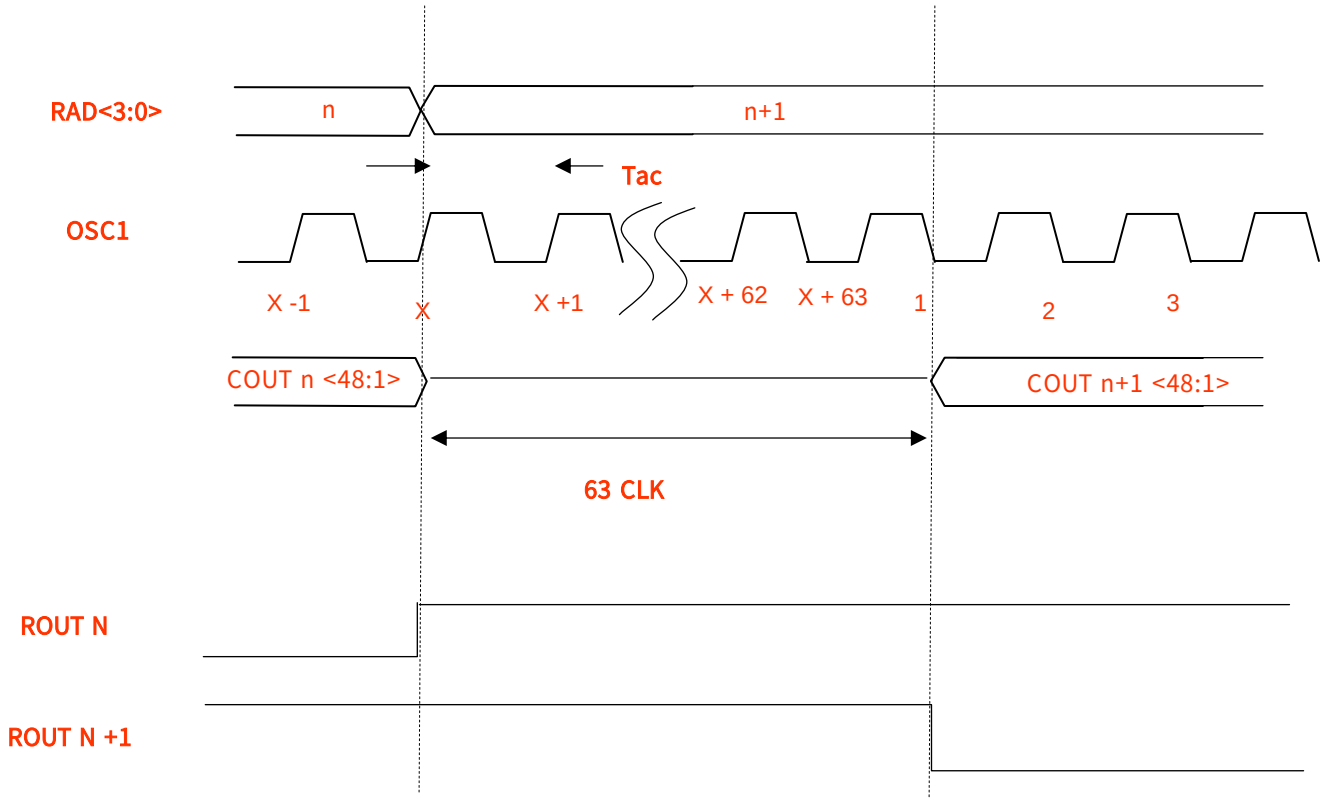


MASK = 63 x OSC1 PW = 1023 x OSC1

SCAN = MASK + (PW X N)

FUNCTIONAL DESCRIPTION (continued)

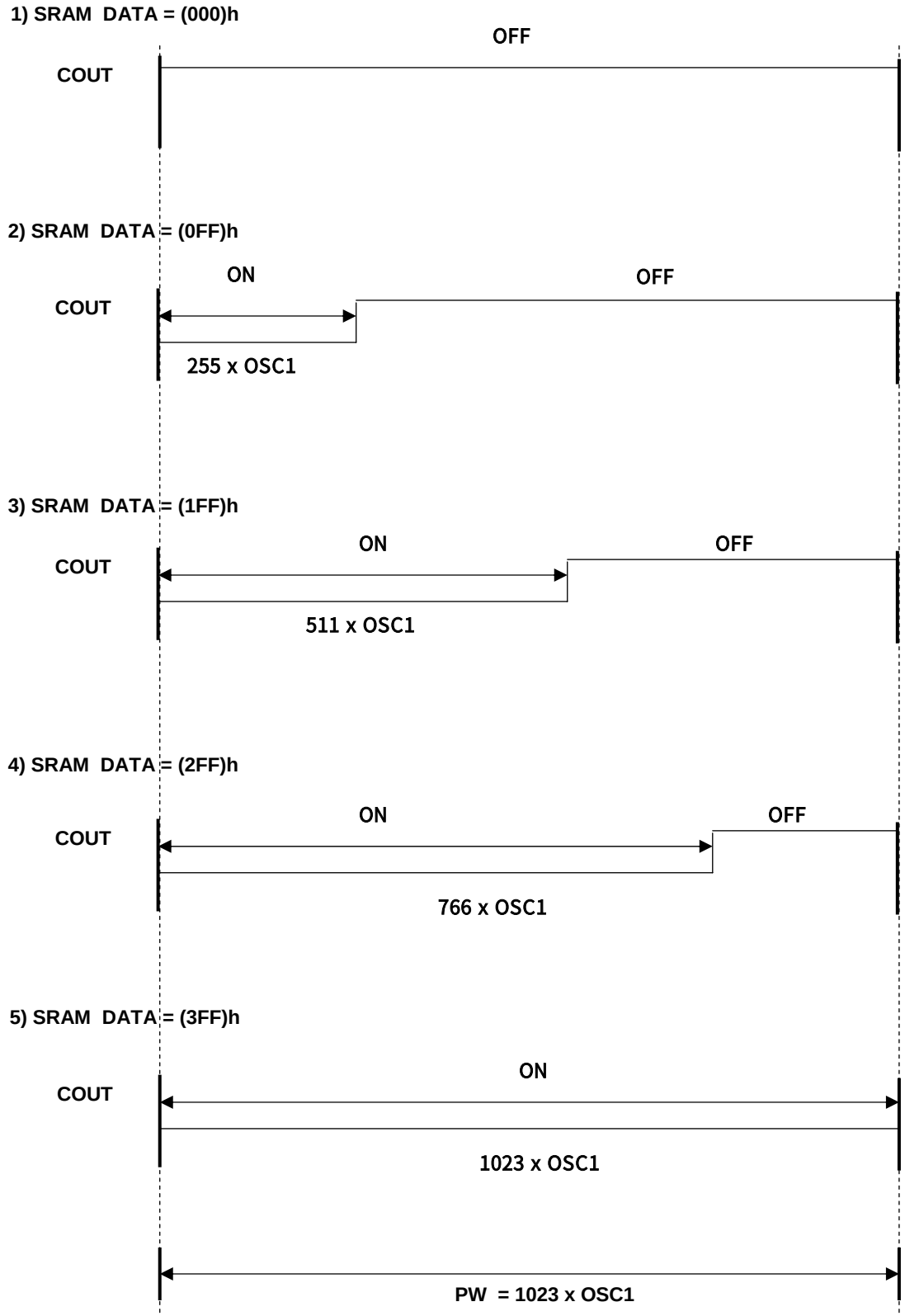
EXTERNAL ROW CONTROL TIMING



RAD Should Change at Time = (63 + 1023 x N) x OSC1

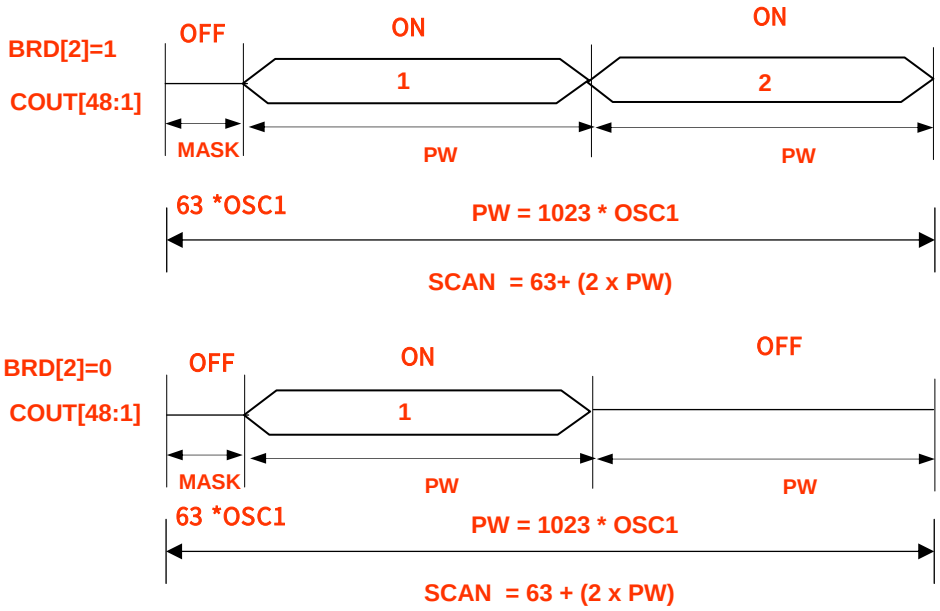
FUNCTIONAL DESCRIPTION (continued)

DATA WITH PWM TIMING DIAGRAM



FUNCTIONAL DESCRIPTION (continued)

COLUMN DRIVER TIMING DIAGRAM
BRIGHTNESS CONTROL(1)



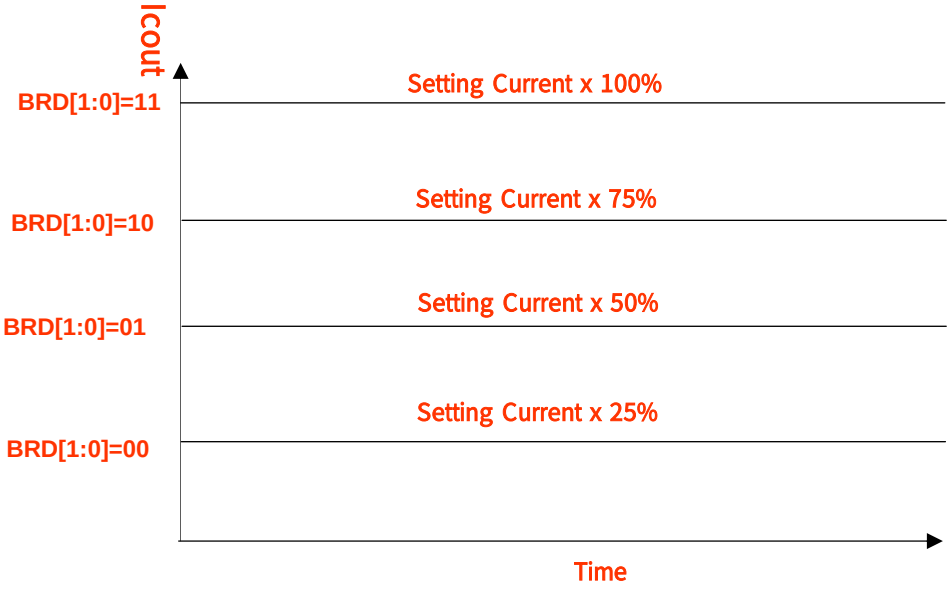
BRD[2] Control PWM Mask Time

When BRD[2]=1, two PW outout become on

When BRD[2]=0 , one of two PW output become off

FUNCTIONAL DESCRIPTION (continued)

COLUMN DRIVER TIMING DIAGRAM
BRIGHTNESS CONTROL(2)



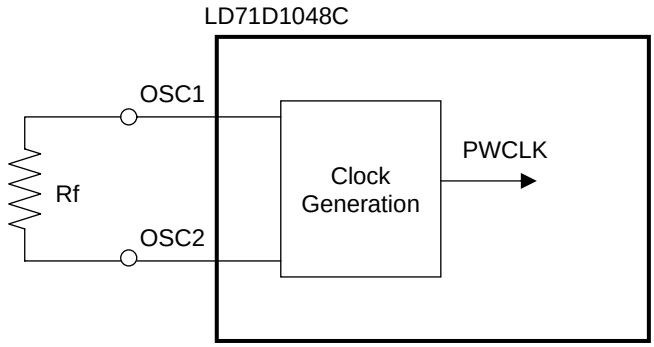
BRD[1:0] Controls Icout Level

BRD[1:0]=11 = Icout X 100%, BRD[1:0]=10 = Icout X 75%,
]
BRD[1:0]=01 = Icout X 50%, BRD[1:0]=00 = Icout X 25%

FUNCTIONAL DESCRIPTION (continued)

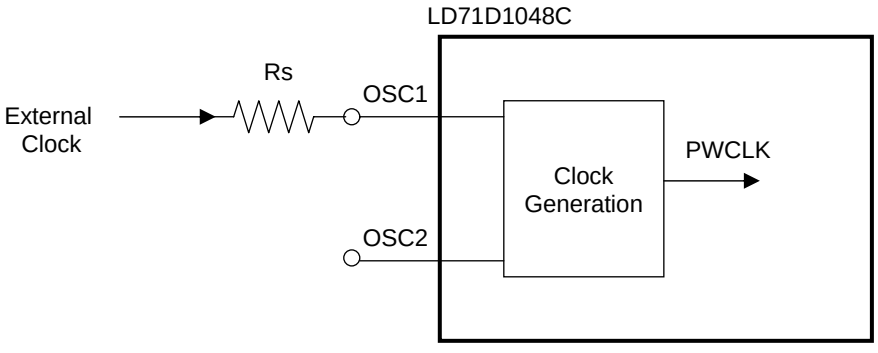
RC OSCILLATION

Internal Oscillation



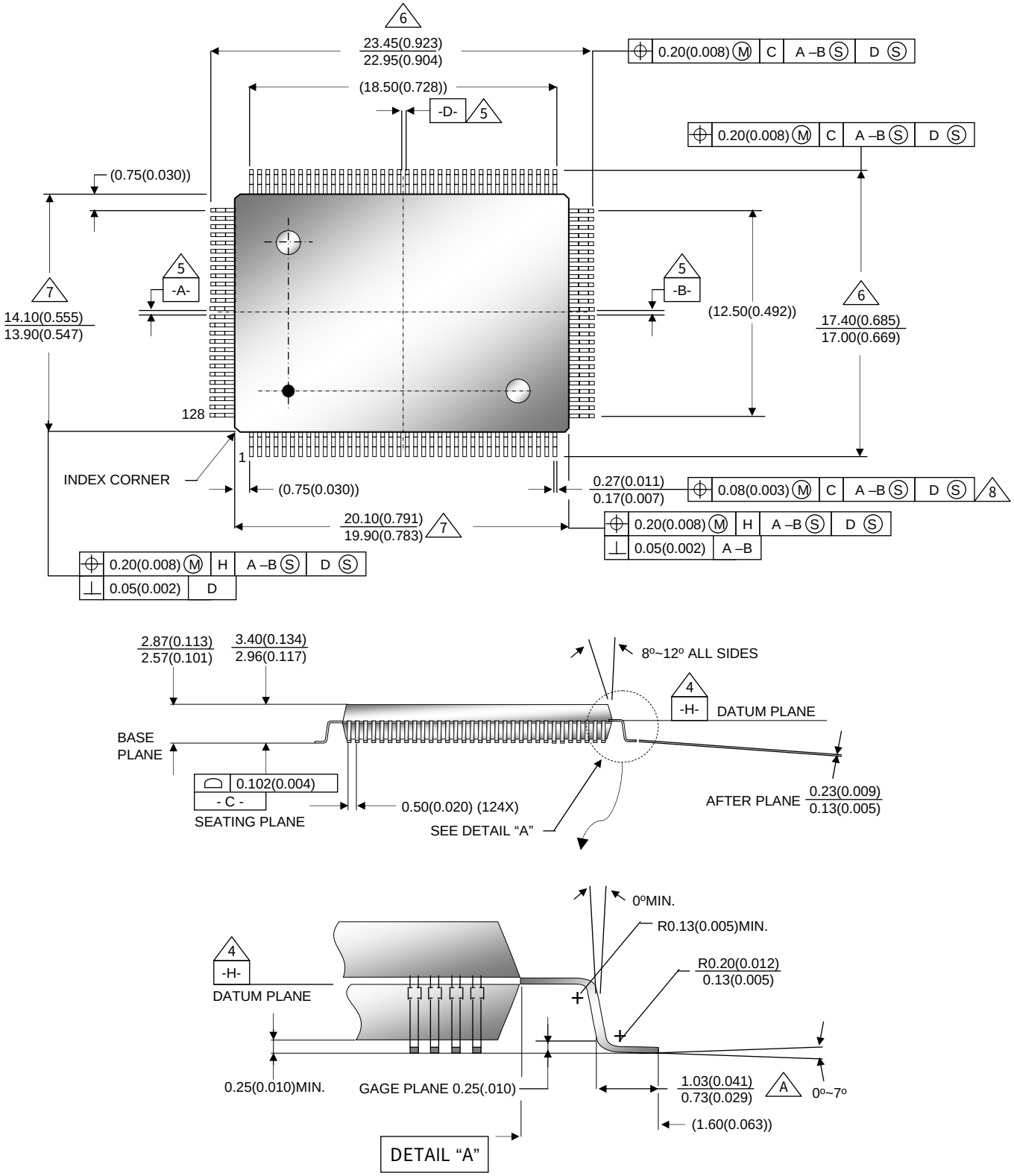
Rf = 0.0k OSC1 = 10MHz +- 10%
Rf = 2k OSC1 = 9MHz +- 10%
Rf = 3k OSC1 = 7MHz +- 10%
Rf = 4k OSC1 = 6MHz +- 10%
Rf = 5k OSC1 = 5MHz +- 10%

External Oscillation



PACKAGE INFORMATION

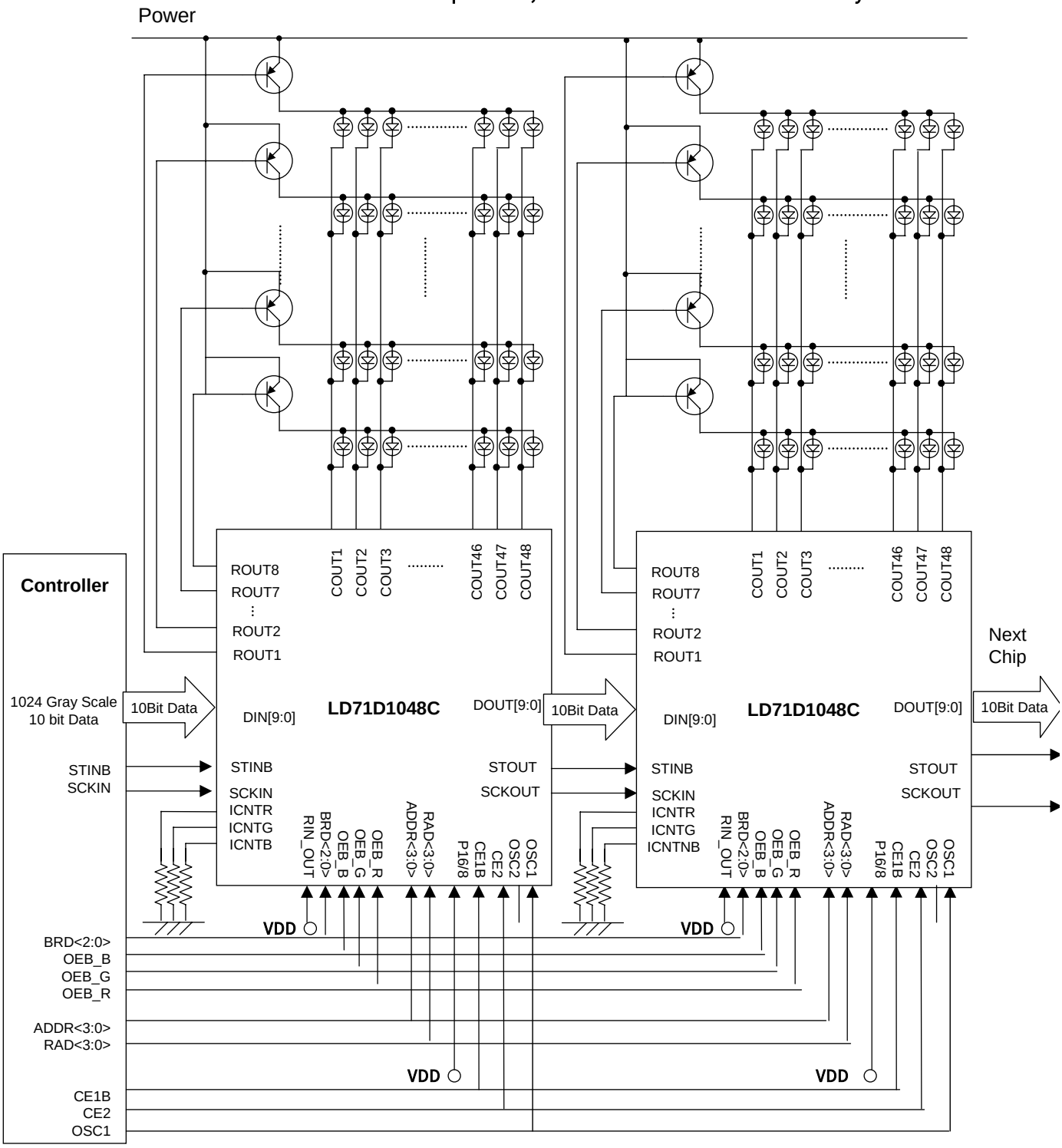
128 PIN MQFP (14 x 20 Body)



REFERENCE APPLICATIONS

Case 1 : External ROUT Change : You can select ROUT port with RAD<3:0>

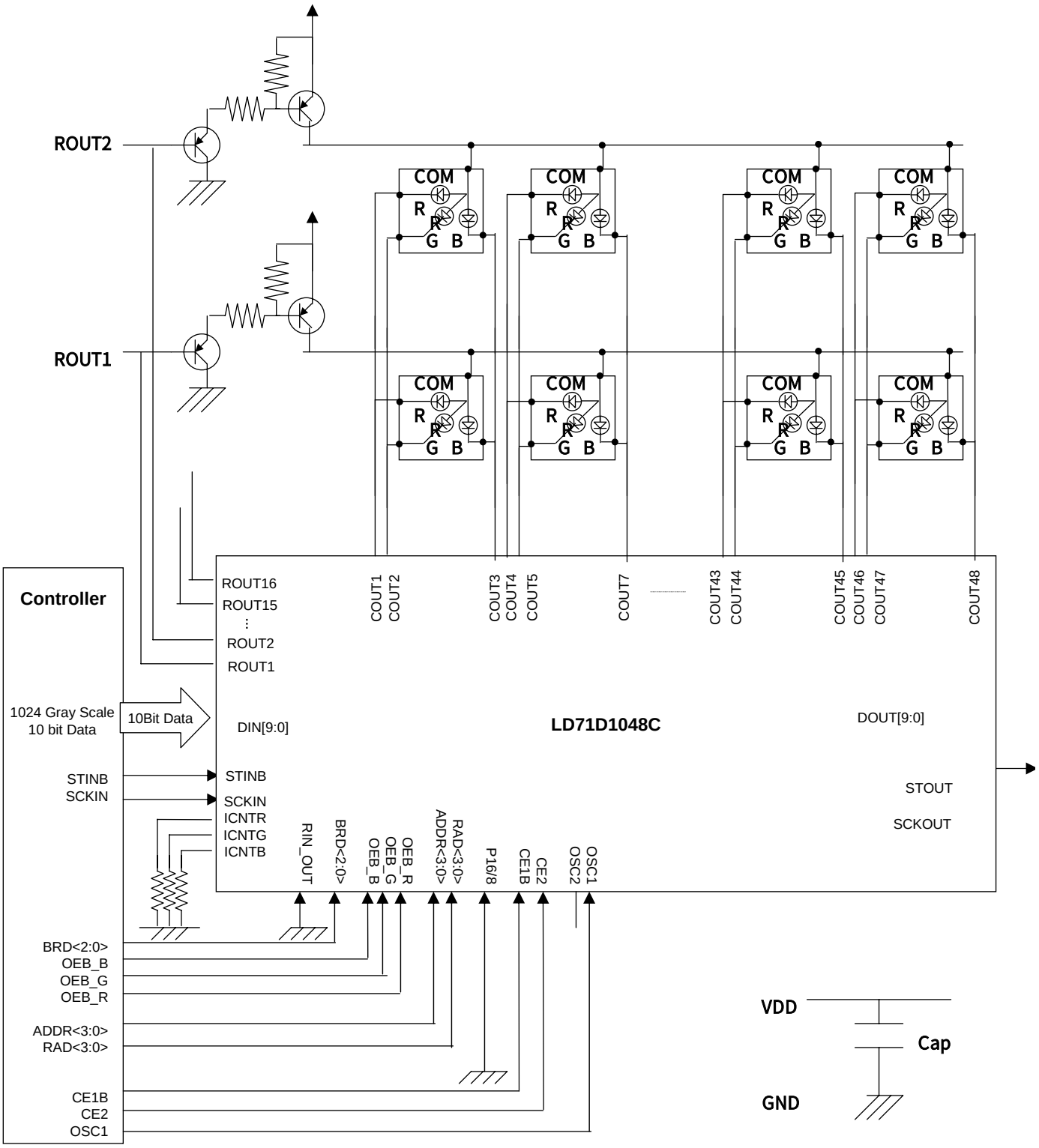
For Eample RAD3,RAD2=GND ROU1~ROUT4 Actived by RAD<1:0>



Data & Control Signal Connection

REFERENCE APPLICATIONS 2

Case 5 : Interal ROUT Change : ROUT1 ~ ROUT8



Data & Control Signal Connection