

N-Channel Power MOSFET 22A, 600Volts

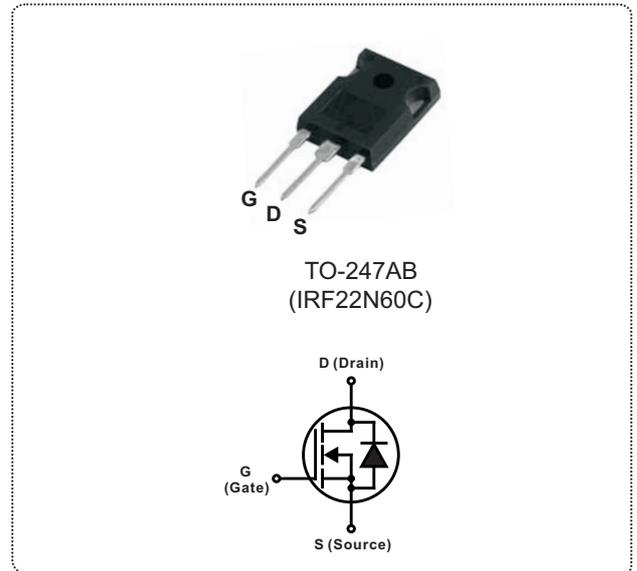
DESCRIPTION

The Nell **IRF22N60** is a three-terminal silicon device with current conduction capability of 22A, fast switching speed, low on-state resistance, breakdown voltage rating of 600V, and max. threshold voltage of 5 volts.

They are designed for use in applications such as switched mode power supplies, DC to DC converters, motor control circuits, UPS and general purpose switching applications.

FEATURES

- $R_{DS(ON)} = 0.28\Omega @ V_{GS} = 10V$
- Ultra low gate charge(150nC Max.)
- Low reverse transfer capacitance ($C_{RSS} = 36pF$ typical)
- Fast switching capability
- 100% avalanche energy specified
- Improved dv/dt capability
- 150°C operation temperature



PRODUCT SUMMARY

I_D (A)	22
V_{DSS} (V)	600
$R_{DS(ON)}$ (Ω)	0.28 @ $V_{GS} = 10V$
Q_G (nC) max.	150

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ C$ unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS	VALUE	UNIT
V_{DSS}	Drain to Source voltage	$T_J = 25^\circ C$ to $150^\circ C$	600	
V_{DGR}	Drain to Gate voltage	$R_{GS} = 20K\Omega$	600	V
V_{GS}	Gate to Source voltage		± 30	
I_D	Continuous Drain Current ($V_{GS} = 10V$)	$T_C = 25^\circ C$	22	A
		$T_C = 100^\circ C$	14	
I_{DM}	Pulsed Drain current(Note 1)		88	
I_{AR}	Avalanche current(Note 1)		22	
E_{AR}	Repetitive avalanche energy(Note 1)	$I_{AR} = 22A, R_{GS} = 50\Omega, V_{GS} = 10V$	37	mJ
E_{AS}	Single pulse avalanche energy(Note 2)	$I_{AS} = 22A, L = 1.5mH$	380	
dv/dt	Peak diode recovery dv/dt(Note 3)		18	V / ns
P_D	Total power dissipation	$T_C = 25^\circ C$	370	W
	Derate above $25^\circ C$		2.9	W / $^\circ C$
T_J	Operation junction temperature		-55 to 150	
T_{STG}	Storage temperature		-55 to 150	$^\circ C$
T_L	Maximum soldering temperature, for 10 seconds	1.6mm from case	300	
	Mounting torque, #6-32 or M3 screw		10 (1.1)	lbf-in (N·m)

Note: 1. Repetitive rating: pulse width limited by junction temperature.
 2. $I_{AS} = 22A, L = 1.5mH, V_{DD} = 50V, R_G = 25\Omega$, starting $T_J = 25^\circ C$.
 3. $I_{SD} \leq 22A, di/dt \leq 540A/\mu s, V_{DD} \leq V_{(BR)DSS}$, starting $T_J < 150^\circ C$.

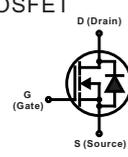
Nell High Power Products

THERMAL RESISTANCE					
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$R_{th(j-c)}$	Thermal resistance, junction to case			0.34	°C/W
$R_{th(c-s)}$	Thermal resistance, case to heat sink		0.24		
$R_{th(j-a)}$	Thermal resistance, junction to ambient			40	

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
◎ STATIC						
$V_{(BR)DSS}$	Drain to source breakdown voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	600			V
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown voltage temperature coefficient	$I_D = 1\text{mA}, V_{DS} = V_{GS}$		0.30		V/°C
I_{DSS}	Drain to source leakage current	$V_{DS} = 600\text{V}, V_{GS} = 0\text{V}$ $T_C = 25^\circ\text{C}$			50	μA
		$V_{DS} = 480\text{V}, V_{GS} = 0\text{V}$ $T_C = 125^\circ\text{C}$			250	
I_{GSS}	Gate to source forward leakage current	$V_{GS} = 30\text{V}, V_{DS} = 0\text{V}$			100	nA
	Gate to source reverse leakage current	$V_{GS} = -30\text{V}, V_{DS} = 0\text{V}$			-100	
$R_{DS(ON)}$	Static drain to source on-state resistance	$I_D = 13\text{A}, V_{GS} = 10\text{V}$		0.24	0.28	Ω
$V_{GS(TH)}$	Gate threshold voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	3.0		5.0	V
g_{fs}	Forward transconductance	$V_{DS} = 50\text{V}, I_D = 13\text{A}$	11			S
◎ DYNAMIC						
C_{ISS}	Input capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$		3570		pF
C_{OSS}	Output capacitance				350	
C_{RSS}	Reverse transfer capacitance				36	
$t_{d(ON)}$	Turn-on delay time	$V_{DD} = 300\text{V}, V_{GS} = 10\text{V}$ $I_D = 22\text{A}, R_G = 6.2\Omega, R_D = 3.2\Omega$ (Note1,2)		26		ns
t_r	Rise time			99		
$t_{d(OFF)}$	Turn-off delay time			48		
t_f	Fall time			37		
Q_G	Total gate charge	$V_{DD} = 480\text{V}, V_{GS} = 10\text{V}$ $I_D = 22\text{A},$ (Note1,2)			150	nC
Q_{GS}	Gate to source charge				45	
Q_{GD}	Gate to drain charge (Miller charge)				76	

SOURCE TO DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SD}	Diode forward voltage	$I_{SD} = 22\text{A}, V_{GS} = 0\text{V}$			1.5	V
$I_S (I_{SD})$	Continuous source to drain current	Integral reverse P-N junction diode in the MOSFET 			22	A
I_{SM}	Pulsed source current				88	
t_{rr}	Reverse recovery time	$I_{SD} = 22\text{A}, V_{GS} = 0\text{V},$ $di_f/dt = 100\text{A}/\mu\text{s}$	$T_J = 25^\circ\text{C}$	590	890	ns
			$T_J = 125^\circ\text{C}$	670	1010	
Q_{rr}	Reverse recovery charge	$I_{SD} = 22\text{A}, V_{GS} = 0\text{V},$ $di_f/dt = 100\text{A}/\mu\text{s}$	$T_J = 25^\circ\text{C}$	7.2	11	μC
			$T_J = 125^\circ\text{C}$	8.5	13	
I_{RRM}	Reverse recovery current			26	39	A
t_{qd}	Forward turn-on time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Note: 1. Pulse test: Pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

ORDERING INFORMATION SCHEME

IRF 22N60 C

MOSFET series

N-Channel, IRF series

Current and Voltage rating, I_D & V_{DS}

22A / 600V

Package type

C = TO-247AB

■ TYPICAL CHARACTERISTICS

Fig.1 Typical output characteristics, $T_C=25^\circ\text{C}$

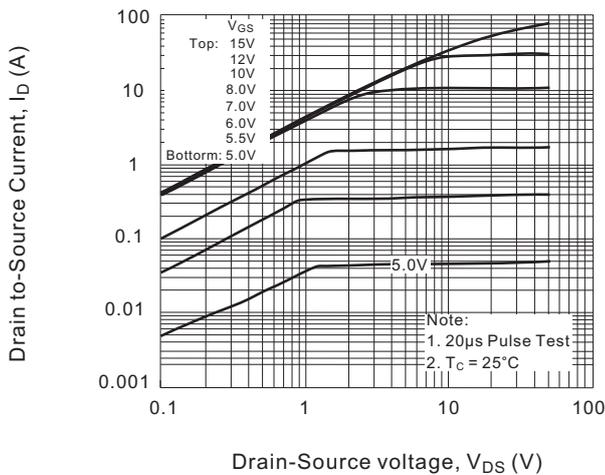


Fig.2 Typical output characteristics, $T_C=150^\circ\text{C}$

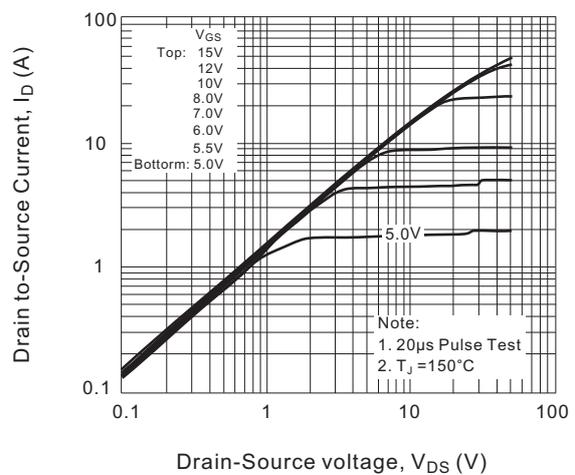


Fig.3 Typical transfer characteristics

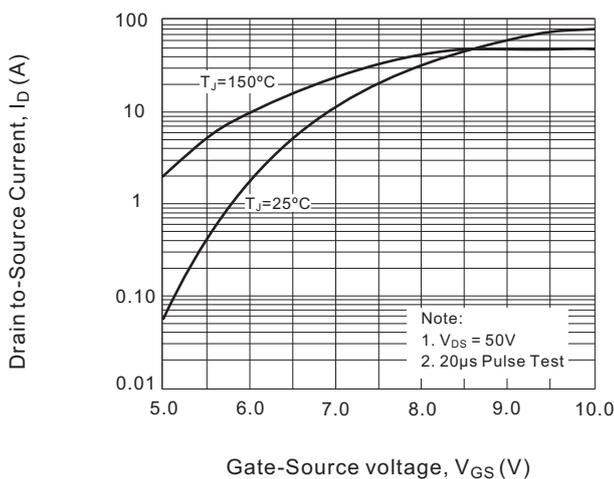


Fig.4 Normalized On-Resistance vs. Temperature

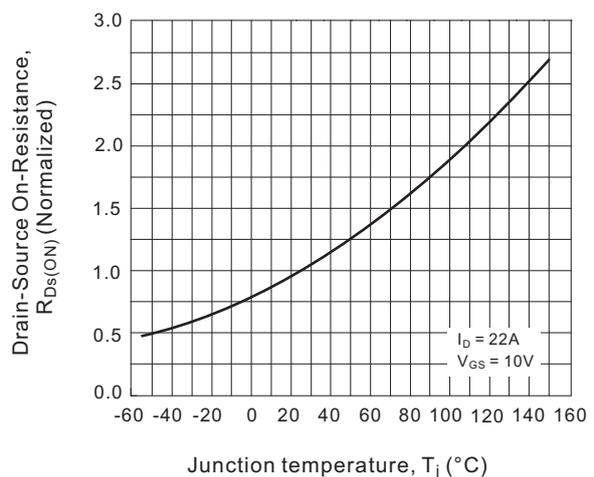


Fig.5 Typical capacitance vs. Drain-to-Source voltage

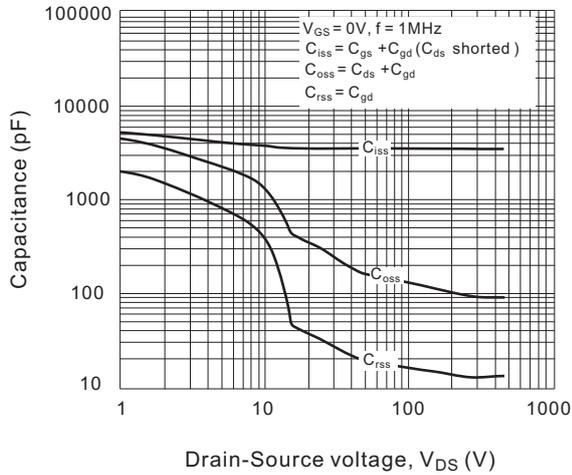


Fig.6 Typical gate charge vs. gate-to-source voltage

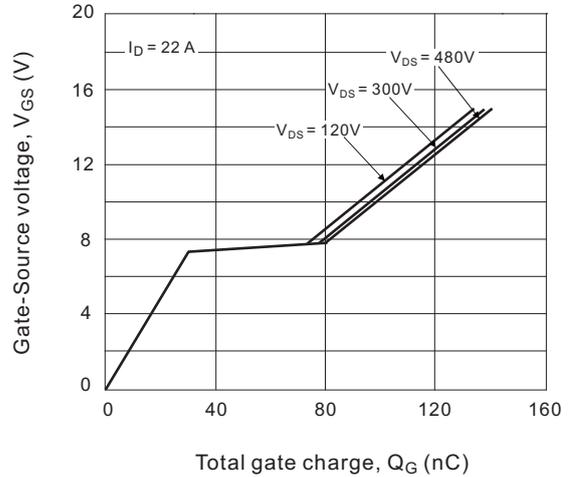


Fig.7 Typical source-drain diode forward voltage

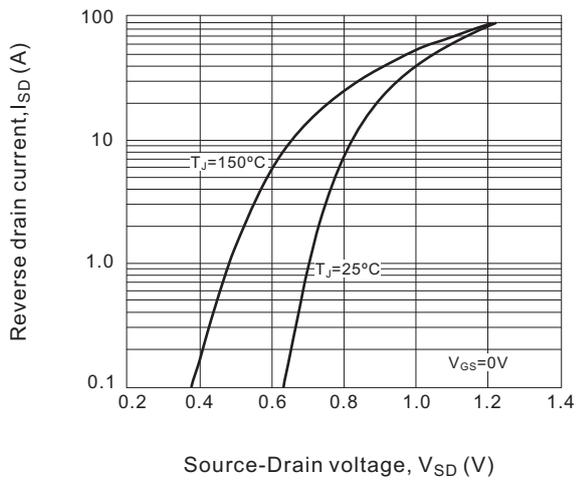


Fig.8 Maximum safe operating area

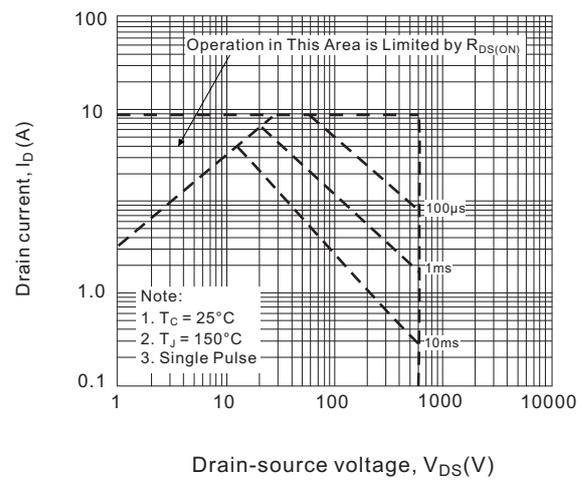


Fig.9 Maximum drain current vs. Case temperature

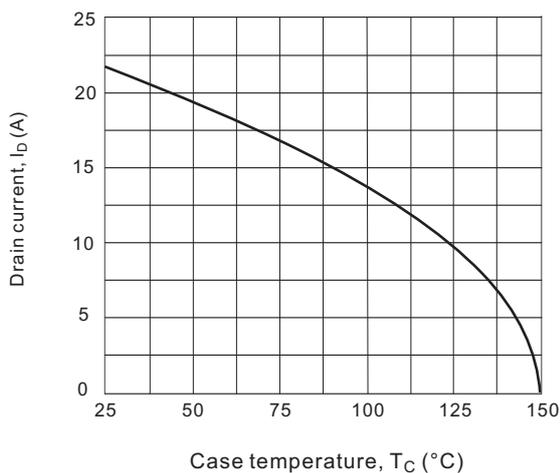


Fig.10 Maximum effective transient thermal impedance, Junction-to-Case

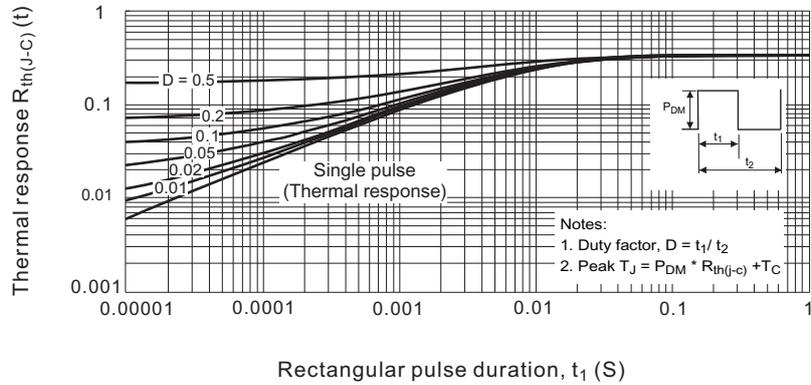


Fig.11a. Switching time test circuit

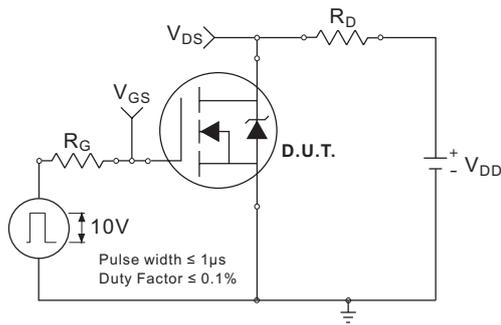


Fig.11b. Switching time waveforms

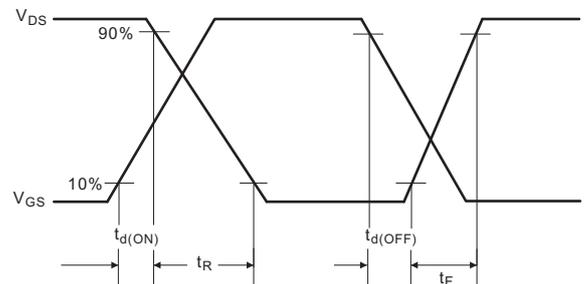
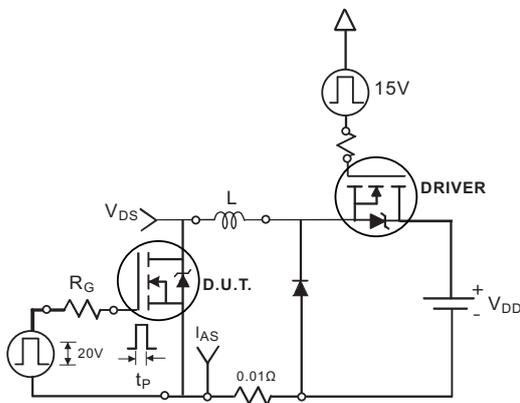


Fig.12a. Unclamped Inductive test circuit



Vary t_p to obtain required I_{AS}

Fig.12b. Unclamped Inductive waveforms

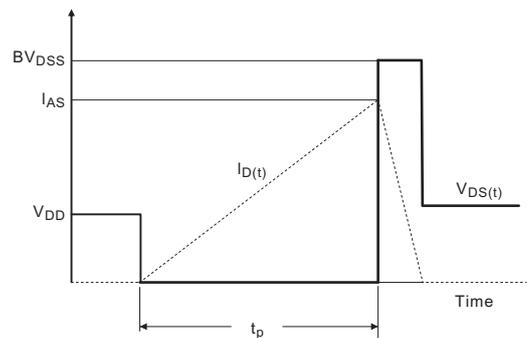


Fig.12c. Maximum avalanche energy vs. Drain current

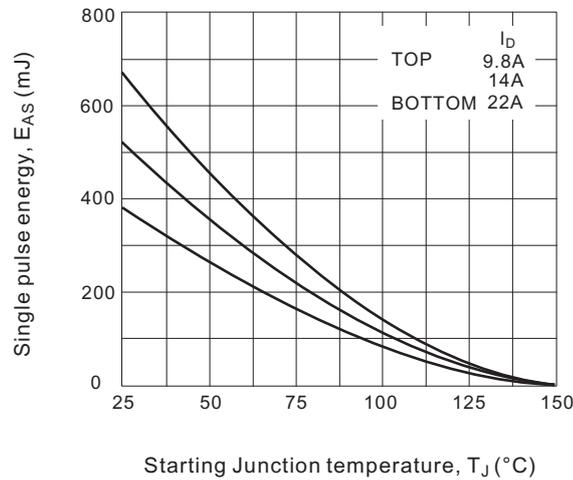


Fig.13a. Basic gate charge waveform

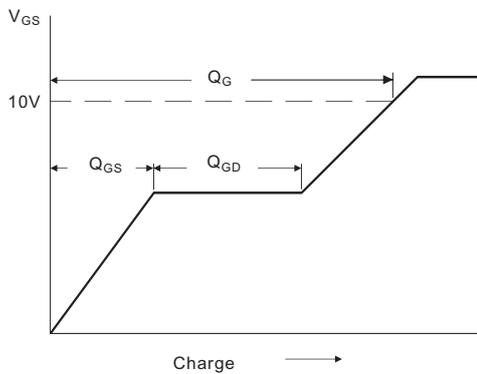


Fig.13b. Gate charge test circuit

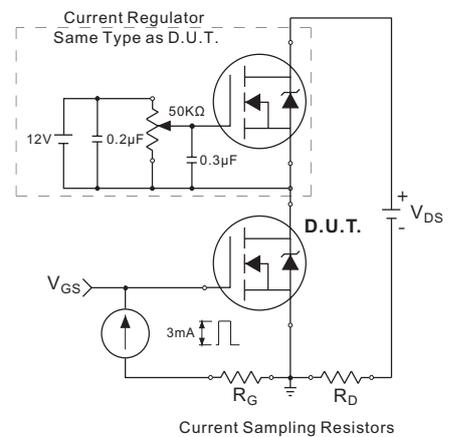
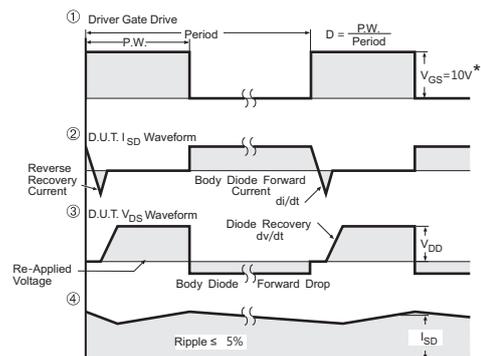
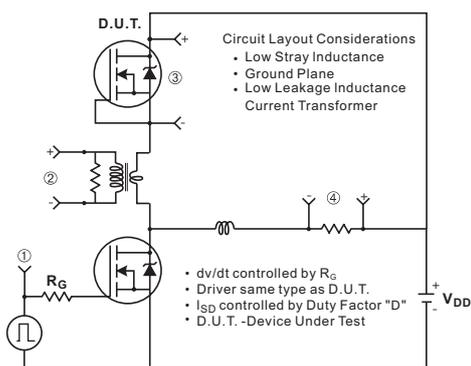


Fig.14 Peak diode recovery dv/dt test circuit for N-Channel MOSFET



* $V_{GS} = 5V$ for Logic Level Devices and $3V$ for drive devices

