TY Semicondutor®

Product specification

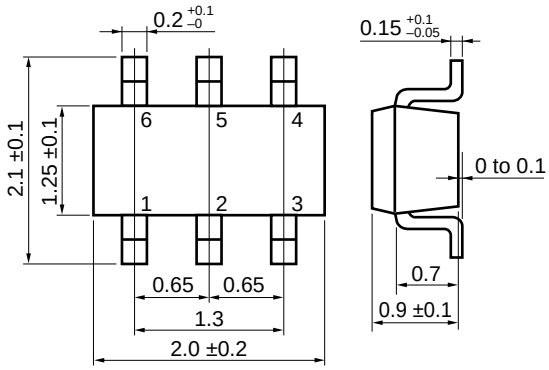
μPA672T

The μPA672T is a super-mini-mold device provided with two MOS FET elements. It achieves high-density mounting and saves mounting costs.

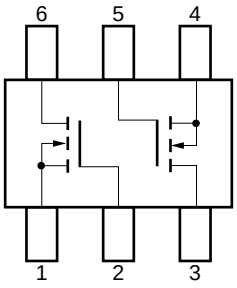
FEATURES

- Two MOS FET circuits in package the same size as SC-70
- Automatic mounting supported

PACKAGE DIMENSIONS (in millimeters)



PIN CONNECTION



1. Source 1 (S1)
2. Gate 1 (G1)
3. Drain 2 (D2)
4. Source 2 (S2)
5. Gate 2 (G2)
6. Drain 1 (D1)

Marking: MA

ABSOLUTE MAXIMUM RATINGS (T_A = 25 ˚C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Drain to Source Voltage	V_{DSS}		50	V
Gate to Source Voltage	V_{GSS}		±7.0	V
Drain Current (DC)	$I_{D(DC)}$		100	mA
Drain Current (pulse)	$I_{D(pulse)}$	PW ≤ 10 ms, Duty Cycle ≤ 50 %	200	mA
Total Power Dissipation	P_T		200 (Total)	mW
Channel Temperature	T_{ch}		150	˚C
Storage Temperature	T_{stg}		–55 to +150	˚C

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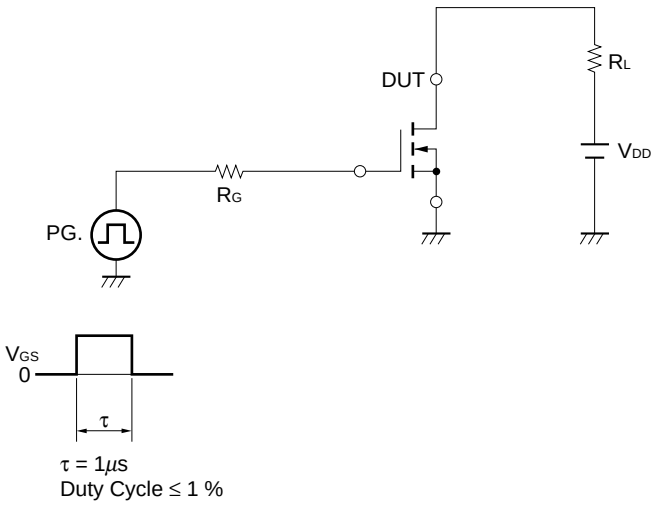
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain Cut-off Current	I_{DSS}	V_{DS} = 50 V, V_{GS} = 0			10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±7.0 V, V_{DS} = 0			±5.0	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 3.0 V, I_D = 1.0 μA	0.7	1.0	1.5	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 3.0 V, I_D = 10 mA	20			mS
Drain to Source On-State Resistance	$R_{DS(on)1}$	V_{GS} = 2.5 V, I_D = 10 mA		20	40	Ω
Drain to Source On-State Resistance	$R_{DS(on)2}$	V_{GS} = 4.0 V, I_D = 10 mA		15	20	Ω
Input Capacitance	C_{iss}	V_{DS} = 3.0 V, V_{GS} = 0, f = 1.0 MHz		6		pF
Output Capacitance	C_{oss}			8		pF
Reverse Transfer Capacitance	C_{rss}			1.2		pF
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 3 V, I_D = 20 mA, $V_{GS(on)}$ = 3 V, R_G = 10 Ω, R_L = 120 Ω		9		ns
Rise Time	t_r			50		ns
Turn-Off Delay Time	$t_{d(off)}$			20		ns
Fall Time	t_f			40		ns

SWITCHING TIME MEASUREMENT CIRCUIT AND CONDITIONS



τ = 1μs
Duty Cycle ≤ 1 %