



# BUK7Y72-80E

N-channel 80 V, 72 mΩ standard level MOSFET in LPAK56

20 February 2013

Product data sheet

## 1. General description

Standard level N-channel MOSFET in an LPAK56 (Power SO8) package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

## 2. Features and benefits

- Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True standard level gate with  $V_{GS(th)}$  rating of greater than 1 V at 175 °C

## 3. Applications

- 12 V, 24 V and 48 V Automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	-	80	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>	-	-	16	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	-	-	45	W
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 5\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 11</a>	-	54	72	mΩ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 10\text{ V}$ ; $I_D = 5\text{ A}$ ; $V_{DS} = 64\text{ V}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	-	3.3	-	nC

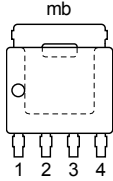
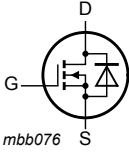


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## 5. Pinning information

**Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p><b>LPAK; Power-SO8 (SOT669)</b></p>	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 6. Ordering information

**Table 3. Ordering information**

Type number	Package		Version
	Name	Description	
BUK7Y72-80E	LPAK; Power-SO8	plastic single-ended surface-mounted package; 4 leads	SOT669

## 7. Marking

**Table 4. Marking codes**

Type number	Marking code
BUK7Y72-80E	77280E

## 8. Limiting values

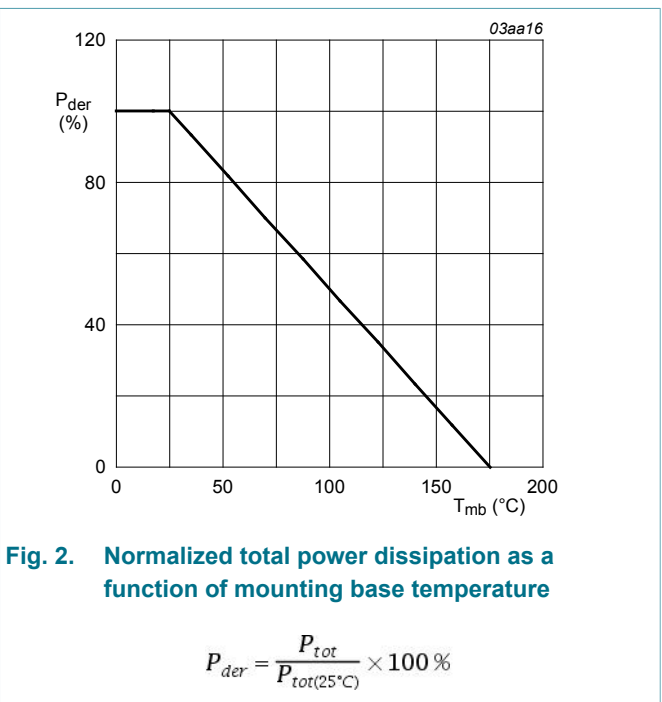
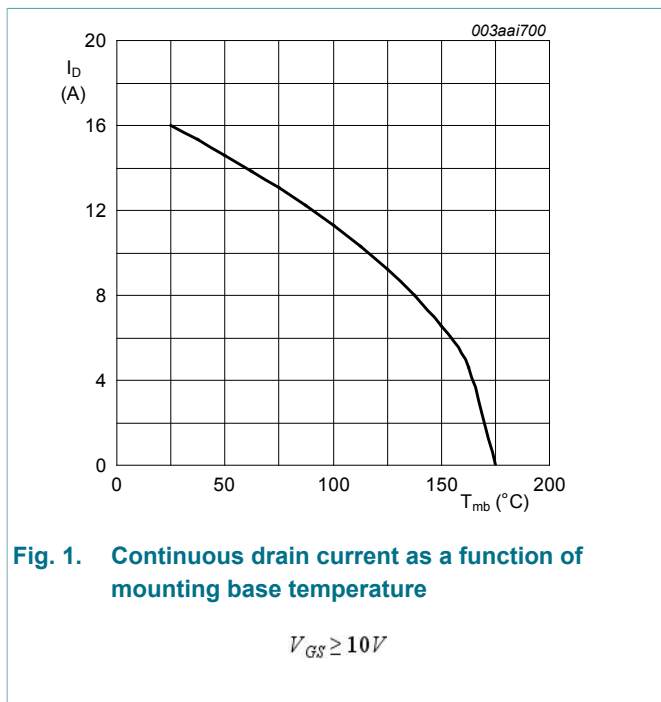
**Table 5. Limiting values**

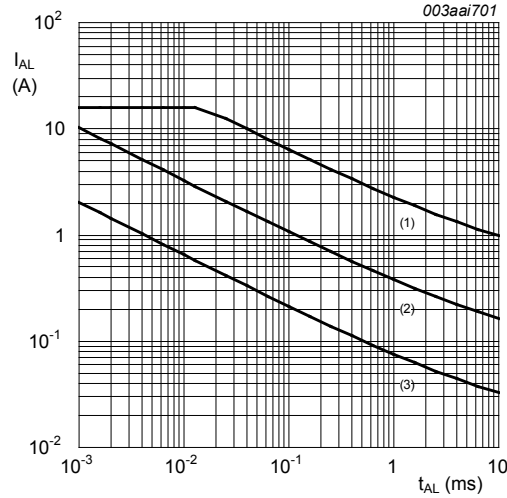
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	80	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	80	V
$V_{GS}$	gate-source voltage	$T_j \leq 175\text{ °C}; DC$	-20	20	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V}; \text{Fig. 1}$	-	16	A
		$T_{mb} = 100\text{ °C}; V_{GS} = 10\text{ V}; \text{Fig. 1}$	-	11	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C}; \text{pulsed}; t_p \leq 10\text{ }\mu\text{s}; \text{Fig. 4}$	-	63	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}; \text{Fig. 2}$	-	45	W
$T_{stg}$	storage temperature		-55	175	°C

Symbol	Parameter	Conditions	Min	Max	Unit
$T_j$	junction temperature		-55	175	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	16	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$	-	63	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 16\text{ A}$ ; $V_{sup} \leq 80\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; unclamped; <a href="#">Fig. 3</a>	[1][2]	-	12.5 mJ

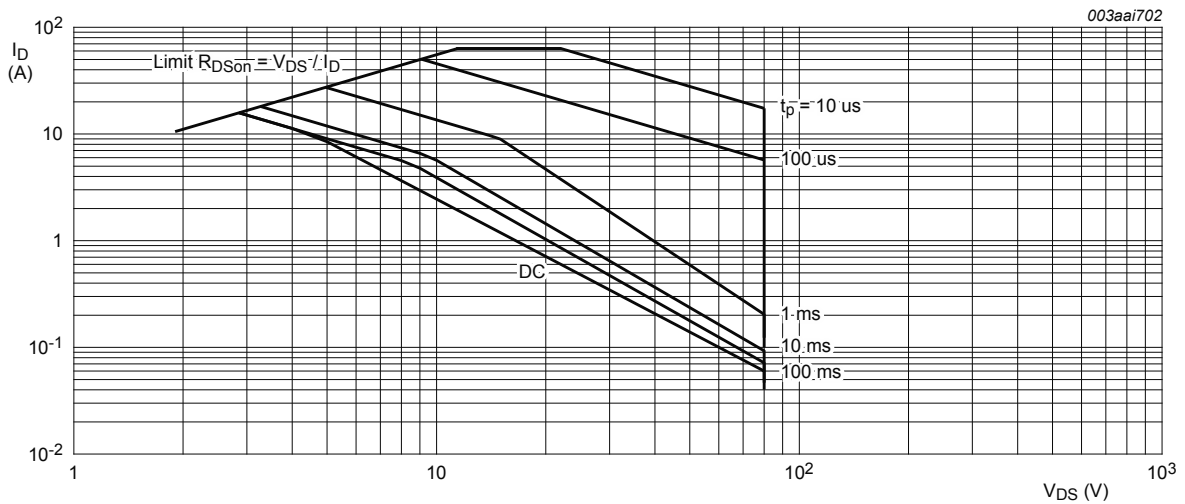
- [1] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [2] Refer to application note AN10273 for further information.





**Fig. 3. Avalanche rating; avalanche current as a function of avalanche time**

(1)  $T_{j (init)} = 25^\circ C$ ; (2)  $T_{j (init)} = 150^\circ C$ ; (3) Repetitive Avalanche



**Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

$T_{mb} = 25^\circ C$ ;  $I_{DM}$  is a single pulse

## 9. Thermal characteristics

**Table 6. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 5</a>	-	-	3.33	K/W

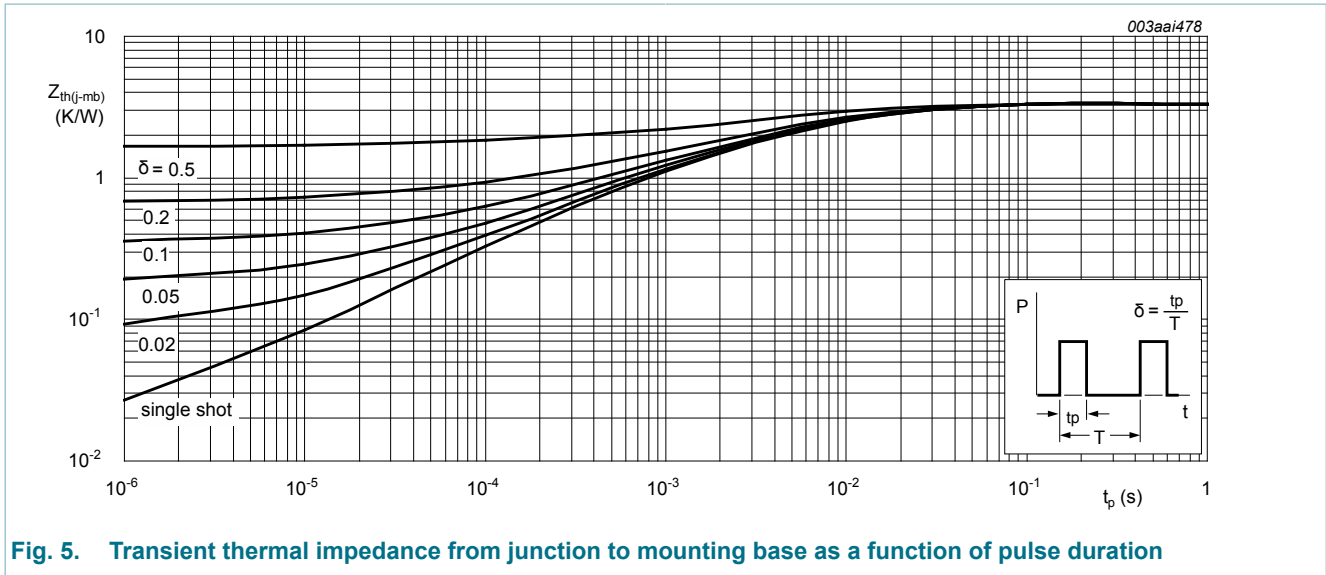


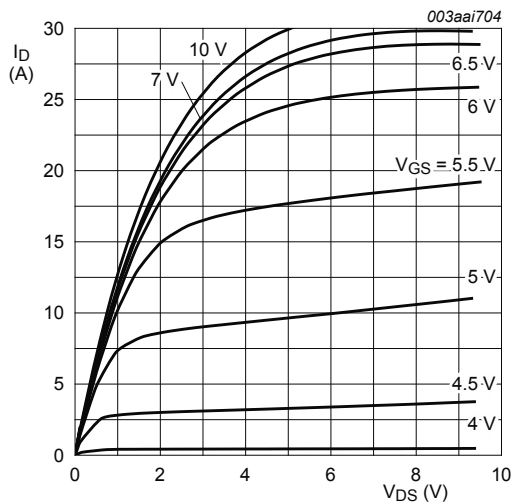
Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 10. Characteristics

Table 7. Characteristics

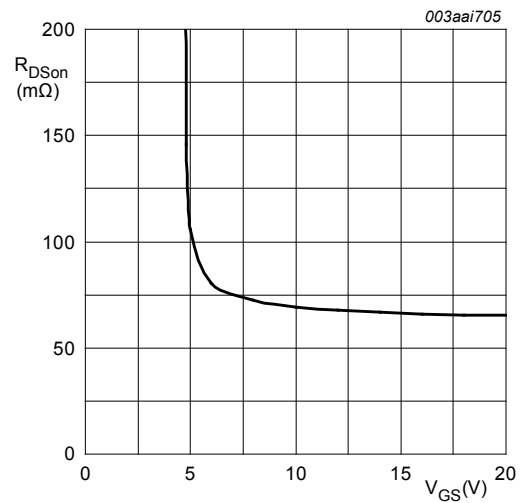
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	80	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	72	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 9; Fig. 10</a>	2.4	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C;$ <a href="#">Fig. 9</a>	-	-	4.5	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C;$ <a href="#">Fig. 9</a>	1	-	-	V
$I_{DSS}$	drain leakage current	$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.01	1	$\mu A$
		$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ C$	-	-	500	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 11</a>	-	54	72	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 175 \text{ }^\circ C;$ <a href="#">Fig. 11; Fig. 12</a>	-	-	181	mΩ
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 5 \text{ A}; V_{DS} = 64 \text{ V}; V_{GS} = 10 \text{ V};$ $T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 13; Fig. 14</a>	-	9.8	-	nC
$Q_{GS}$	gate-source charge		-	1.6	-	nC
$Q_{GD}$	gate-drain charge		-	3.3	-	nC

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{iss}$	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz};$	-	475	633	pF
$C_{oss}$	output capacitance	$T_j = 25\text{ °C};$ <a href="#">Fig. 15</a>	-	77	93	pF
$C_{rss}$	reverse transfer capacitance		-	57	78	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 60\text{ V}; R_L = 10\text{ }\Omega; V_{GS} = 10\text{ V};$	-	4	-	ns
$t_r$	rise time	$R_{G(ext)} = 5\text{ }\Omega; T_j = 25\text{ °C}$	-	4	-	ns
$t_{d(off)}$	turn-off delay time		-	8	-	ns
$t_f$	fall time		-	5	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 5\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ °C};$ <a href="#">Fig. 16</a>	-	0.84	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 5\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$	-	22	-	ns
$Q_r$	recovered charge	$V_{DS} = 25\text{ V}; T_j = 25\text{ °C}$	-	20	-	nC



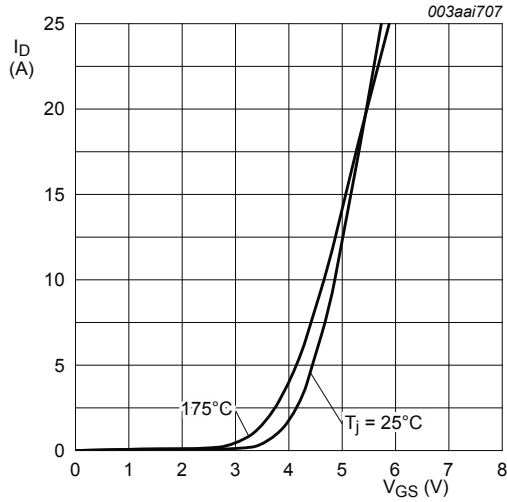
$T_j = 25\text{ °C}; t_p = 300\text{ }\mu\text{s}$

**Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values**



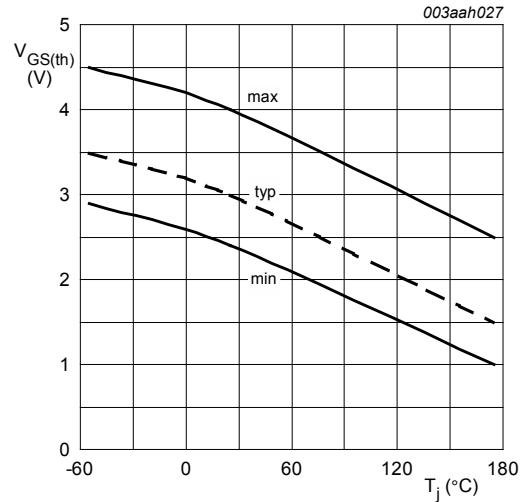
**Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values**

$T_j = 25\text{ °C}; I_D = 5\text{ A}$



**Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values**

$$V_{DS} = 10V$$



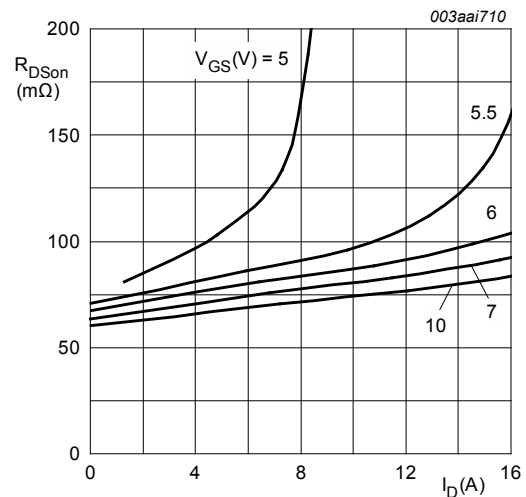
**Fig. 9. Gate-source threshold voltage as a function of junction temperature**

$$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$$



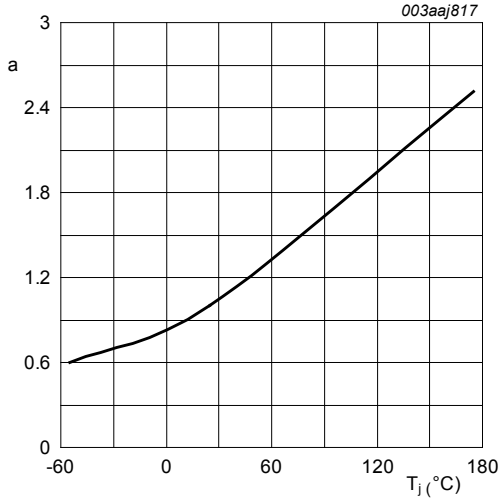
**Fig. 10. Sub-threshold drain current as a function of gate-source voltage**

$$T_j = 25^\circ C; V_{DS} = 5V$$



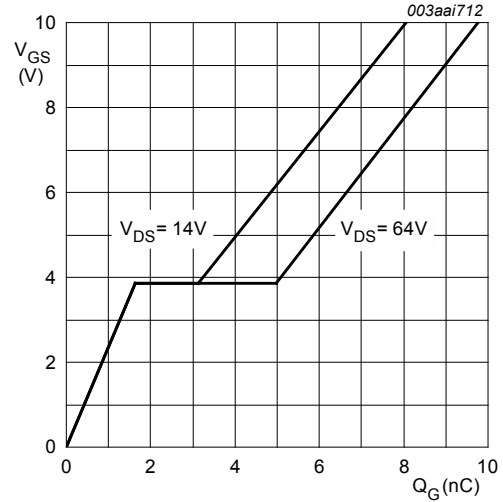
**Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature**

$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ C)}$$



**Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature**

$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^\circ\text{C})}}$$

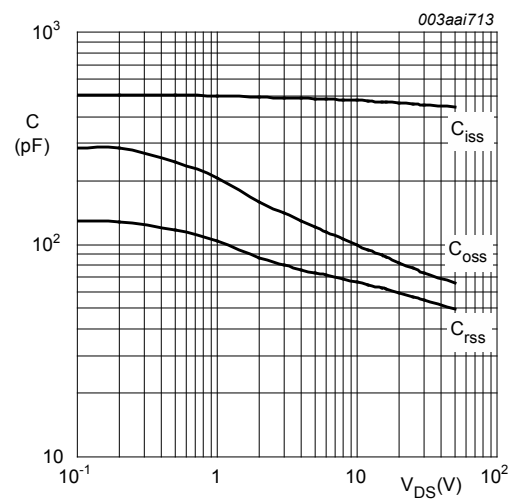


**Fig. 13. Gate-source voltage as a function of gate charge; typical values**

$$T_j = 25^\circ\text{C}; I_D = 5\text{A}$$



**Fig. 14. Gate charge waveform definitions**



**Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

$$V_{GS} = 0\text{V}; f = 1\text{MHz}$$



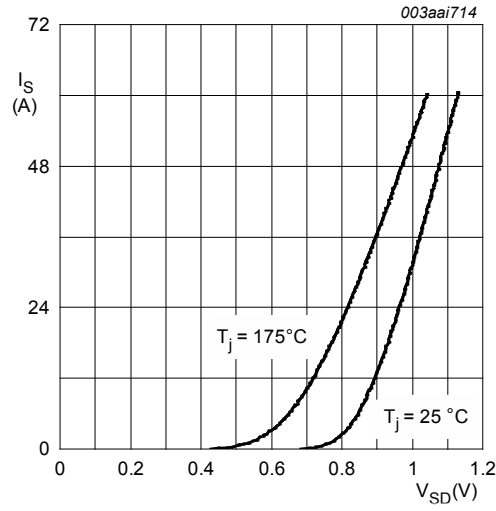


Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$$V_{GS} = 0V$$

### 11. Package outline

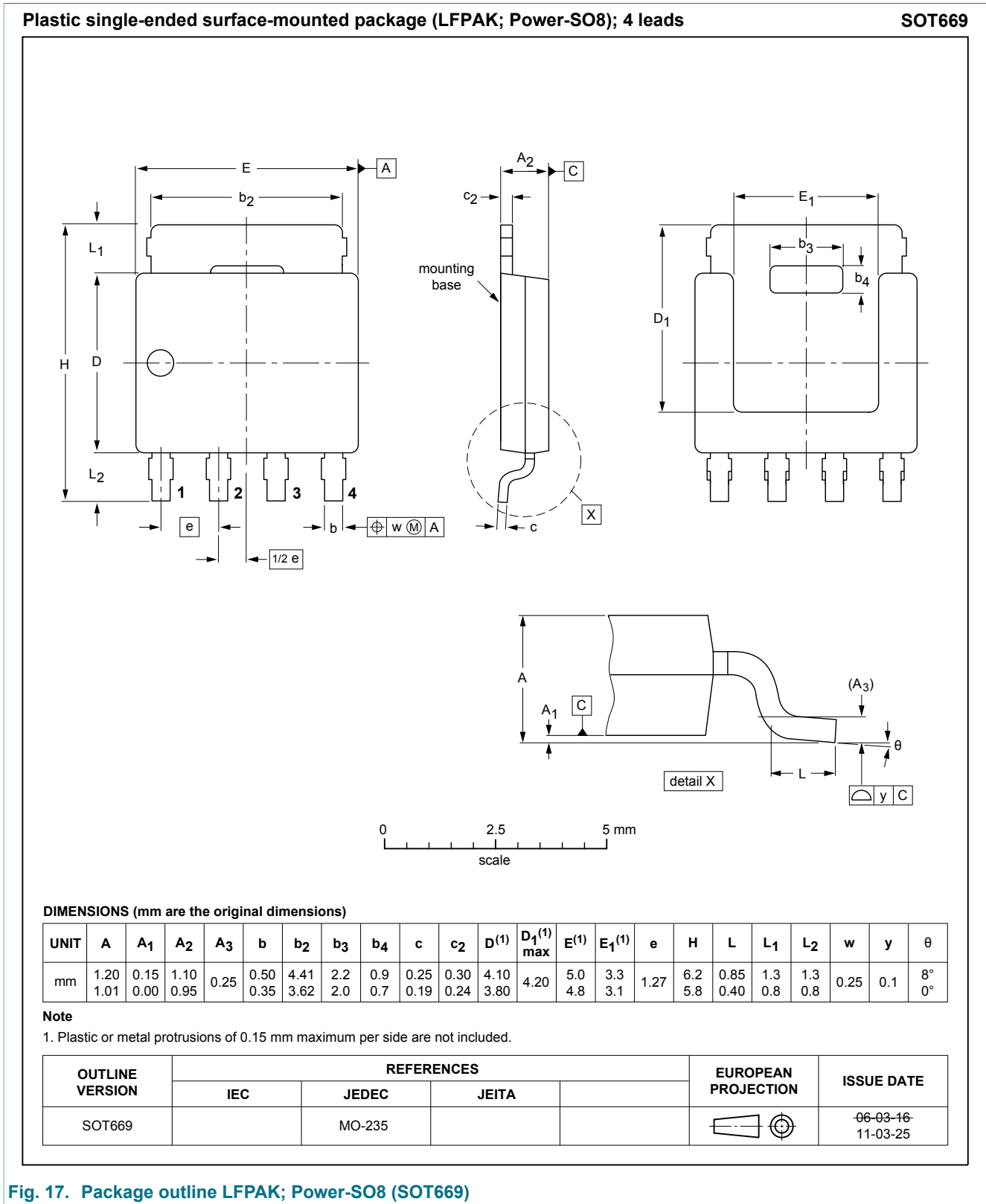


Fig. 17. Package outline LPAK; Power-SO8 (SOT669)

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