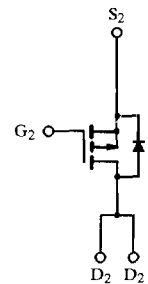
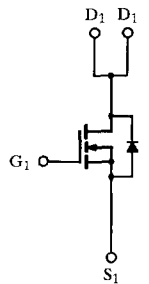
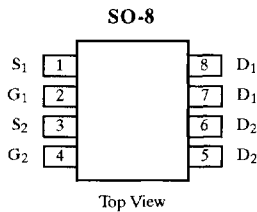


Dual Enhancement-Mode MOSFET (N- and P-Channel)

Product Summary

	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
N-Channel	20	0.125 @ $V_{GS} = 10$ V	± 3.0
		0.250 @ $V_{GS} = 4.5$ V	± 2.0
P-Channel	-20	0.160 @ $V_{GS} = -10$ V	± 2.8
		0.300 @ $V_{GS} = -4.5$ V	± 2.0



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Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage	V_{DS}	20	-20	V
Gate-Source Voltage	V_{GS}	± 20	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$)	I_D	$T_A = 25^\circ\text{C}$	± 3.0	A
		$T_A = 70^\circ\text{C}$	± 2.5	
Pulsed Drain Current	I_{DM}	± 10	± 10	
Continuous Source Current (Diode Conduction)	I_S	1.6	-1.6	
Maximum Power Dissipation (Surface Mounted on FR4 Board)	P_D	$T_A = 25^\circ\text{C}$		W
		$T_A = 70^\circ\text{C}$		
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$

Thermal Resistance Ratings

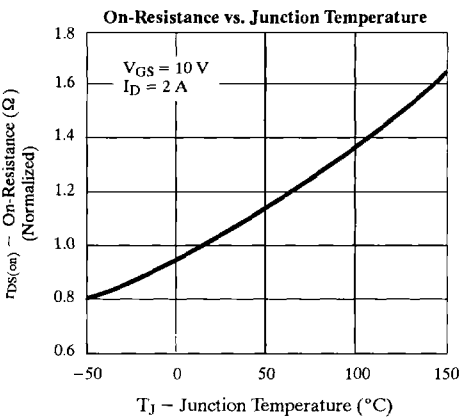
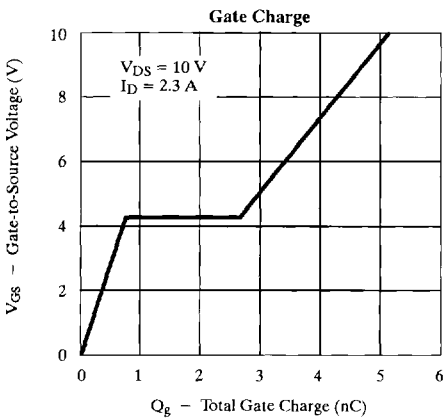
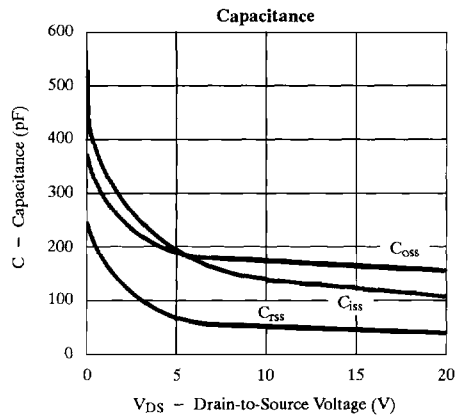
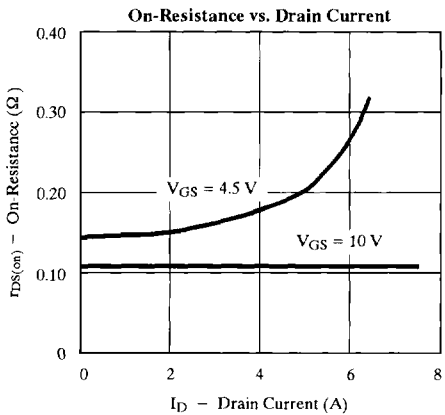
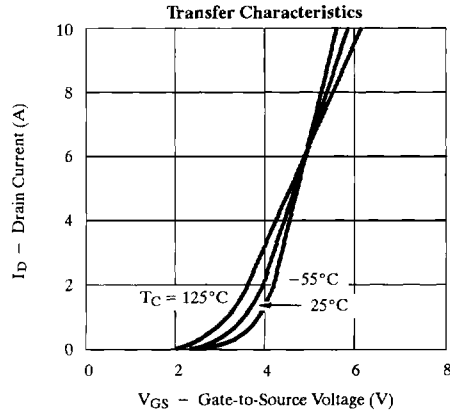
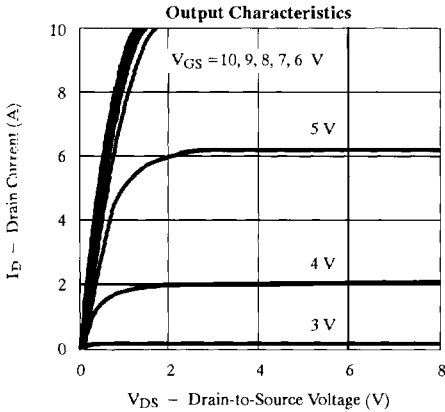
Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient (Surface Mounted on FR4 Board)	R_{thJA}	62.5	$^\circ\text{C/W}$

Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit	
Static							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	N-Ch	1.0		V	
		$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	P-Ch	-1.0			
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 16 \text{ V}, V_{GS} = 0 \text{ V}$	N-Ch			2	μA
		$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}$	P-Ch			-2	
		$V_{DS} = 16 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$	N-Ch			25	
		$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$	P-Ch			-25	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \geq 5 \text{ V}, V_{GS} = 10 \text{ V}$	N-Ch	10		A	
		$V_{DS} \leq -5 \text{ V}, V_{GS} = -10 \text{ V}$	P-Ch	-10			
		$V_{DS} \geq 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	N-Ch	2			
		$V_{DS} \leq -5 \text{ V}, V_{GS} = -4.5 \text{ V}$	P-Ch	-2			
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = 10 \text{ V}, I_D = 3.0 \text{ A}$	N-Ch		0.100	0.125	Ω
		$V_{GS} = -10 \text{ V}, I_D = 3.0 \text{ A}$	P-Ch	0.100	0.130	0.160	
		$V_{GS} = 6 \text{ V}, I_D = 2.0 \text{ A}$	N-Ch		0.120	0.160	
		$V_{GS} = -6 \text{ V}, I_D = 2.0 \text{ A}$	P-Ch	0.120	0.160	0.200	
		$V_{GS} = 4.5 \text{ V}, I_D = 1.5 \text{ A}$	N-Ch		0.160	0.250	
		$V_{GS} = -4.5 \text{ V}, I_D = 1.5 \text{ A}$	P-Ch		0.20	0.300	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15 \text{ V}, I_D = 3.0 \text{ A}$	N-Ch		3.7	S	
		$V_{DS} = -15 \text{ V}, I_D = -3.0 \text{ A}$	P-Ch		3.0		
Diode Forward Voltage ^b	V_{SD}	$I_S = 1.25 \text{ A}, V_{GS} = 0 \text{ V}$	N-Ch		0.9	1.2	V
		$I_S = -1.25 \text{ A}, V_{GS} = 0 \text{ V}$	P-Ch		-1.4	-1.6	
Dynamic^a							
Total Gate Charge	Q_g	$V_{DS} = 10 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 2.3 \text{ A}$ $V_{DS} = -10 \text{ V}, V_{GS} = -10 \text{ V}, I_D = -2.3 \text{ A}$	N-Ch		5.2	25	nC
Gate-Source Charge	Q_{gs}		P-Ch		9.4	25	
			N-Ch		0.8		
Gate-Drain Charge	Q_{gd}		P-Ch		1.3		
		N-Ch		2.0			
Turn-On Delay Time	$t_{d(on)}$	P-Ch		2.0			
		N-Ch		5	15		
Rise Time	t_r	N-Ch		12	40	ns	
		P-Ch		10	20		
Turn-Off Delay Time	$t_{d(off)}$	N-Ch		19	40		
		P-Ch		25	50		
Fall Time	t_f	N-Ch		42	90		
		P-Ch		22	50		
Source-Drain Reverse Recovery Time	t_{rr}	N-Ch		27	50		
		P-Ch		69	100		
		$I_F = 1.25 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$	N-Ch		69	100	
			P-Ch		69	100	

Notes

- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.

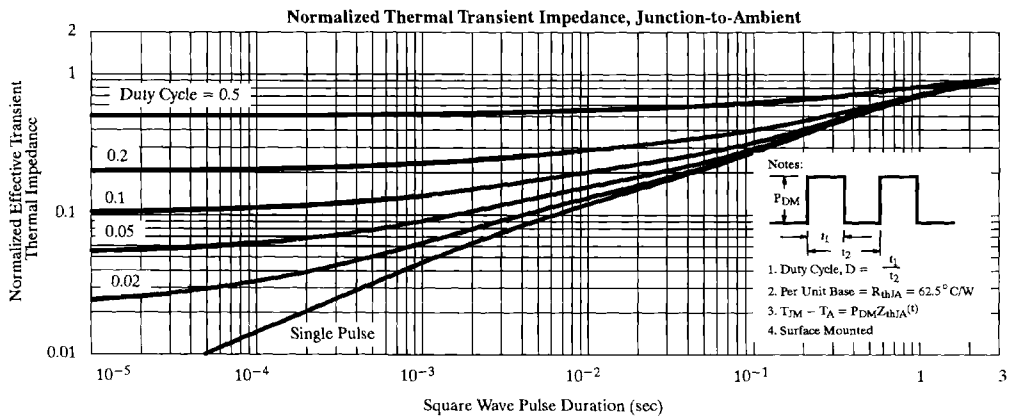
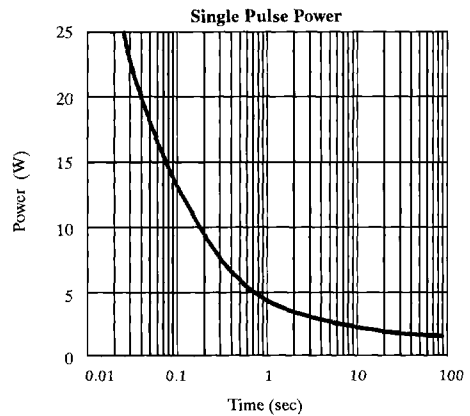
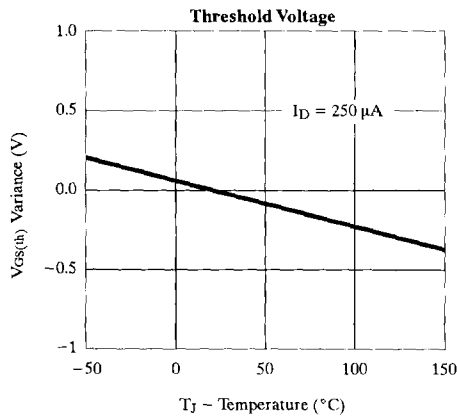
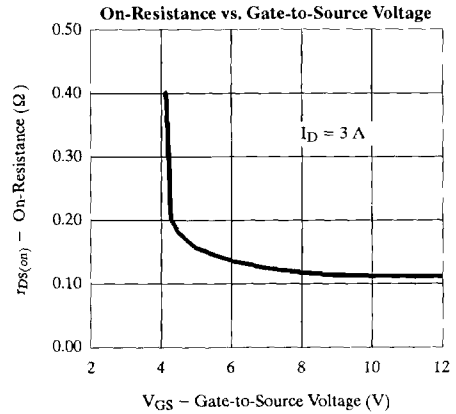
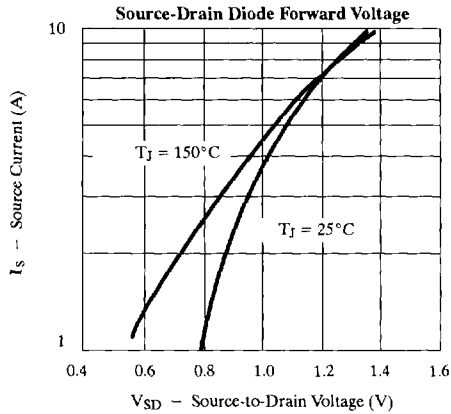


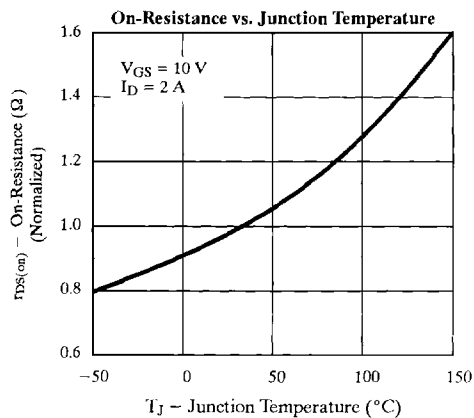
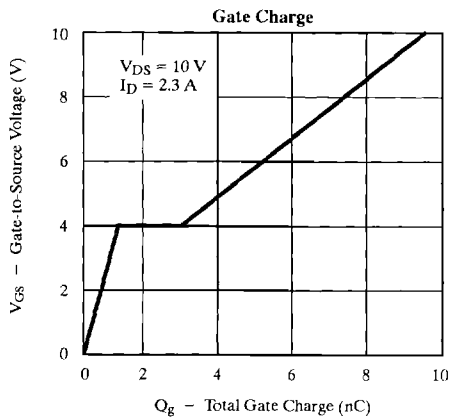
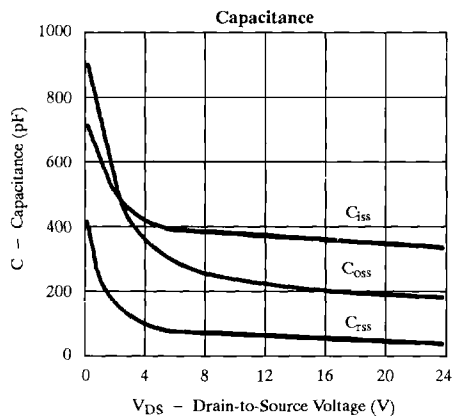
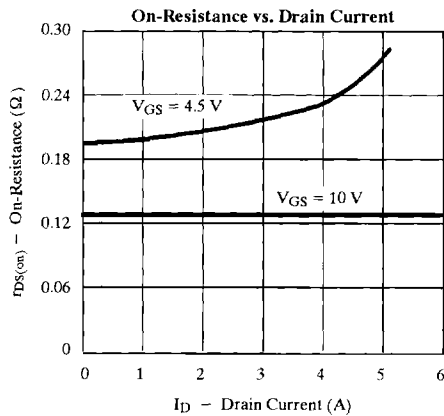
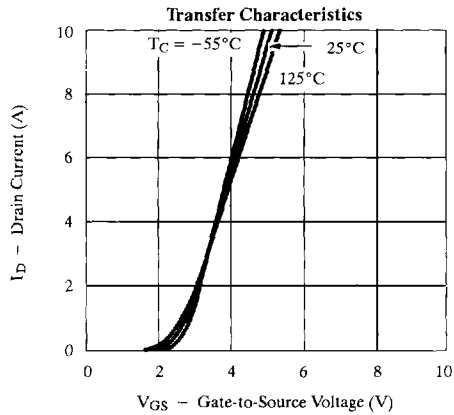
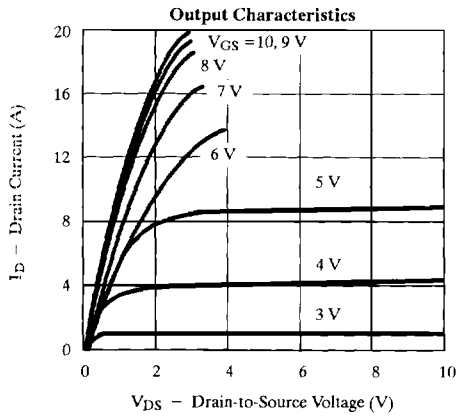
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Typical Characteristics (25°C Unless Otherwise Noted)

N-Channel





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