Dual-Core LEON3-FT SPARC V8 Processor
GR712RC
Data Sheet

Features

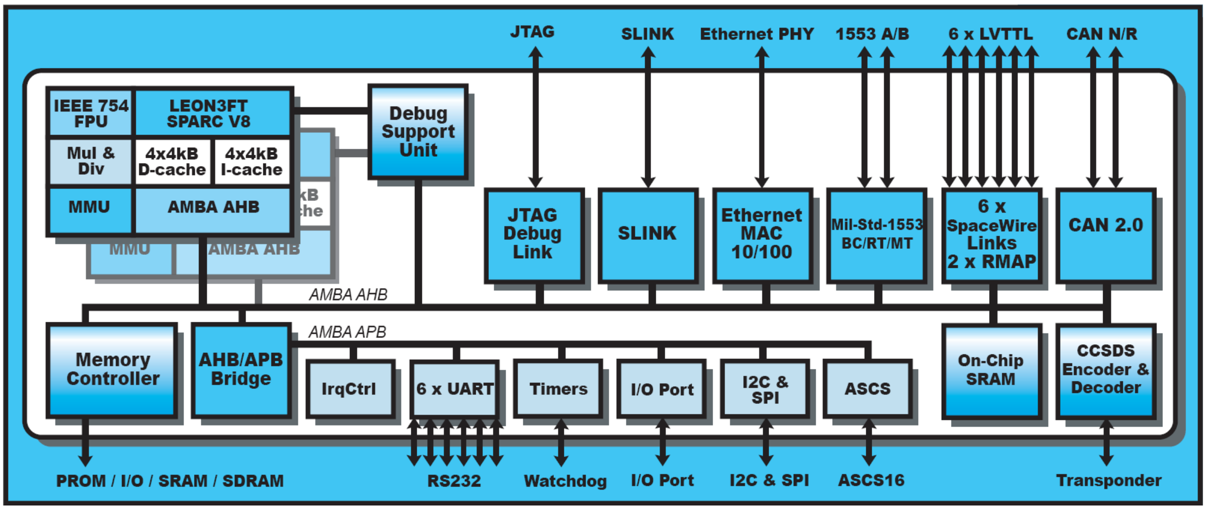
- Dual-core SPARC V8 integer unit, each with 7-stage pipeline, 8 register windows, 4x4 KiB multi-way instruction cache, 4x4 KiB multi-way data cache, branch prediction, hardware multiplier and divider, power-down mode, hardware watchpoints, single-vector trapping, SPARC reference memory management unit, etc.
- Two high-performance double precision IEEE-754 floating point units
- EDAC protected (8-bit BCH and 16-bit Reed-Solomon) interface to multiple 8/32-bits PROM/SRAM/SDRAM memory banks
- Advanced on-chip debug support unit
- 192 KiB EDAC protected on-chip memory
- Multiple SpaceWire links with RMAP target
- Redundant 1553 BC/RT/MT interfaces
- Redundant CAN 2.0 interfaces
- 10/100 Ethernet MAC with RMII interface
- SPI, I^2C, ASCS16 (STR), SLINK interfaces
- CCSDS/ECSS Telemetry and Telecommand
- UARTs, Timers & Watchdog, GPIO ports, Interrupt controllers, Status registers, JTAG, etc.
- Configurable I/O switch matrix

Description

The GR712RC is an implementation of the dual-core LEON3FT SPARC V8 processor using RadSafe™ technology. The fault tolerant design of the processor in combination with the radiation tolerant technology provides total immunity to radiation effects.

Specification

- CQFP240 package
- Total Ionizing Dose (TID) up to 300 krad(Si)
- Proven Single-Event Latch-Up (SEL) immunity
- Proven Single-Event Upset (SEU) tolerance
- 1.8V & 3.3V supply
- 15 mW/MHz processor core power consumption
- 100 MHz system frequency
- 200 Mbps SpaceWire links
- 10 Mbps CCSDS Telecommand link
- 50 Mbps CCSDS Telemetry link



Applications

GR712RC is an advanced system-on-chip, targeting high reliability rad-hard space, aeronautics and military applications.

It incorporates a dual-core LEON3-FT SPARC V8 processor and is implemented using Ramon Chips' RadSafe™ library on Tower Semiconductors' standard 180 nm CMOS technology.

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1 Introduction

1.1 Overview

GR712RC is a dual-core LEON3-FT SPARC V8 processor, with advanced interface protocols, dedicated for high reliability Rad-Hard aerospace applications.

The GR712RC is fabricated at Tower Semiconductors Ltd., using standard 180 nm CMOS technology. It employs radiation-hard-by-design methods from Aeroflex Gaisler and the RadSafe™ technology from Ramon Chips Ltd., enabling superior radiation hardness together with excellent low-power performance.

The LEON3-FT processors provide hardware support for cache coherency, processor enumeration and interrupt steering. Each processor core includes a SPARC Reference Memory Management Unit (SRMMU) and an IEEE-754 compliant double-precision FPU for floating-point operations. It can be utilized in symmetric or asymmetric multiprocessing mode.

The GR712RC architecture is centered around the AMBA Advanced High-speed Bus (AHB), to which the two LEON3-FT processors and other high-bandwidth units are connected. Low-bandwidth units are connected to the AMBA Advanced Peripheral Bus (APB) which is accessed through an AHB to APB bridge.

GR712RC is provided in a 240-pin, 0.5 mm pitch high-reliability ceramic quad flat package (CQFP).

This document is complemented by the *GR712RC Dual-Core LEON3-FT SPARC V8 Processor - User's Manual* from Aeroflex Gaisler [UM], which provides information related to software integration and development.

1.2 Key features

- Technology: 180 nm standard CMOS, Tower Semiconductors Ltd.
- Library: 180 nm RadSafe™, Ramon Chips Ltd.
- Package:
  - 240 pin CQFP, 0.5 mm pitch, 32 mm °* 32 mm, hermetically sealed,
    delivered with flat pins and insulating lead-frame for customer trim and fold
  - Core voltage 1.8V +/- 0.15V, I/O voltage 3.3V +/- 0.3V
  - -55ºC to +125ºC temperature range
- Radiation tolerance:
  - TID: 300 krad (Si)
  - SEL: > 118 MeV-cm^2/mg
  - SEU: proven tolerance with hardened flip-flops and error correction on all on-chip memories
  - Error detection and correction on external memories
- Maximum system clock frequency of 100 MHz (depending on external memory choice)
  - Optional 2x internal system frequency multiplication by an all-digital DLL
  - Optional 2x or 4x internal SpaceWire frequency multiplication by an all-digital DLL
  - Clock-gating for each major core

- Two LEON3-FT SPARC V8 compliant 32-bit processors, each with:
  - SPARC reference memory management unit (SRMMU) with 32 TLB entries
  - High-performance double-precision IEEE-754 floating point co-processor (GRFPU)
  - 16 KiB multi-way instruction cache and 16 KiB multi-way data cache
- Internal on-chip high speed AMBA (AHB) bus
- Instruction trace and AMBA (AHB) trace buffers for debugging
- Timer unit with four 32-bit timers including watchdog
- Secondary timer unit with four 32-bit timers
- Primary and secondary interrupt controller for 31 interrupts
- On-chip 192 KiB memory block with EDAC
- External memory support:
  - Bus width: 8 bits, or 32 bit data plus 8/16 bits for EDAC checkbits, 24 bit address
  - 8 bit BCH EDAC for SRAM and PROM, 16 bit Reed-Solomon EDAC for SDRAM
  - Memory types: SRAM, SDRAM, PROM / EEPROM / NOR-FLASH and I/O address space
  - Programmable wait-states:
    - SRAM read/write cycle 2 - 5 clock cycles
    - PROM / EEPROM / NOR-FLASH read cycle 2 - 32 clock periods
    - One idle clock period between accesses to SRAM and PROM
- Debug Support Unit (DSU) accessed via JTAG and SpaceWire RMAP targets
- Two SpaceWire ports with RMAP targets, maximum 200 Mbps full-duplex data rate
- Configurable I/O selection matrix, connecting a subset of available I/O units to 67 shared pins:
  - Four SpaceWire ports, maximum 200 Mbps full-duplex data rate
  - Redundant MIL-STD-1553B BRM (BC/RT/BM) interface
  - Two CAN 2.0B bus controllers
  - Six UART ports, with 8-byte FIFO
  - Ethernet MAC with RMII 10/100 Mbps port
  - SPI master serial port
  - I2C master serial port
  - ASCS16 (STR) serial port
  - SLINK 6 MHz serial port
  - CCSDS / ECSS Telecommand decoder (five input channels), maximum 10 Mbps input rate
  - CCSDS / ECSS Telemetry encoder, maximum 50 Mbps output rate
  - 26 input and 38 input/output general purpose ports

1.3 Signal overview

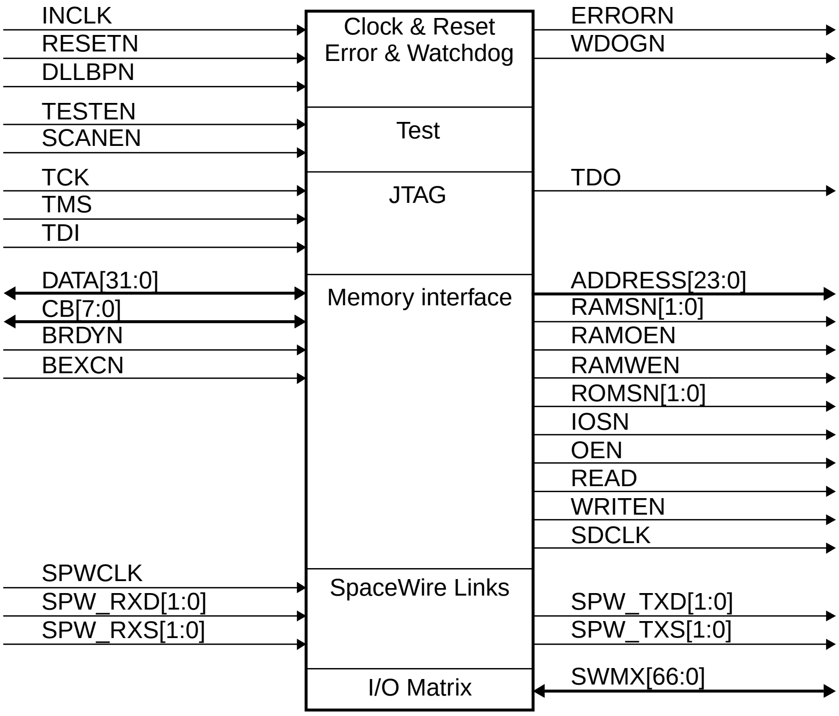

Figure 1. Signal overview

1.4 Signal description

The external signals are described in table 1.

Table 1. External signals

Name	Usage	Direction	Polarity
INCLK	Main system clock	In	-
DLLBPN	DLL bypass	In	Low
RESETN	System reset	In	Low
SCANEN	Scan enable (tie to ground)	In	High
TESTEN	Test enable (tie to ground)	In	High
ERRORN	Processor error mode	Out-Tri	Low
WDOGN	Watchdog output	Out-Tri	Low
TCK	JTAG Test Clock	In	-
TMS	JTAG Test Mode	In	High
TDI	JTAG Test Data Input	In	-
TDO	JTAG Test Data Output	Out	-
ADDRESS[23:0]	Memory address	Out	-
DATA[31:0]	Memory data bus	In/Out	-
CB[7:0]	Memory checkbits	In/Out	-
RAMSN[1:0]	SRAM chip selects	Out	Low
RAMOEN	SRAM output enable	Out	Low
RAMWEN	SRAM write enable strobe	Out	Low
OEN	PROM, I/O output enable	Out	Low
WRITEN	PROM, I/O write strobe	Out	Low
READ	SRAM, PROM I/O read indicator [1)]	Out	High
IOSN	I/O area chip select	Out	Low
ROMSN[1:0]	PROM chip selects	Out	Low
BRDYN	Bus ready	In	Low
BEXCN	Bus exception	In	Low
SDCLK	SDRAM clock	Out	-
SPWCLK	SpaceWire receiver and transmitter clock	In	-
SPW_RXD[1:0]	SpaceWire Data input	In	High
SPW_RXS[1:0]	SpaceWire Strobe input	In	High
SPW_TXD[1:0]	SpaceWire Data output	Out	High
SPW_TXS[1:0]	SpaceWire Strobe output	Out	High
SWMX[66:0]	I/O switch matrix	In/Out	-

Note 1: The READ signal may also change value during SDRAM accesses.

1.5 I/O switch matrix overview

The I/O switch matrix provides access to several I/O units. When an interface is not activated, its pins automatically become general purpose I/O. After reset, all I/O switch matrix pins are defined as I/O until programmed otherwise. Note that some pins are input only, some are output only, and the rest are both input and output, as described in table 3. The enabling of the I/O units is described in [UM].

Figure 2 shows how the various I/O units are connected to the I/O switch matrix.

Table 2 shows examples of possible configurations using the I/O switch matrix. Note that two SpaceWire interfaces are always available outside the I/O switch matrix.

Table 3 shows a listing of all pins in the I/O switch matrix, indicating the priority amongst them.

Table 4 shows a listing of pin utilization per I/O unit.

Table 5 shows a listing of pins in the I/O switch matrix grouped per function (GPIO is not listed).

Table 6 shows a complete listing of conflicts between I/O units (GPIO is not listed).

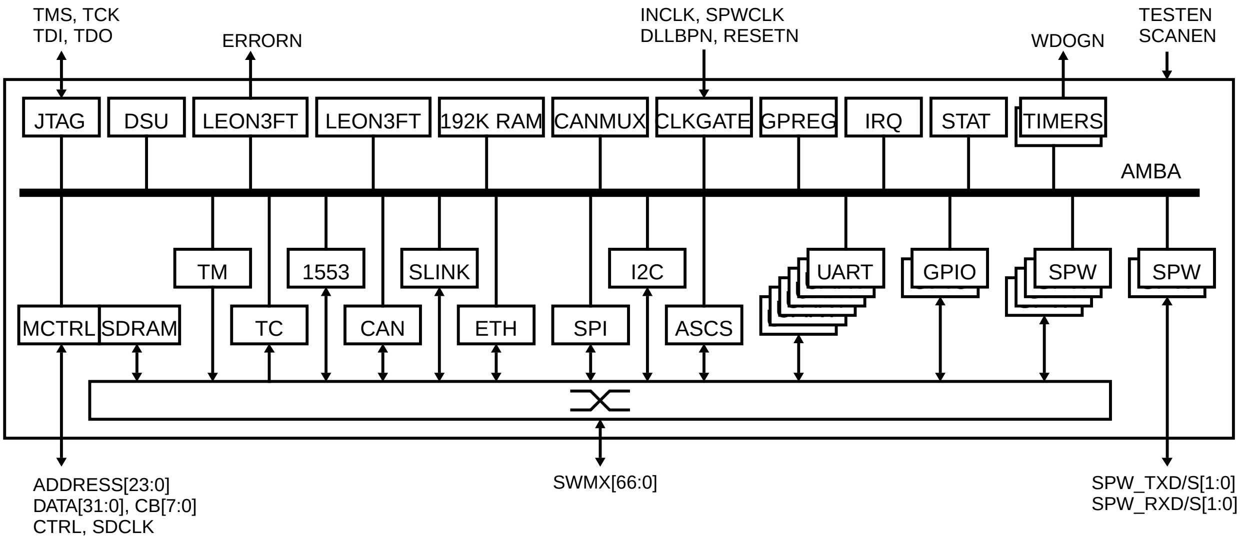

Figure 2. Architectural block diagram showing connections to the I/O switch matrix

Table 2. Example of possible configurations using the I/O switch matrix. Note that other configurations are also possible.

Interface type	**Example configuration**					
	CF0	**CF1**	**CF2**	**CF3**	**CF4**	**CF5**
SDRAM with or without Reed-Solomon		1	1	1	1	1
UART	6	4	6	6	6	6
SpaceWire	6	4	2	2	4	3
Ethernet					1	1
MIL-STD-1553B BC/RT/BM	1					
I2C	1		1	1	1	1
SPI	1				1	1
SLINK			1	1		
ASCS16			1			
CCSDS/ECSS TC & TM		1				

Table 3. I/O switch matrix pin description, defining the order of priority for outputs and input/outputs, with the highest priority for each pin listed first.

Pin no.	Pin name	Pin function	Polarity	Reset value	Dir.	Description
4	SWMX[0]	UART_TX[0]	-	High	Out	UART Transmit 0
3	SWMX[1]	UART_RX[0]	-		In	UART Receive 0
2	SWMX[2]	UART_TX[1]	-	High	Out	UART Transmit 1
1	SWMX[3]	UART_RX[1]	-		In	UART Receive 1
		GPIO[0]	-		In	GPIO 1 Register, bit 0 (input only)
240	SWMX[4]	UART_TX[2]	-	High-Z	Out	UART Transmit 2
		GPIO[1]	-	High-Z	In/Out	GPIO 1 Register, bit 1
		MCFG3[8]	-		In	At reset, bit 8 in MCFG3 register in the memory controller is set from this input.
239	SWMX[5]	UART_RX[2]	-		In	UART Receive 2
		GPIO[2]	-		In	GPIO 1 Register, bit 2 (input only)
238	SWMX[6]	UART_TX[3]	-	High-Z	Out	UART Transmit 3
		GPIO[3]	-	High-Z	In/Out	GPIO 1 Register, bit 3
		MCFG1[9]	-		In	At reset, bit 9 in MCFG1 register in the memory controller is set from this input
233	SWMX[7]	UART_RX[3]	-		In	UART Receive 3
		GPIO[4]	-		In	GPIO 1 Register, bit 4 (input only)
232	SWMX[8]	UART_TX[4]	-	High-Z	Out	UART Transmit 4
		TMDO	-	High-Z	Out	Telemetry Data Out
		GPIO[5]	-	High-Z	In/Out	GPIO 1 Register, bit 5
231	SWMX[9]	UART_RX[4]	-		In	UART Receive 4
		TMCLKI	Rising		In	Telemetry Clock Input
		GPIO[6]	-		In	GPIO 1 Register, bit 6 (input only)
230	SWMX[10]	UART_TX[5]	-	High-Z	Out	UART Transmit 5
		TMCLKO	-	High-Z	Out	Telemetry Clock Output
		GPIO[7]	-	High-Z	In/Out	GPIO 1 Register, bit 7
229	SWMX[11]	UART_RX[5]	-		In	UART Receive 5
		TCACT[0]	High		In	Telecommand Active 0
		GPIO[8]	-		In	GPIO 1 Register, bit 8 (input only)
228	SWMX[12]	SPW_TXS[4]	High	High-Z	Out	SpaceWire Transmit Strobe 4
		SDCSN[0]	Low	High-Z	Out	SDRAM Select 0
		GPIO[9]	-	High-Z	In/Out	GPIO 1 Register, bit 9
227	SWMX[13]	SPW_TXD[4]	High	High-Z	Out	SpaceWire Transmit Data 4
		SDCSN[1]	Low	High-Z	Out	SDRAM Select 1
		GPIO[10]	-	High-Z	In/Out	GPIO 1 Register, bit 10
226	SWMX[14]	SPW_RXS[4]	High		In	SpaceWire Receive Strobe 4
		TCCLK[0]	Rising		In	Telecommand Clock 0
		A16DASA	-		In	ASCS DAS A - Slave data in
		GPIO[11]	-		In	GPIO 1 Register, bit 11 (input only)
225	SWMX[15]	SPW_RXD[4]	High		In	SpaceWire Receive Data 4
		TCD[0]	-		In	Telecommand Data 0
		A16DASB	-		In	ASCS DAS B - Slave data in
		GPIO[12]	-		In	GPIO 1 Register, bit 12 (input only)
220	SWMX[16]	SPW_TXS[2]	High	High-Z	Out	SpaceWire Transmit Strobe 2
		CANTXA	-	High-Z	Out	CAN Transmit A
		GPIO[13]	-	High-Z	In/Out	GPIO 1 Register, bit 13

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Pin no.	Pin name	Pin function	Polarity	Reset value	Dir.	Description
219	SWMX[17]	SPW_TXD[2]	High	High-Z	Out	SpaceWire Transmit Data 2
		CANTXB	-	High-Z	Out	CAN Transmit B
		GPIO[14]	-	High-Z	In/Out	GPIO 1 Register, bit 14
218	SWMX[18]	SPW_RXS[2]	High		In	SpaceWire Receive Strobe 2
		CANRXA	-		In	CAN Receive A
		GPIO[15]	-		In	GPIO 1 Register, bit 15 (input only)
217	SWMX[19]	SPW_RXD[2]	High		In	SpaceWire Receive Data 2
		CANRXB	-		In	CAN Receive B
		GPIO[16]	-		In	GPIO 1 Register, bit 16 (input only)
203	SWMX[20]	SPW_TXS[3]	High	High-Z	Out	SpaceWire Transmit Strobe 3
		SLSYNC	High	High-Z	Out	SLINK SYNC
		GPIO[17]	-	High-Z	In/Out	GPIO 1 Register, bit 17
202	SWMX[21]	SPW_TXD[3]	High	High-Z	Out	SpaceWire Transmit Data 3
		A16ETR	High	High-Z	Out	ASCS ETR - Synchronization signal
		GPIO[18]	-	High-Z	In/Out	GPIO 1 Register, bit 18
201	SWMX[22]	SPW_RXS[3]]	High		In	SpaceWire Receive Strobe 3
		GPIO[19]	-		In	GPIO 1 Register, bit 19 (input only)
200	SWMX[23]	SPW_RXD[3]	High		In	SpaceWire Receive Data 3
		GPIO[20]	-		In	GPIO 1 Register, bit 20 (input only)
197	SWMX[24]	SPW_TXD[5]	High	High-Z	Out	SpaceWire Transmit Data 5
		SDDQM[0]	High	High-Z	Out	SDRAM Data Mask 0, corresponds to DATA[7:0]
		GPIO[21]	-	High-Z	In/Out	GPIO 1 Register, bit 21
196	SWMX[25]	SPW_TXS[5]	High	High-Z	Out	SpaceWire Transmit Strobe 5
		SDDQM[1]	High	High-Z	Out	SDRAM Data Mask 1, corresponds to DATA[15:8]
		GPIO[22]	-	High-Z	In/Out	GPIO 1 Register, bit 22
193	SWMX[26]	SPW_RXS[5]	High		In	SpaceWire Receive Strobe 5
		TCRFAVL[0]	High		In	Telecommand RF Available 0
		GPIO[23]	-		In	GPIO 1 Register, bit 23 (input only)
192	SWMX[27]	SPW_RXD[5]	High		In	SpaceWire Receive Data 5
		TCCLK[1]	Rising		In	Telecommand Clock 1
		GPIO[24]	-		In	GPIO 1 Register, bit 24 (input only)
191	SWMX[28]	1553RXENA	High	High-Z	Out	MIL-STD-1553B Receive Enable A
		-		High-Z	Out	Proprietary, enabled by CAN
		RMTXD[0]	-	High-Z	Out	Ethernet Transmit Data 0
		GPIO[25]	-	High-Z	In/Out	GPIO 1 Register, bit 25
190	SWMX[29]	1553TXA	High	High-Z	Out	MIL-STD-1553B Transmit Positive A
		-		High-Z	Out	Proprietary, enabled by CAN
		RMTXD[1]	-	High-Z	Out	Ethernet Transmit Data 1
		GPIO[26]	-	High-Z	In/Out	GPIO 1 Register, bit 26
189	SWMX[30]	1553RXA	High		In	MIL-STD-1553B Receive Positive A
		TCD[1]	-		In	Telecommand Data 1
		RMRXD[0]	-		In	Ethernet Receive Data 0
		GPIO[27]	-		In	GPIO 1 Register, bit 27 (input only)

Table 3. I/O switch matrix pin description, defining the order of priority for outputs and input/outputs, with the highest priority for each pin listed first.

Pin no.	**Pin name**	**Pin function**	**Polarity**	**Reset value**	**Dir.**	**Description**
188	SWMX[31]	1553RXNA	Low		In	MIL-STD-1553B Receive Negative A
		TCACT[1]	High		In	Telecommand Active 1
		RMRXD[1]	-		In	Ethernet Receive Data 1
		GPIO[28]	-		In	GPIO 1 Register, bit 28 (input only)
185	SWMX[32]	1553TXNA	Low	High-Z	Out	MIL-STD-1553B Transmit Negative A
		-		High-Z	Out	Proprietary, enabled by CAN
		RMTXEN	High	High-Z	Out	Ethernet Transmit Enable
		GPIO[29]	-	High-Z	In/Out	GPIO 1 Register, bit 29
184	SWMX[33]	1553TXINHA	High	High-Z	Out	MIL-STD-1553B Transmit Inhibit A
		-		High-Z	Out	Proprietary, enabled by CAN
		GPIO[30]	-	High-Z	In/Out	GPIO 1 Register, bit 30
183	SWMX[34]	1553RXB	High		In	MIL-STD-1553B Receive Positive B
		TCRFAVL[1]	High		In	Telecommand RF Available 1
		RMCRSDV	High		In	Ethernet Carrier Sense / Data Valid
		GPIO[31]	-		In	GPIO 1 Register, bit 31 (input only)
182	SWMX[35]	1553RXNB	Low		In	MIL-STD-1553B Receive Negative B
		TCCLK[2]	Rising		In	Telecommand Clock 2
		RMINTN	Low		In	Ethernet Management Interrupt
		GPIO[32]	-		In	GPIO 2 Register, bit 0 (input only)
179	SWMX[36]	1553RXENB	High	High-Z	Out	MIL-STD-1553B Receive Enable B
		A16MCS	High	High-Z	Out	ASCS MCS - TM start/stop signal
		RMMDIO	-	High-Z	In/Out	Ethernet Media Interface Data
		GPIO[33]	-	High-Z	In/Out	GPIO 2 Register, bit 1
178	SWMX[37]	1553TXB	High	High-Z	Out	MIL-STD-1553B Transmit Positive B
		A16HS	High	High-Z	Out	ASCS HS - TM/TC serial clock
		RMMDC	-	High-Z	Out	Ethernet Media Interface Clock
		GPIO[34]	-	High-Z	In/Out	GPIO 2 Register, bit 2
		SpaceWire clock divisor registers	-		In	At reset, bits 8 and 0 in the clock divisor register of the SpaceWire interfaces are set from this input
177	SWMX[38]	1553CK	-		In	MIL-STD-1553B Clock
		TCD[2]	-		In	Telecommand Data 2
		RMRFCLK	-		In	Ethernet Reference Clock
		GPIO[35]	-		In	GPIO 2 Register, bit 3 (input only)
176	SWMX[39]	TCACT[2]	High		In	Telecommand Active 2
		GPIO[36]	-		In	GPIO 2 Register, bit 4 (input only)
175	SWMX[40]	1553TXNB	Low	High-Z	Out	MIL-STD-1553B Transmit Negative B
		A16DCS	-	High-Z	Out	ASCS DCS - Slave data out
		GPIO[37]	-	High-Z	In/Out	GPIO 2 Register, bit 5
		SpaceWire clock divisor registers	-		In	At reset, bits 9 and 1 in the clock divisor register of the SpaceWire interfaces are set from this input
174	SWMX[41]	1553TXINHB	High	High-Z	Out	MIL-STD-1553B Transmit Inhibit B
		A16MAS	High	High-Z	Out	ASCS MAS - TM start/stop signal
		GPIO[38]	-	High-Z	In/Out	GPIO 2 Register, bit 6

Table 3. I/O switch matrix pin description, defining the order of priority for outputs and input/outputs, with the highest priority for each pin listed first.

Pin no.	Pin name	Pin function	Polarity	Reset value	Dir.	Description
173	SWMX[42]	TCRFAVL[2]	High		In	Telecommand RF Available 2
		GPIO[39]	-		In	GPIO 2 Register, bit 7 (input only)
172	SWMX[43]	-		High-Z	Out	Proprietary, enabled by CAN
		GPIO[40]	-	High-Z	In/Out	GPIO 2 Register, bit 8
		SpaceWire clock divisor registers	-		In	At reset, bits 10 and 2 in the clock divisor register of the SpaceWire interfaces are set from this input
169	SWMX[44]	SPICLK		High-Z	Out	SPI Clock
		SLO	-	High-Z	Out	SLINK Data Out
		GPIO[41]	-	High-Z	In/Out	GPIO 2 Register, bit 9
166	SWMX[45]	SPIMOSI	-	High-Z	Out	SPI Master Out Slave In
		SLCLK	High	High-Z	Out	SLINK Clock
		GPIO[42]	-	High-Z	In/Out	GPIO 2 Register, bit 10
		SpaceWire clock divisor registers	-		In	At reset, bits 11 and 3 in the clock divisor register of the SpaceWire interfaces are set from this input
165	SWMX[46]	TCCLK[3]	Rising		In	Telecommand Clock 3
		GPIO[43]	-		In	GPIO 2 Register, bit 11 (input only)
164	SWMX[47]	TCD[3]	-		In	Telecommand Data 3
		GPIO[44]	-		In	GPIO 2 Register, bit 12 (input only)
163	SWMX[48]	SDCASN	Low	High-Z	Out	SDRAM Column Address Strobe
		GPIO[45]	-	High-Z	In/Out	GPIO 2 Register, bit 13
162	SWMX[49]	SDRASN	Low	High-Z	Out	SDRAM Row Address Strobe
		GPIO[46]	-	High-Z	In/Out	GPIO 2 Register, bit 14
161	SWMX[50]	TCACT[3]	High		In	Telecommand Active 3
		GPIO[47]	-		In	GPIO 2 Register, bit 15 (input only)
160	SWMX[51]	SPIMISO			In	SPI Master In Slave Out
		TCRFAVL[3]	High		In	Telecommand RF Available 3
		SLI	-		In	SLINK Data In
		GPIO[48]	-		In	GPIO 2 Register, bit 16 (input only)
157	SWMX[52]	SDWEN	Low	High-Z	Out	SDRAM Write Enable
		GPIO[49]	-	High-Z	In/Out	GPIO 2 Register, bit 17
155	SWMX[53]	SDDQM[2]	High	High-Z	Out	SDRAM Data Mask 2, corresponds to DATA[23:16]
		GPIO[50]	-	High-Z	In/Out	GPIO 2 Register, bit 18
154	SWMX[54]	SDDQM[3]	High	High-Z	Out	SDRAM Data Mask 3, corresponds to DATA[31:24]
		GPIO[51]	-	High-Z	In/Out	GPIO 2 Register, bit 19
153	SWMX[55]	TCACT[4]	High		In	Telecommand Active 4
		GPIO[52]	-		In	GPIO 2 Register, bit 20 (input only)
144	SWMX[56]	TCRFAVL[4]	High		In	Telecommand RF Available 4
		GPIO[53]	-		In	GPIO 2 Register, bit 21 (input only)
143	SWMX[57]	I2CSDA		High-Z	In/Out	I2C Serial Data
		GPIO[54]	-	High-Z	In/Out	GPIO 2 Register, bit 22
		TCCLK[4]	Rising		In	Telecommand Clock 4
142	SWMX[58]	I2CSCL		High-Z	In/Out	I2C Serial Clock
		GPIO[55]	-	High-Z	In/Out	GPIO 2 Register, bit 23
		TCD[4]	-		In	Telecommand Data 4

Table 3. I/O switch matrix pin description, defining the order of priority for outputs and input/outputs, with the highest priority for each pin listed first.

Pin no.	Pin name	Pin function	Polarity	Reset value	Dir.	Description
140	SWMX[59]	CB[8]	-	High-Z	In/Out	Reed-Solomon Check Bit 8
		GPIO[56]	-	High-Z	In/Out	GPIO 2 Register, bit 24
137	SWMX[60]	CB[9]	-	High-Z	In/Out	Reed-Solomon Check Bit 9
		GPIO[57]	-	High-Z	In/Out	GPIO 2 Register, bit 25
136	SWMX[61]	CB[10]	-	High-Z	In/Out	Reed-Solomon Check Bit 10
		GPIO[58]	-	High-Z	In/Out	GPIO 2 Register, bit 26
135	SWMX[62]	CB[11]	-	High-Z	In/Out	Reed-Solomon Check Bit 11
		GPIO[59]	-	High-Z	In/Out	GPIO 2 Register, bit 27
132	SWMX[63]	CB[12]	-	High-Z	In/Out	Reed-Solomon Check Bit 12
		GPIO[60]	-	High-Z	In/Out	GPIO 2 Register, bit 28
129	SWMX[64]	CB[13]	-	High-Z	In/Out	Reed-Solomon Check Bit 13
		GPIO[61]	-	High-Z	In/Out	GPIO 2 Register, bit 29
128	SWMX[65]	CB[14]	-	High-Z	In/Out	Reed-Solomon Check Bit 14
		GPIO[62]	-	High-Z	In/Out	GPIO 2 Register, bit 30
127	SWMX[66]	CB[15]	-	High-Z	In/Out	Reed-Solomon Check Bit 15
		GPIO[63]	-	High-Z	In/Out	GPIO 2 Register, bit 31

Table 4. I/O switch matrix pin utilization per interface type

Interface type	Pin function	Direction			Total
		In	Out	In/Out	
SDRAM	SDDQM[3:0], SDCASN, SDRASN, SDWEN, SDCSN[1:0]		9		9
SDRAM Reed-Solomon	CB[15:8]			8	8
GPIO	GPIO[...]	26		38	64
UART	UART_TX[5:0], UART_RX[5:0]	6	6		12
SpaceWire	SPW_RXD[5:2], SPW_RXS[5:2], SPW_TXD[5:2], SPW_TXS[5:2]	8	8		16
Ethernet	RMTXD[1:0], RMTXEN, RMMDIO, RMMDC RMRFCLK, RMRXD[0:1], RMCRSDV, RMINTN	5	4	1	10
CAN	CANTXA, CANRXA, CANTXB, CANRXB	4	4		8
MIL-STD-1553B BC/RT/BM	1553RXA, 1553RXNA, 1553RXENA, 1553TXA, 1553TXNA, 1553TXINHA 1553RXB, 1553RXNB, 1553RXENB, 1553TXB, 1553TXNB, 1553TXINHB 1553CK	5	8		13
I2C	I2CSDA, I2CSCL			2	2
SPI	SPICLK, SPIMOSI, SPIMISO	1	2		3
SLINK	SLI, SLO, SLSYNC, SLCLK	1	3		4
ASCS16	A16DASA, A16DASB, A16MCS, A16HS, A16DCS, A16MAS, A16ETR	2	5		7
CCSDS/ECSS TC	TCACT[4:0], TCD[4:0], TCCLK[4:0], TCRFAV[4:0]	20			20
CCSDS/ECSS TM	TMDO, TMCLKO, TMCLKI	1	2		3

Table 5. I/O switch matrix pins listed per function, including supporting signals outside the I/O switch matrix.

Pin no.	Pin name	Pin function	Polarity	Reset value	Dir.	Description
157	SWMX[52]	SDWEN	Low	High-Z	Out	SDRAM Write Enable
163	SWMX[48]	SDCASN	Low	High-Z	Out	SDRAM Column Address Strobe
162	SWMX[49]	SDRASN	Low	High-Z	Out	SDRAM Row Address Strobe
228	SWMX[12]	SDCSN[0]	Low	High-Z	Out	SDRAM Select 0
227	SWMX[13]	SDCSN[1]	Low	High-Z	Out	SDRAM Select 1
197	SWMX[24]	SDDQM[0]	High	High-Z	Out	SDRAM Data Mask 0, corresponds to DATA[7:0]
196	SWMX[25]	SDDQM[1]	High	High-Z	Out	SDRAM Data Mask 1, corresponds to DATA[15:8]
155	SWMX[53]	SDDQM[2]	High	High-Z	Out	SDRAM Data Mask 2, corresponds to DATA[23:16]
154	SWMX[54]	SDDQM[3]	High	High-Z	Out	SDRAM Data Mask 3, corresponds to DATA[31:24]
140	SWMX[59]	CB[8]	-	High-Z	In/Out	Check Bit 8, Reed-Solomon
137	SWMX[60]	CB[9]	-	High-Z	In/Out	Check Bit 9, Reed-Solomon
136	SWMX[61]	CB[10]	-	High-Z	In/Out	Check Bit 10, Reed-Solomon
135	SWMX[62]	CB[11]	-	High-Z	In/Out	Check Bit 11, Reed-Solomon
132	SWMX[63]	CB[12]	-	High-Z	In/Out	Check Bit 12, Reed-Solomon
129	SWMX[64]	CB[13]	-	High-Z	In/Out	Check Bit 13, Reed-Solomon
128	SWMX[65]	CB[14]	-	High-Z	In/Out	Check Bit 14, Reed-Solomon
127	SWMX[66]	CB[15]	-	High-Z	In/Out	Check Bit 15, Reed-Solomon
	ADDRESS[16:2]	ADDRESS[16:2]	-	Low	Out	Memory address
	DATA[31:0]	DATA[31:0]	-	High-Z	In/Out	Memory data bus
	CB[7:0]	CB[7:0]	-	High-Z	In/Out	Memory checkbits
240	SWMX[4]	MCFG3[8]	-		In	At reset, bit 8 in MCFG3 register in the memory controller is set from this input.
238	SWMX[6]	MCFG1[9]	-		In	At reset, bit 9 in MCFG1 register in the memory controller is set from this input
4	SWMX[0]	UART_TX[0]	-	High	Out	UART Transmit 0
3	SWMX[1]	UART_RX[0]	-		In	UART Receive 0
2	SWMX[2]	UART_TX[1]	-	High	Out	UART Transmit 1
1	SWMX[3]	UART_RX[1]	-		In	UART Receive 1
240	SWMX[4]	UART_TX[2]	-	High-Z	Out	UART Transmit 2
239	SWMX[5]	UART_RX[2]	-		In	UART Receive 2
238	SWMX[6]	UART_TX[3]	-	High-Z	Out	UART Transmit 3
233	SWMX[7]	UART_RX[3]	-		In	UART Receive 3
232	SWMX[8]	UART_TX[4]	-	High-Z	Out	UART Transmit 4
231	SWMX[9]	UART_RX[4]	-		In	UART Receive 4
230	SWMX[10]	UART_TX[5]	-	High-Z	Out	UART Transmit 5
229	SWMX[11]	UART_RX[5]	-		In	UART Receive 5
213	SPW_RXD[0]	SPW_RXD[0]	High		In	SpaceWire Receive Data 0
214	SPW_RXS[0]	SPW_RXS[0]	High		In	SpaceWire Receive Strobe 0
215	SPW_TXD[0]	SPW_TXD[0]	High	Low	Out	SpaceWire Transmit Data 0
216	SPW_TXS[0]	SPW_TXS[0]	High	Low	Out	SpaceWire Transmit Strobe 0
204	SPW_RXD[1]	SPW_RXD[1]	High		In	SpaceWire Receive Data 1
205	SPW_RXS[1]	SPW_RXS[1]	High		In	SpaceWire Receive Strobe 1
206	SPW_TXD[1]	SPW_TXD[1]	High	Low	Out	SpaceWire Transmit Data 1
209	SPW_TXS[1]	SPW_TXS[1]	High	Low	Out	SpaceWire Transmit Strobe 1
217	SWMX[19]	SPW_RXD[2]	High		In	SpaceWire Receive Data 2

Table 5. I/O switch matrix pins listed per function, including supporting signals outside the I/O switch matrix.

Pin no.	Pin name	Pin function	Polarity	Reset value	Dir.	Description
218	SWMX[18]	SPW_RXS[2]	High		In	SpaceWire Receive Strobe 2
219	SWMX[17]	SPW_TXD[2]	High	High-Z	Out	SpaceWire Transmit Data 2
220	SWMX[16]	SPW_TXS[2]	High	High-Z	Out	SpaceWire Transmit Strobe 2
200	SWMX[23]	SPW_RXD[3]	High		In	SpaceWire Receive Data 3
201	SWMX[22]	SPW_RXS[3]	High		In	SpaceWire Receive Strobe 3
202	SWMX[21]	SPW_TXD[3]	High	High-Z	Out	SpaceWire Transmit Data 3
203	SWMX[20]	SPW_TXS[3]	High	High-Z	Out	SpaceWire Transmit Strobe 3
225	SWMX[15]	SPW_RXD[4]	High		In	SpaceWire Receive Data 4
226	SWMX[14]	SPW_RXS[4]	High		In	SpaceWire Receive Strobe 4
227	SWMX[13]	SPW_TXD[4]	High	High-Z	Out	SpaceWire Transmit Data 4
228	SWMX[12]	SPW_TXS[4]	High	High-Z	Out	SpaceWire Transmit Strobe 4
192	SWMX[27]	SPW_RXD[5]	High		In	SpaceWire Receive Data 5
193	SWMX[26]	SPW_RXS[5]	High		In	SpaceWire Receive Strobe 5
197	SWMX[24]	SPW_TXD[5]	High	High-Z	Out	SpaceWire Transmit Data 5
196	SWMX[25]	SPW_TXS[5]	High	High-Z	Out	SpaceWire Transmit Strobe 5
178	SWMX[37]	SpaceWire clock divisor registers values at reset, all other bits are zero.	-		In	At reset, bits 8 & 0 are set from this input
175	SWMX[40]		-		In	At reset, bits 9 & 1 are set from this input
172	SWMX[43]		-		In	At reset, bits 10 & 2 are set from this input
166	SWMX[45]		-		In	At reset, bits 11 & 3 are set from this input
185	SWMX[32]	RMTXEN	High	High-Z	Out	Ethernet Transmit Enable
191	SWMX[28]	RMTXD[0]	-	High-Z	Out	Ethernet Transmit Data 0
190	SWMX[29]	RMTXD[1]	-	High-Z	Out	Ethernet Transmit Data 1
189	SWMX[30]	RMRXD[0]	-		In	Ethernet Receive Data 0
188	SWMX[31]	RMRXD[1]	-		In	Ethernet Receive Data 1
183	SWMX[34]	RMCRSDV	High		In	Ethernet Carrier Sense / Data Valid
182	SWMX[35]	RMINTN	Low		In	Ethernet Management Interrupt
179	SWMX[36]	RMMDIO	-	High-Z	In/Out	Ethernet Media Interface Data
178	SWMX[37]	RMMDC	-	High-Z	Out	Ethernet Media Interface Clock
177	SWMX[38]	RMRFCLK	-		In	Ethernet Reference Clock
220	SWMX[16]	CANTXA	-	High-Z	Out	CAN Transmit A
218	SWMX[18]	CANRXA	-		In	CAN Receive A
219	SWMX[17]	CANTXB	-	High-Z	Out	CAN Transmit B
217	SWMX[19]	CANRXB	-		In	CAN Receive B
191	SWMX[28]	-		High-Z	Out	Proprietary, enabled by CAN
190	SWMX[29]	-		High-Z	Out	Proprietary, enabled by CAN
185	SWMX[32]	-		High-Z	Out	Proprietary, enabled by CAN
184	SWMX[33]	-		High-Z	Out	Proprietary, enabled by CAN
172	SWMX[43]	-		High-Z	Out	Proprietary, enabled by CAN
177	SWMX[38]	1553CK	-		In	MIL-STD-1553B Clock
184	SWMX[33]	1553TXINHA	High	High-Z	Out	MIL-STD-1553B Transmit Inhibit A
190	SWMX[29]	1553TXA	High	High-Z	Out	MIL-STD-1553B Transmit Positive A
185	SWMX[32]	1553TXNA	Low	High-Z	Out	MIL-STD-1553B Transmit Negative A
191	SWMX[28]	1553RXENA	High	High-Z	Out	MIL-STD-1553B Receive Enable A
189	SWMX[30]	1553RXA	High		In	MIL-STD-1553B Receive Positive A
188	SWMX[31]	1553RXNA	Low		In	MIL-STD-1553B Receive Negative A
174	SWMX[41]	1553TXINHB	High	High-Z	Out	MIL-STD-1553B Transmit Inhibit B
178	SWMX[37]	1553TXB	High	High-Z	Out	MIL-STD-1553B Transmit Positive B

Table 5. I/O switch matrix pins listed per function, including supporting signals outside the I/O switch matrix.

Pin no.	Pin name	Pin function	Polarity	Reset value	Dir.	Description
175	SWMX[40]	1553TXNB	Low	High-Z	Out	MIL-STD-1553B Transmit Negative B
179	SWMX[36]	1553RXENB	High	High-Z	Out	MIL-STD-1553B Receive Enable B
183	SWMX[34]	1553RXB	High		In	MIL-STD-1553B Receive Positive B
182	SWMX[35]	1553RXNB	Low		In	MIL-STD-1553B Receive Negative B
143	SWMX[57]	I2CSDA		High-Z	In/Out	I2C Serial Data
142	SWMX[58]	I2CSCL		High-Z	In/Out	I2C Serial Clock
169	SWMX[44]	SPICLK		High-Z	Out	SPI Clock
166	SWMX[45]	SPIMOSI	-	High-Z	Out	SPI Master Out Slave In
160	SWMX[51]	SPIMISO			In	SPI Master In Slave Out
203	SWMX[20]	SLSYNC	High	High-Z	Out	SLINK SYNC
166	SWMX[45]	SLCLK	High	High-Z	Out	SLINK Clock
160	SWMX[51]	SLI	-		In	SLINK Data In
169	SWMX[44]	SLO	-	High-Z	Out	SLINK Data Out
226	SWMX[14]	A16DASA	-		In	ASCS DAS A - Slave data in
225	SWMX[15]	A16DASB	-		In	ASCS DAS B - Slave data in
202	SWMX[21]	A16ETR	High	High-Z	Out	ASCS ETR - Synchronization signal
175	SWMX[40]	A16DCS	-	High-Z	Out	ASCS DCS - Slave data out
174	SWMX[41]	A16MAS	High	High-Z	Out	ASCS MAS - TM start/stop signal
179	SWMX[36]	A16MCS	High	High-Z	Out	ASCS MCS - TC start/stop signal
178	SWMX[37]	A16HS	High	High-Z	Out	ASCS HS - TM/TC serial clock
229	SWMX[11]	TCACT[0]	High		In	Telecommand Active 0
226	SWMX[14]	TCCLK[0]	Rising		In	Telecommand Clock 0
225	SWMX[15]	TCD[0]	-		In	Telecommand Data 0
193	SWMX[26]	TCRFAVL[0]	High		In	Telecommand RF Available 0
188	SWMX[31]	TCACT[1]	High		In	Telecommand Active 1
192	SWMX[27]	TCCLK[1]	Rising		In	Telecommand Clock 1
189	SWMX[30]	TCD[1]	-		In	Telecommand Data 1
183	SWMX[34]	TCRFAVL[1]	High		In	Telecommand RF Available 1
176	SWMX[39]	TCACT[2]	High		In	Telecommand Active 2
182	SWMX[35]	TCCLK[2]	Rising		In	Telecommand Clock 2
177	SWMX[38]	TCD[2]	-		In	Telecommand Data 2
173	SWMX[42]	TCRFAVL[2]	High		In	Telecommand RF Available 2
161	SWMX[50]	TCACT[3]	High		In	Telecommand Active 3
165	SWMX[46]	TCCLK[3]	Rising		In	Telecommand Clock 3
164	SWMX[47]	TCD[3]	-		In	Telecommand Data 3
160	SWMX[51]	TCRFAVL[3]	High		In	Telecommand RF Available 3
153	SWMX[55]	TCACT[4]	High		In	Telecommand Active 4
143	SWMX[57]	TCCLK[4]	Rising		In	Telecommand Clock 4
142	SWMX[58]	TCD[4]	-		In	Telecommand Data 4
144	SWMX[56]	TCRFAVL[4]	High		In	Telecommand RF Available 4
231	SWMX[9]	TMCLKI	Rising		In	Telemetry Clock Input
230	SWMX[10]	TMCLKO	-	High-Z	Out	Telemetry Clock Output
232	SWMX[8]	TMDO	-	High-Z	Out	Telemetry Data Out

Table 6. Conflicting interfaces in the I/O switch matrix are marked with an X, with duplicates shown in bold typeface.

	SDRAM (with RS)	UART 0	UART 1	UART 2	UART 3	UART 4	UART 5	SpaceWire 0	SpaceWire 1	SpaceWire 2	SpaceWire 3	SpaceWire 4	SpaceWire 5	Ethernet	CAN	MIL-STD-1553B	I2C	SPI	SLINK	ASCS	CCSDS TC 0	CCSDS TC 1	CCSDS TC 2	CCSDS TC 3	CCSDS TC 4	CCSDS TM
SDRAM (with RS)	-											**X**	**X**													
UART 0		-																								
UART 1			-																							
UART 2				-																						
UART 3					-																					
UART 4						-																				**X**
UART 5							-														**X**					**X**
SpaceWire 0								-																		
SpaceWire 1									-																	
SpaceWire 2										-					**X**					**X**						
SpaceWire 3											-								**X**							
SpaceWire 4	X											-								**X**	**X**					
SpaceWire 5	X												-								**X**	**X**				
Ethernet														-	**X**	**X**						***X***	***X***			
CAN										X				X	-											
MIL-STD-1553B														X		-				**X**		**X**	**X**			
I2C																	-								**X**	
SPI																		-	**X**					**X**		
SLINK											X							X	-					**X**		
ASCS										X		X				X				-	***X***					
CCSDS TC 0							X					X	X							*X*	-					
CCSDS TC 1													X	*X*		X						-				
CCSDS TC 2														*X*		X							-			
CCSDS TC 3																		X	X					-		
CCSDS TC 4																	X								-	
CCSDS TM						X	X																			-

2 Electrical characteristics

2.1 Absolute maximum ratings

These values specify the stress that might apply to the device without causing it permanent damage.

Table 7. Absolute maximum ratings [1)]

Symbol	Parameter	Rating		Units
		Min.	Max.	
V_{DDIO}	DC Supply Voltage for I/O	-0.3	4.2	V
V_{DD}	DC Supply Voltage for Core	-0.3	2.4	V
V_{IN}	Input Voltage	-0.3	V_{DDIO} + 0.3	V
T_{stor}	Storage Temperature	-65	+150	˚C
T_{case}	Operating Case Temperature	-55	+125	˚C
T_{solder}	Lead Temperature (Soldering 10 sec.)		+250	˚C
T_j	Junction Temperature		+150	˚C
Θ_{JC} (ceramic)	Thermal Resistance, Junction to Case		4	˚C/W
P_D	Power Dissipation		6.25	W

Note 1: Extended operation at the maximum levels may degrade the performance and affect the reliability of the device.

2.2 Recommended operating conditions

Table 8. Recommended operating conditions

Symbol	Parameter	Rating			Units
		Min.	Typ.	Max.	
V_{DDIO}	DC Supply Voltage for I/O	3.0	3.3	3.6	V
V_{DD}	DC Supply Voltage for Core	1.65	1.8	1.95	V
V_{IN}	Input Voltage	0		V_{DDIO}	V
T_{case}	Operating Case Temperature	-55		+125	˚C
SL_{IN}	Slew rate of all inputs [1)]	0.4			V/ns

Note 1: Applies only to the range 0.8 V and 2.0 V.

2.3 DC electrical performance characteristics

Table 9. DC characteristics (V_{DD} = 1.8 V +/- 0.15 V, V_{DDIO} = 3.3 V +/- 0.3 V, T_{case} = -55˚C to +125˚C)

Symbol	Parameter	Condition	Rating			Units
			Min.	Typ.	Max.	
V_{OH}	Output High Voltage [1]	I_{OH} = -4 mA [2] I_{OH} = -6 mA [3]	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 4 mA [2] I_{OL} = 6 mA [3]			0.5	V
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_{ILEAK}	Input Leakage Current		-10		10	uA
I_{OLEAK}	Output Leakage Current	outputs at tri-state	-10		10	uA
I_{OS}	Short-circuit Output Current	V_O = V_{DDIO}, V_{DDIO} = 3.6 V V_O = 0 V, V_{DDIO} = 3.6 V	-120 [5]		120 [5]	mA
I_{DDS}	Core Static Current	F_{CLK} = 0 MHz		1	10	mA
I_{DD}	Core Supply Current	F_{CLK} = 100 MHz		0.9	2.0 [5]	A
I_{DDIOS}	I/O Static Current [4]	F_{CLK} = 0 MHz V_{DDIO} = 3.6 V		0.2	2	mA
I_{DDIO}	I/O Supply Current [6]					mA
$C_{I/O}$	I/O Pad Capacitance [5]				15	pF

Note 1: Except open-drain outputs ERRORN, WDOGN, I2CSCL and I2CSDA.

Note 2: All outputs defined with a maximum load of 50 pF.

Note 3: All outputs defined with a maximum load of 100 pF.

Note 4: All inputs at 0 V or V_{DDIO}. No resistive load.

Note 5: Supplied as a design limit. Parameter not measured during production test.

Note 6: The dynamic power consumption of the I/O supply can be calculated as a function of the average frequency and the capacitive load of each output *i*: sum of $[F_{I/O} * C_{LOAD}]_{(i)} * (V_{DDIO})^2$

Table 10. Detailed core power consumption (V_{DD} = 1.8 V +/- 0.15 V, V_{DDIO} = 3.3 V +/- 0.3 V, T_{case} = -55˚C to +125˚C)

Test condition	**Rating**		**Units**
	Typ.	**Max.** [1)]	
Static, no clocks or toggling signals	30	50	mW
Standby, all cores clock gated	4	6	mW/MHz
1 processor core active at 50%, remaining IP cores clock gated	7	10	mW/MHz
1 processor core active at 100%, remaining IP cores clock gated	10	15	mW/MHz
2 processor cores active at 100%, remaining IP cores clock gated	15	24	mW/MHz
1 SpaceWire link active @ 100 Mbit/s	1	1.5	mW/MHz
2 CAN interfaces active 100% @ 1 Mbit/s	1	1.5	mW/MHz
Telemetry encoder active @ 10 Mbit/s	0.5	1	mW/MHz

Note 1: Supplied as a design limit. Parameter not measured during production test.

2.4 AC electrical performance characteristics

All measured AC parameters have been tested with a 50 pF - 70 pF capacitive load on the outputs. Transition time measurements have been tested at a voltage level of 1.4 V. Equivalent load chart is provided in the product specification [PS.]

2.4.1 Clock

The timing waveforms and timing parameters are shown in figure 3 and are defined in table 11.

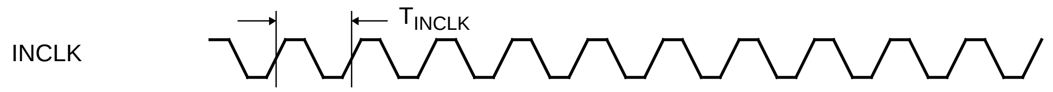

Figure 3. Timing waveforms

Table 11. Timing parameters (V_{DD} = 1.8 V +/- 0.15 V, V_{DDIO} = 3.3 V +/- 0.3 V, T_{case} = -55˚C to +125˚C)

Name	Parameter	Reference	Min	Max	Unit
T_{INCLK}	input clock period without DLL	INCLK	10	-	ns
F_{INCLK}	input clock frequency without DLL 2)	INCLK	-	100	MHz
T_{INCLK_HIGH}	input clock high phase without DLL 5)	INCLK	4.5		ns
T_{INCLK_LOW}	input clock low phase without DLL 5)	INCLK	4.5		ns
T_{INCLK}	input clock period with DLL 1)	INCLK	20	22 3)	ns
F_{INCLK}	input clock frequency with DLL 1) 2)	INCLK	46 3)	50	MHz
DC_{INCLK}	input frequency duty cycle with DLL	INCLK	35	65	%
T_{INCLK_HIGH}	input clock high phase with DLL 5)	INCLK	7		ns
T_{INCLK_LOW}	input clock low phase with DLL 5)	INCLK	7		ns
T_{CLK}	internal system clock period 4) 5) 6)	-	10	-	ns
F_{CLK}	internal system clock frequency 2) 4) 5) 6)	-	-	100	MHz

Note 1: For the system clock, the DLL provides a times 2 multiplication of the input frequency.

Note 2: $T_{INCLK} = 1/F_{INCLK}$, $T_{CLK} = 1/F_{CLK}$

Note 3: Parameter not measured during production test.

Note 4: Applies to the system clock only (i.e. processor and AMBA clock) only. SpaceWire clocks are discussed in section 2.4.9.

Note 5: The maximum internal system clock frequency is specified by the parameters T_{CLK} and F_{CLK}.

The parameters T_{INCLK} and F_{INCLK} specify the what the clock input pin and the DLL can support, and not what the internal logic can support.

Note 6: The internal system clock frequency is limited by the timing of the memory interface towards external synchronous memory components.

2.4.2 Reset and initialization

The timing waveforms and timing parameters are shown in figure 4 and are defined in table 12.

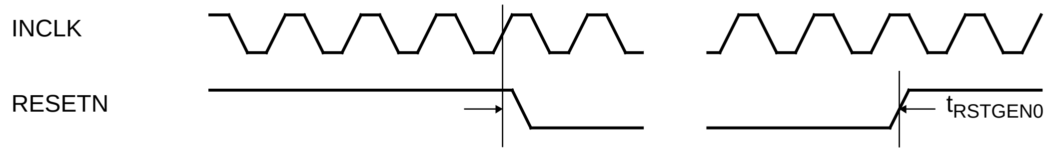

Figure 4. Timing waveforms

Table 12. Timing parameters (V_{DD} = 1.8 V +/- 0.15 V, V_{DDIO} = 3.3 V +/- 0.3 V, T_{case} = -55˚C to +125˚C)

Name	Parameter	Reference edge	Min	Max	Unit
$t_{RSTGEN0}$	asserted period	-	10	-	T_{INCLK} periods

Note 1: The RESETN input is re-synchronized internally.

Note 2: V_{DD} must reach at least minimum operating voltage for $t_{RESTGEN0}$ before RESETN is de-asserted.

Note 3: If DLL is used, the internal reset is released 2048 T_{INCLK} periods after RESETN is de-asserted

Note 4: After power-up all flip-flops, on-chip memory and DLL are in an unknown state before reset.

2.4.3 LEON3 - High-performance SPARC V8 32-bit Processor

The timing waveforms and timing parameters are shown in figure 5 and are defined in table 13.

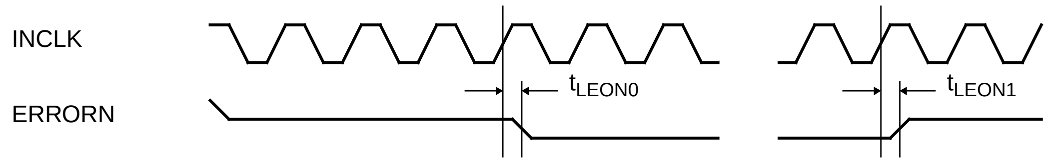

Figure 5. Timing waveforms

Table 13. Timing parameters (V_{DD} = 1.8 V +/- 0.15 V, V_{DDIO} = 3.3 V +/- 0.3 V, T_{case} = -55˚C to +125˚C)

Name	Parameter	Reference edge	Min	Max	Unit
t_{LEON0}	clock to output delay	rising INCLK edge	2 [1)]	23 [2)]	ns
t_{LEON1}	clock to output tri-state	rising INCLK edge		50 [1)]	ns

Note 1: Parameter not measured during production test.

Note 2: Parameter measured during production test without DLL enabled.

Note 3: For correct operation, the signal should be pulled-up externally with 1- 10 kOhm. GR712RC does not include any internal pull-up resistors.

2.4.4 Fault tolerant memory controller

The timing waveforms and timing parameters are shown in figure 6 and are defined in table 14.

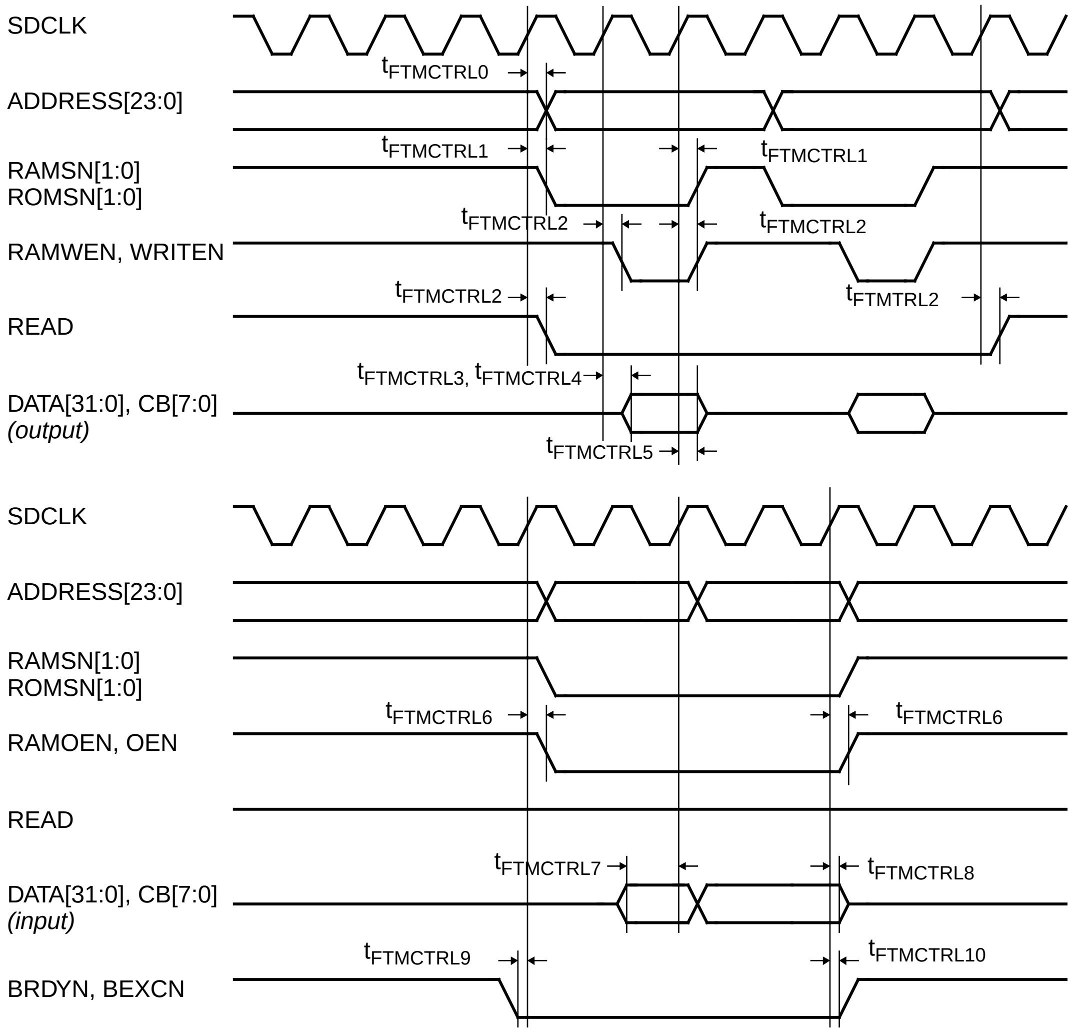

Figure 6. Timing waveforms - SRAM (0 wait state) access, PROM (0 wait state) access

The timing waveforms and timing parameters are shown in figure 7 and are defined in table 14.

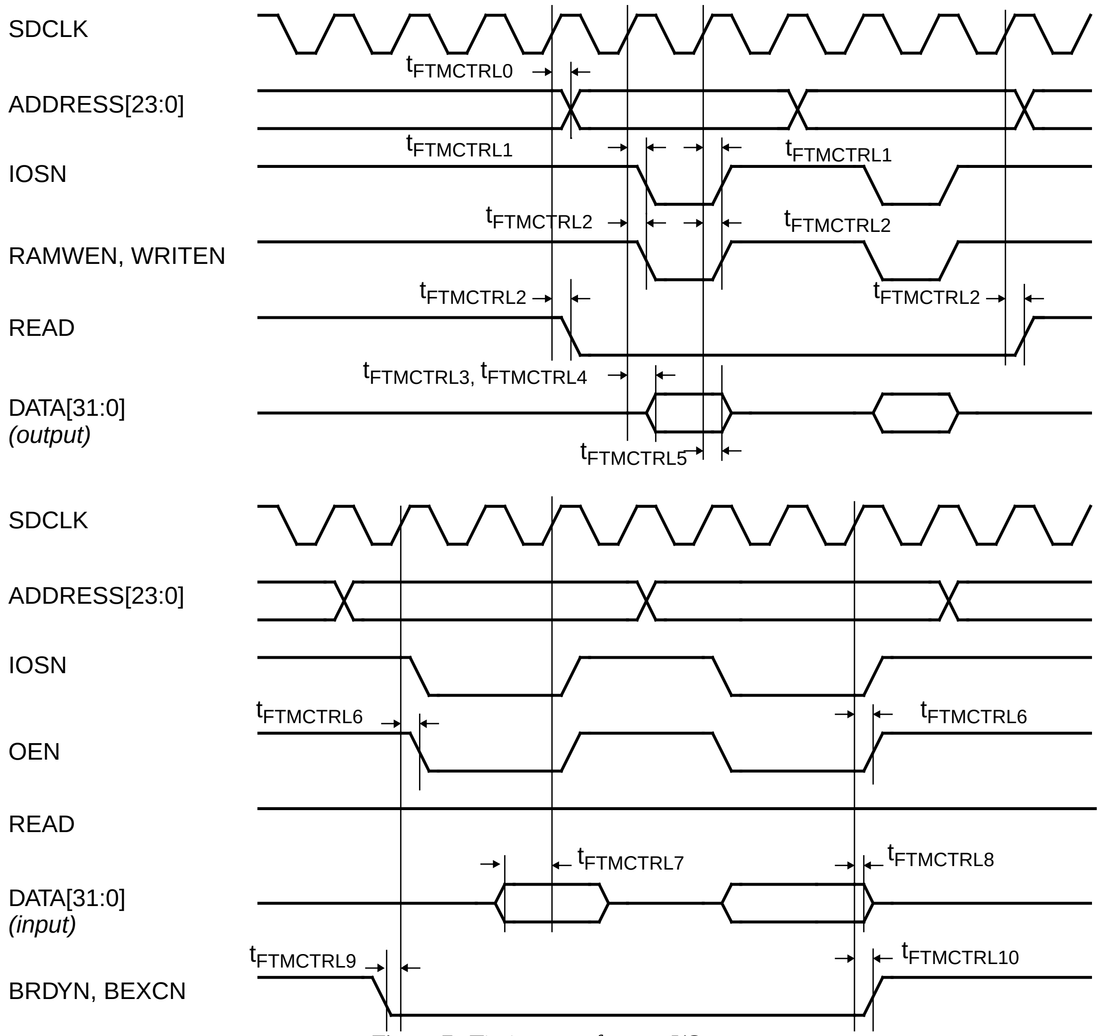

Figure 7. Timing waveforms - I/O accesses

Table 14. Timing parameters (V_{DD} = 1.8 V +/- 0.15 V, V_{DDIO} = 3.3 V +/- 0.3 V, T_{case} = -55˚C to +125˚C)

Name	Parameter	Reference edge [2)]	Min	Max	Unit
$t_{FTMCTRL0}$	address clock to output delay [3)]	rising SDCLK edge	0 [1)]	7.5	ns
$t_{FTMCTRL1}$	clock to RAMSN[1:0] and ROMSN[1:0]output delay [3)]	rising SDCLK edge	0 [1)]	7.5	ns
$t_{FTMCTRL1}$	clock to IOSN output delay [3)]	rising SDCLK edge	0 [1)]	8.5	ns
$t_{FTMCTRL2}$	clock to output delay	rising SDCLK edge	0 [1)]	8.5	ns
$t_{FTMCTRL3}$	clock to data output delay	rising SDCLK edge	0 [1)]	6.5	ns
$t_{FTMCTRL4}$	clock to data non-tri-state delay	rising SDCLK edge	0 [1)]	6.5	ns
$t_{FTMCTRL5}$	clock to data tri-state delay [4)]	rising SDCLK edge	0 [1)]	6.5 [1)]	ns
$t_{FTMCTRL6}$	clock to output delay	rising SDCLK edge	0 [1)]	8.5	ns
$t_{FTMCTRL7}$	data input to clock setup	rising SDCLK edge	6.9	-	ns
$t_{FTMCTRL8}$	data input from clock hold	rising SDCLK edge	-0.5 [1)]	-	ns
$t_{FTMCTRL9}$	input to clock setup	rising SDCLK edge	6.9	-	ns
$t_{FTMCTRL10}$	input from clock hold	rising SDCLK edge	-0.5 [1)]	-	ns

Note 1: Parameter not measured during production test.

Note 2: The specified timing is valid for the default programmable internal clock delay of value 0.

Note 3: The ADDRESS[23:0] and RAMSN[1:0] signals change in the same clock cycle, which might not be compatible with all SRAM types. Check your SRAM documentation for compatibility.

Note 4: GR712RC does not provide internal pull-up resistors on the DATA[31:0] and CB[15:0] buses. In the case of prolonged periods of idle bus activity in a board design, i.e. high impedance state, it is advised to add external pull-up resistors.

The timing waveforms and timing parameters are shown in figure 8 and are defined in table 15.

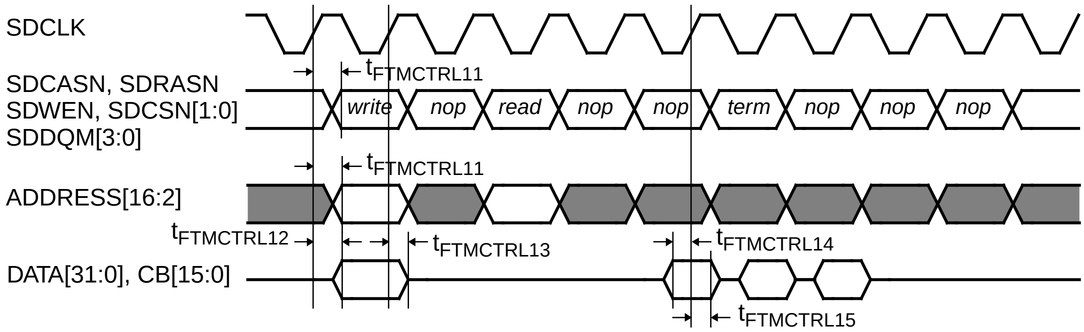

Figure 8. Timing waveforms - SDRAM accesses

Table 15. Timing parameters (V_{DD} = 1.8 V +/- 0.15 V, V_{DDIO} = 3.3 V +/- 0.3 V, T_{case} = -55˚C to +125˚C)

Name	**Parameter**	**Reference edge** 2)	**Min**	**Max**	**Unit**
$t_{FTMCTRL11}$	clock to output delay	rising SDCLK edge	1 1)	6	ns
$t_{FTMCTRL12}$	clock to data output delay	rising SDCLK edge	1 1)	6.5	ns
$t_{FTMCTRL13}$	data clock to data tri-state delay	rising SDCLK edge	1 1)	6.5 1)	ns
$t_{FTMCTRL14}$	data input to clock setup	rising SDCLK edge	6.9	-	ns
$t_{FTMCTRL15}$	data input from clock hold	rising SDCLK edge	-0.5 1)	-	ns

Note 1: Parameter not measured during production test.

Note 2: The specified timing is valid for the default programmable internal clock delay of value 0.

Note 3: The maximum operating frequency of the GR712RC may be limited due to the timing performance of external SDRAM devices.

The timing waveforms and timing parameters are shown in figure 9 and are defined in table 16.

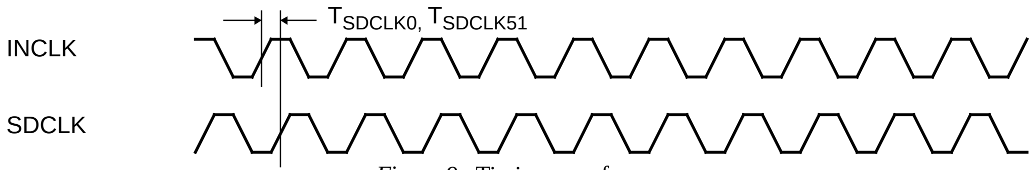

Figure 9. Timing waveforms

Table 16. Timing parameters (V_{DD} = 1.65 V, V_{DDIO} = 3.0 V, T_{case} = +125˚C) 1)

Name	Parameter	Reference	Min	Max	Unit
T_{SDCLK0}	clock to output delay, delay value 0	rising INCLK edge	7	10	ns
$T_{SDCLK51}$	clock to output delay, delay value 51	rising INCLK edge	16	25	ns

Note 1: Production test performed at fixed voltage and temperature.

2.4.5 JTAG Debug Interface

The timing waveforms and timing parameters are shown in figure 10 and are defined in table 17.

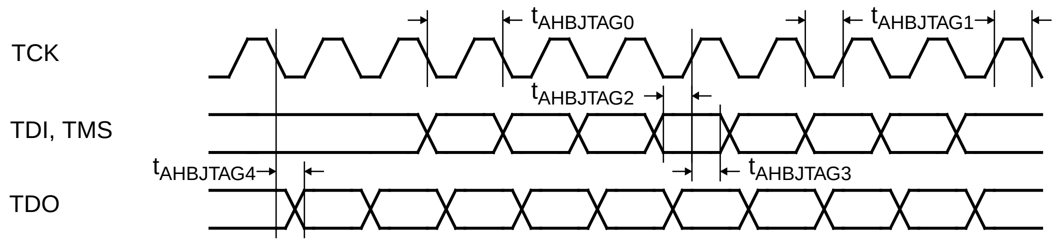

Figure 10. Timing waveforms

Table 17. Timing parameters (V_{DD} = 1.8 V +/- 0.15 V, V_{DDIO} = 3.3 V +/- 0.3 V, T_{case} = -55˚C to +125˚C)

Name	**Parameter**	**Reference edge**	**Min**	**Max**	**Unit**
$t_{AHBJTAG0}$	clock period	-	100	-	ns
$t_{AHBJTAG1}$	clock low/high period	-	40	-	ns
$t_{AHBJTAG2}$	data input to clock setup	rising TCK edge	10 [1)]	-	ns
$t_{AHBJTAG3}$	data input from clock hold	rising TCK edge	10 [1)]	-	ns
$t_{AHBJTAG4}$	clock to data output delay	falling TCK edge	0 [1)]	21	ns

Note 1: Parameter not measured during production test.

Note 2: For correct operation, all JTAG signals should be pulled-up externally with 1 - 10 kOhm. This is in line with the TAP specification where TMS and TDI implementation should be such that if an external signal fails (e.g. open circuit) then the behavior of TMS and TDI should be equivalent to a logical 1 input. GR712RC does not include any internal pull-up resistors.

2.4.6 General Purpose Timer Unit

The timing waveforms and timing parameters are shown in figure 11 and are defined in table 18.

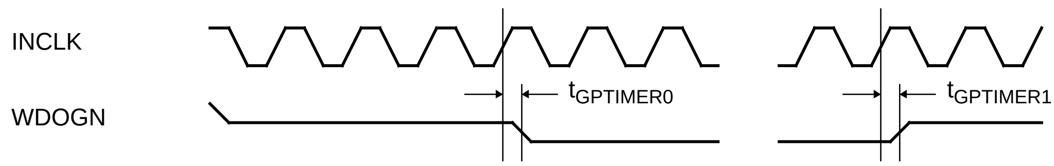

Figure 11. Timing waveforms

Table 18. Timing parameters (V_{DD} = 1.8 V +/- 0.15 V, V_{DDIO} = 3.3 V +/- 0.3 V, T_{case} = -55˚C to +125˚C)

Name	**Parameter**	**Reference edge**	**Min**	**Max**	**Unit**
$t_{GPTIMER0}$	clock to output delay	rising INCLK edge	2 [1)]	23 [2)]	ns
$t_{GPTIMER1}$	clock to output tri-state	rising INCLK edge		50 [1)]	ns

Note 1: Parameter not measured during production test.

Note 2: Parameter measured during production test without DLL enabled.

Note 3: For correct operation, the signal should be pulled-up externally with 1 - 10 kOhm. GR712RC does not include any internal pull-up resistors.

Note 4: WDOGN output is undefined during internal reset when DLL is used to generate the internal system clock frequency. See section 2.4.2 for detailed timing information on the reset behavior.

2.4.7 General Purpose Input Output Port

The timing waveforms and timing parameters are shown in figure 12 and are defined in table 19.

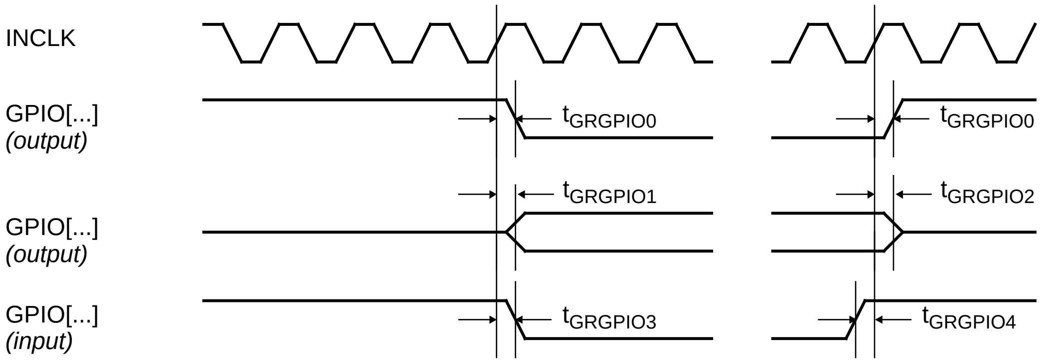

Figure 12. Timing waveforms

Table 19. Timing parameters (V_{DD} = 1.8 V +/- 0.15 V, V_{DDIO} = 3.3 V +/- 0.3 V, T_{case} = -55˚C to +125˚C)

Name	**Parameter**	**Reference edge**	**Min**	**Max**	**Unit**
$t_{GRGPIO0}$	clock to output delay	rising INCLK edge	2 [1)]	21 [2)]	ns
$t_{GRGPIO1}$	clock to non-tri-state delay	rising INCLK edge	2 [1)]	21 [1)]	ns
$t_{GRGPIO2}$	clock to tri-state delay	rising INCLK edge		50 [1)]	ns
$t_{GRGPIO3}$	input to clock hold	rising INCLK edge	-	-	ns [3)]
$t_{GRGPIO4}$	input to clock setup	rising INCLK edge	-	-	ns [3)]

Note 1: Parameter not measured during production test.

Note 2: Parameter measured during production test without DLL enabled.

Note 3: The GPIO[...] inputs are re-synchronized to the internal system clock with a T_{CLK} period.

2.4.8 UART Serial Interface

The timing waveforms and timing parameters are shown in figure 13 and are defined in table 20.

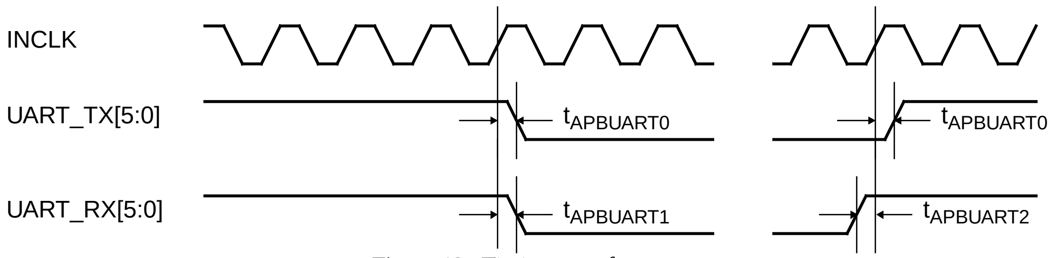

Figure 13. Timing waveforms

Table 20. Timing parameters (V_{DD} = 1.8 V +/- 0.15 V, V_{DDIO} = 3.3 V +/- 0.3 V, T_{case} = -55˚C to +125˚C)

Name	**Parameter**	**Reference edge**	**Min**	**Max**	**Unit**
$t_{APBUART0}$	clock to output delay	rising INCLK edge	2 [1)]	21 [2)]	ns
$t_{APBUART1}$	input to clock hold	rising INCLK edge	-	-	ns [3)]
$t_{APBUART2}$	input to clock setup	rising INCLK edge	-	-	ns [3)]

Note 1: Parameter not measured during production test.

Note 2: Parameter measured during production test without DLL enabled.

Note 3: The UART_RX[5:0] inputs are re-synchronized to the internal system clock with a T_{CLK} period.

2.4.9 SpaceWire Interface

The timing waveforms and timing parameters are shown in figure 14 and are defined in table 21.

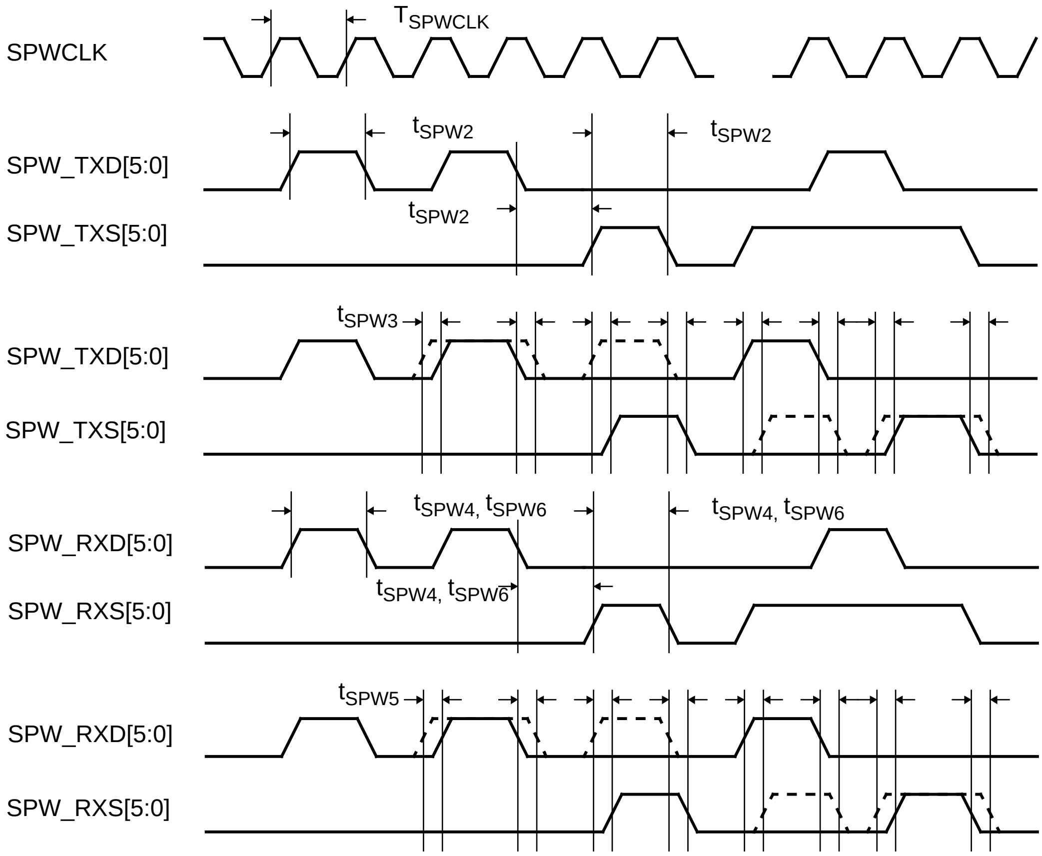

Figure 14. Timing waveforms

Table 21. Timing parameters transmitter (V_{DD} = 1.8 V +/- 0.15 V, V_{DDIO} = 3.3 V +/- 0.3 V, T_{case} = -55˚C to +125˚C)

Name	**Parameter**	**Reference edge**	**Min**	**Max**	**Unit**
T_{SPWCLK}	input clock period without DLL 5)	SPWCLK	10 4)	-	ns
F_{SPWCLK}	input clock frequency without DLL 2)	SPWCLK	-	100 4)	MHz
DC_{SPWCLK}	input frequency duty cycle without DLL 5)	SPWCLK	45	55	%
T_{SPWCLK}	input clock period with DLL x2 1) 6)	SPWCLK	20	22 4)	ns
F_{SPWCLK}	input clock frequency with DLL x2 1) 2)	SPWCLK	45 4)	50	MHz
T_{SPWCLK}	input clock period with DLL x4 1) 6)	SPWCLK	20	22 4)	ns
F_{SPWCLK}	input clock frequency with DLL x4 1) 2)	SPWCLK	45 4)	50	MHz
DC_{SPWCLK}	input frequency duty cycle with DLL	SPWCLK	35 4)	65 4)	%
T_{SPW}	internal transmitter clock period 6)	-	5	500 4)	ns
F_{SPW}	internal transmitter clock frequency 2) 6)	-	2 4)	200	MHz
t_{SPW2}	output data bit period	-	5 4)	500 4)	ns
t_{SPW3}	data & strobe output skew & jitter	-	-	500 4)	ps
t_{SPW4}	input data bit period	-	5 4)	500 4)	ns
t_{SPW5}	data & strobe input skew, jitter & hold	-	-	800 4)	ps
t_{SPW6}	data & strobe edge separation 5)	-	2500 4)	-	ps

Note 1: For the internal SpaceWire clock, the DLL provides a times 2 or 4 multiplication of the input frequency.

Note 2: $T_{SPWCLK} = 1/F_{SPWCLK}$, $T_{SPW} = 1/F_{SPW}$

Note 3: N/A

Note 4: Parameter not measured during production test.

Note 5: Minimum internal edge separation equals half the internal transmitter clock period. Minimum t_{SPW6} is specified at minimum T_{SPW} with 50% duty cycle. External edge separation should not be less than the sum of $t_{SPW5} + t_{SPW6}$.

Note 6: The maximum SpaceWire clock frequency is specified by the parameters T_{SPW} and F_{SPW}.

The parameters T_{SPWCLK} and F_{SPWCLK} specify the what the clock input pin and the DLL can support, and not what the internal logic can support.

Note 7: The parameters t_{SPWn} are only valid between signals belonging to one SpaceWire link.

2.4.10 Ethernet Media Access Controller (MAC)

The timing waveforms and timing parameters are shown in figure 15 and are defined in table 22.

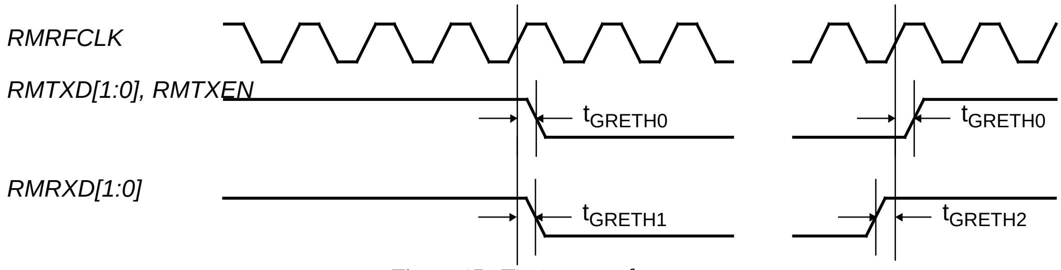

Figure 15. Timing waveforms

Table 22. Timing parameters (V_{DD} = 1.8 V +/- 0.15 V, V_{DDIO} = 3.3 V +/- 0.3 V, T_{case} = -55˚C to +125˚C)

Name	Parameter	Reference edge	Min	Max	Unit
$t_{GRETHREF}$	Ethernet reference clock period	any RMRFCLK edge	20 4)	-	ns
t_{GRETH0}	transmitter clock to output delay	rising RMRFCLK edge	2 1)	15	ns
t_{GRETH1}	input to receiver clock hold	rising RMRFCLK edge	2	-	ns
t_{GRETH2}	input to receiver clock setup	rising RMRFCLK edge	4	-	ns

Note 1: Parameter not measured during production test.

Note 2: The RMINTN, RMMDIO and RMCRSDV inputs are re-synchronized internally.

Note 3: The RMMDIO and RMMDC outputs are low speed signals without any timing relationship with the RMRFCLK clock.

Note 4: According to Ethernet standard the reference clock RMRFCLK frequency must be 50 MHz +/- 50 ppm.

2.4.11 CAN Interface

The timing waveforms and timing parameters are shown in figure 16 and are defined in table 23.

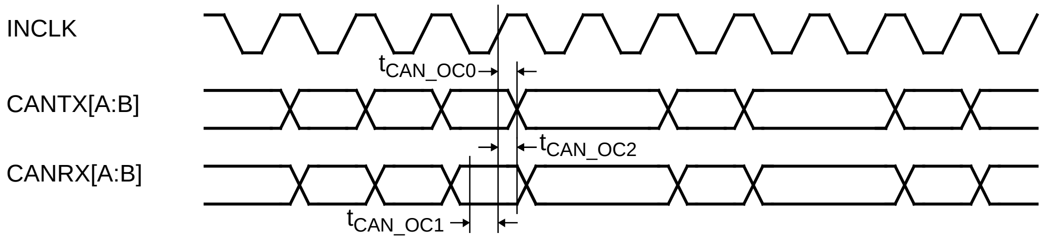

Figure 16. Timing waveforms

Table 23. Timing parameters (V_{DD} = 1.8 V +/- 0.15 V, V_{DDIO} = 3.3 V +/- 0.3 V, T_{case} = -55˚C to +125˚C)

Name	**Parameter**	**Reference edge**	**Min**	**Max**	**Unit**
t_{CAN_OC0}	clock to data output delay	rising INCLK edge	2 1)	21 1)	ns
t_{CAN_OC1}	data input to clock setup	rising INCLK edge	-	-	ns 3)
t_{CAN_OC2}	data input from clock hold	rising INCLK edge	-	-	ns 3)

Note 1: Parameter not measured during production test.

Note 2: Parameter measured during production test without DLL enabled.

Note 3: The CANRX[A:B] input is re-synchronized to the internal system clock with a T_{CLK} period.

2.4.12 Obsolete

Proprietary function not supported.

2.4.13 MIL-STD-1553B BC/RT/BM

The timing waveforms and timing parameters are shown in figure 17 and are defined in table 24.

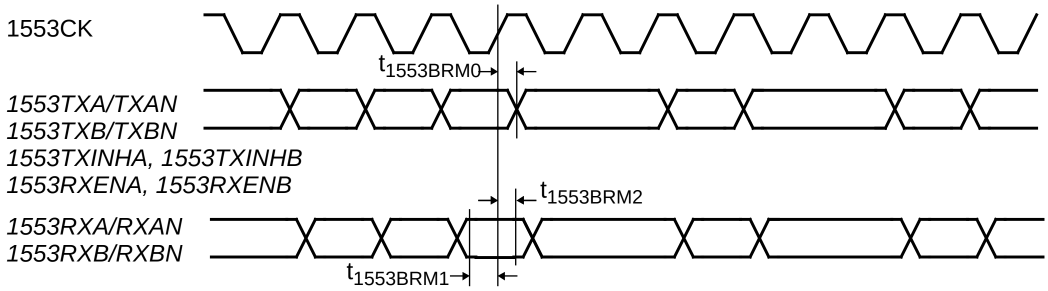

Figure 17. Timing waveforms

Table 24. Timing parameters (V_{DD} = 1.8 V +/- 0.15 V, V_{DDIO} = 3.3 V +/- 0.3 V, T_{case} = -55˚C to +125˚C)

Name	Parameter	Reference edge	Min	Max	Unit
$t_{1553BRM0}$	clock to data output delay	rising 1553CK edge	2 [1)]	21 [1)]	ns
$t_{1553BRM1}$	data input to clock setup	rising 1553CK edge	-	-	ns [2)]
$t_{1553BRM2}$	data input from clock hold	rising 1553CK edge	-	-	ns [2)]
$t_{1553BRM3}$	clock frequency	1553CK	16, 20, 24		MHz [3)]

Note 1: Parameter not measured during production test.

Note 2: The 1553RXA, 1553RXAN, 1553RXB and 1553RXBN inputs are re-synchronized internally.

Note 3: The core frequency must be lower than the internal system frequency: $t_{1553BRM3} < F_{CLK}$

2.4.14 I2C-master

The timing waveforms and timing parameters are shown in figure 18 and are defined in table 25.

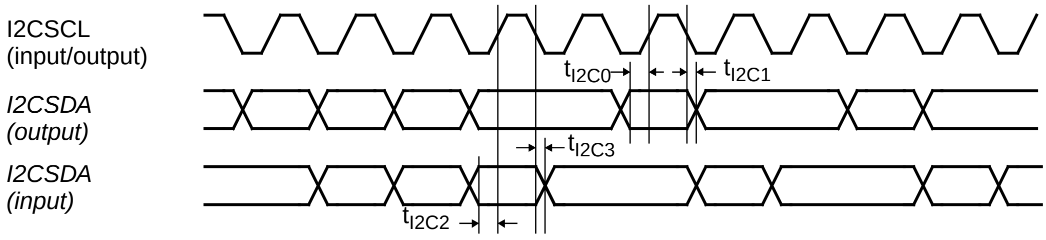

Figure 18. Timing waveforms

Table 25. Timing parameters (V_{DD} = 1.8 V +/- 0.15 V, V_{DDIO} = 3.3 V +/- 0.3 V, T_{case} = -55˚C to +125˚C)

Name	**Parameter**	**Reference edge**	**Min**	**Max**	**Unit**
t_{I2C0}	data output valid before clock	rising I2CSCL edge	-	scaler 1)	T_{CLK} periods
t_{I2C1}	data output valid after clock	falling I2CSCL edge	scaler 1)	-	T_{CLK} periods
t_{I2C2}	data input setup to clock	rising I2CSCL edge	2 2)	-	T_{CLK} periods
t_{I2C3}	data input hold from clock	falling I2CSCL edge	0 2)	-	T_{CLK} periods

Note 1: The core's I2C bus functional timing depends on the core's scaler value and the internal system clock T_{CLK} period. When the scaler is set for the core to operate in Fast- or Standard-Mode, the timing characteristics in the I2C-bus specification apply. The maximum T_{CLK} period for proper operation is 50 ns.

Note 2: The I2CSCL and I2CSDA inputs are re-synchronized to the internal system clock with a T_{CLK} period.

Note 3: I2CSCL and I2CSDA are open-drain outputs, driving a logical 0 level or tri-state.

Note 4: For correct operation, the signals should be pulled-up externally with 10 kOhm. GR712RC does not include any internal pull-up resistors.

2.4.15 SPI controller

The timing waveforms and timing parameters are shown in figure 19 and are defined in table 26.

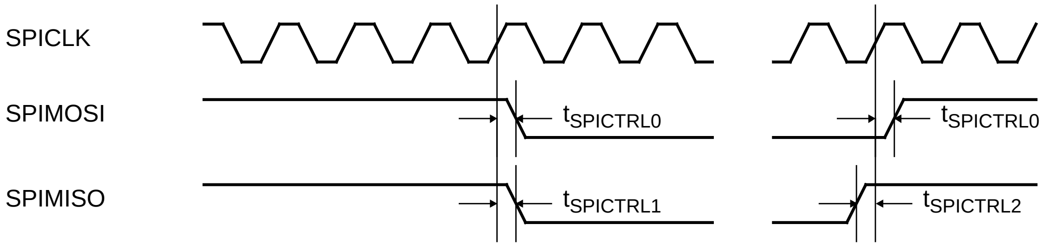

Figure 19. Timing waveforms

Table 26. Timing parameters (V_{DD} = 1.8 V +/- 0.15 V, V_{DDIO} = 3.3 V +/- 0.3 V, T_{case} = -55˚C to +125˚C)

Name	Parameter	Reference edge	Min	Max	Unit
$t_{SPICTRL0}$	clock to output delay	driving SPICLK edge	-15 [2)]	15 [2)]	ns [1)]
$t_{SPICTRL1}$	input to clock hold	sampling SPICLK edge	0 [2)]	-	ns [3)]
$t_{SPICTRL2}$	input to clock setup	sampling SPICLK edge	20 [2)]	-	ns [3)]

Note 1: The driving and sampling edges of the interface are programmable, and always opposite to each other.

Note 2: Parameter not measured during production test.

Note 3: The SPIMISO input is re-synchronized to the internal system clock with a T_{CLK} period.

2.4.16 SLINK Serial Bus Based Real-Time Network Master

The timing waveforms and timing parameters are shown in figure 20 and are defined in table 27.

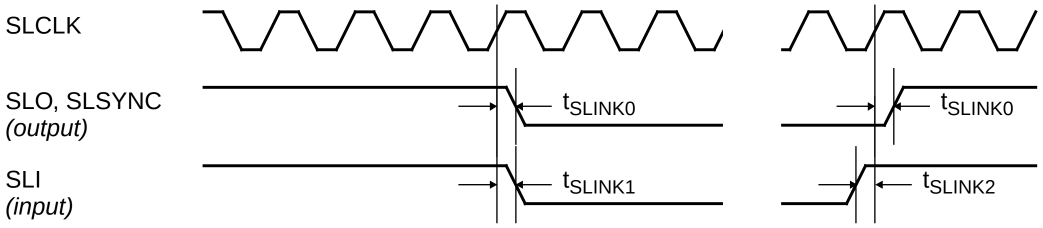

Figure 20. Timing waveforms

Table 27. Timing parameters (V_{DD} = 1.8 V +/- 0.15 V, V_{DDIO} = 3.3 V +/- 0.3 V, T_{case} = -55˚C to +125˚C)

Name	Parameter	Reference edge	Min	Max	Unit
t_{SLINK0}	clock to output delay	rising SLCLK edge	1	-	T_{CLK} periods [1)]
t_{SLINK1}	input to clock hold	rising SLCLK edge	0	-	T_{CLK} periods
t_{SLINK2}	input to clock setup	rising SLCLK edge	2	-	T_{CLK} periods

Note 1: Output timing depends on the ODEL setting in the core's control register. Outputs will transition (ODEL+1)*(system clock period) ns after SLCLK rising edge.

2.4.17 ASCS controller

The timing waveforms and timing parameters are shown in figure 21 and are defined in table 28.

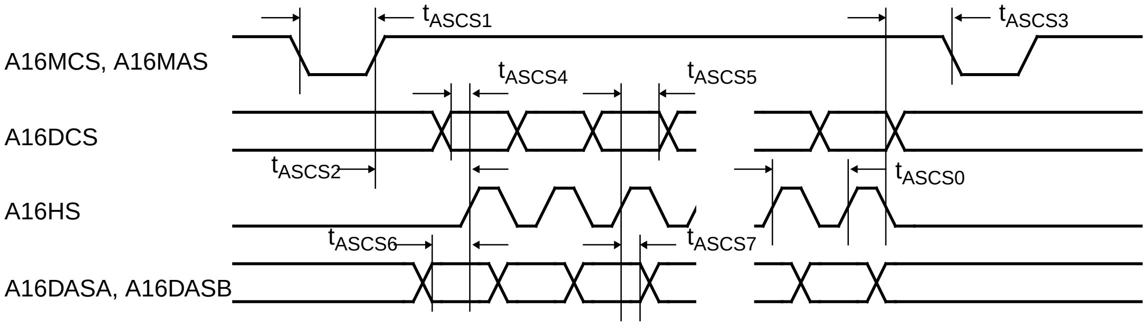

Figure 21. Timing waveforms

Table 28. Timing parameters (V_{DD} = 1.8 V +/- 0.15 V, V_{DDIO} = 3.3 V +/- 0.3 V, T_{case} = -55˚C to +125˚C)

Name	Parameter	Reference edge	Min	Max	Unit
t_{ASCS0}	clock period	rising A16HS edge	2	-	T_{CLK} periods 1)
t_{ASCS1}	qualifier de-asserted width	-	20	-	T_{CLK} periods 1)
t_{ASCS2}	qualifier asserted to clock	rising A16HS edge	8	-	T_{CLK} periods 1)
t_{ASCS3}	clock to qualifier de-asserted	falling A16HS edge	2	-	T_{CLK} periods 1)
t_{ASCS4}	output data to clock setup	rising A16HS edge	1	-	T_{CLK} periods 1)
t_{ASCS5}	output data after clock hold	rising A16HS edge	1	-	T_{CLK} periods 1)
t_{ASCS6}	input data to clock setup	rising A16HS edge	2	-	T_{CLK} periods
t_{ASCS7}	input data after clock hold	rising A16HS edge	2	-	T_{CLK} periods

Note 1: The timing of the interface is programmable and is dependable on the t_{ASCS0} clock period.

2.4.18 CCSDS / ECSS Telecommand Decoder

The timing waveforms and timing parameters are shown in figure 22 and are defined in table 29.

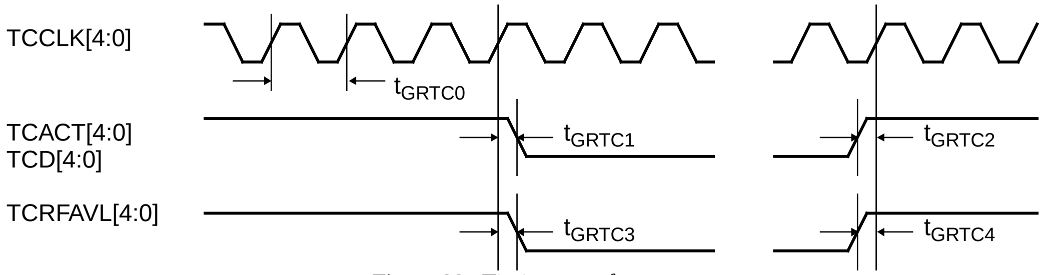

Figure 22. Timing waveforms

Table 29. Timing parameters (V_{DD} = 1.8 V +/- 0.15 V, V_{DDIO} = 3.3 V +/- 0.3 V, T_{case} = -55˚C to +125˚C)

Name	Parameter	Reference edge	Min	Max	Unit
t_{GRTC0}	bit period	rising TCCLK edge	7	-	T_{CLK} periods
t_{GRTC1}	data/active input to clock hold	rising TCCLK edge	3	-	T_{CLK} periods
t_{GRTC2}	data/active input to clock setup	rising TCCLK edge	3	-	T_{CLK} periods
t_{GRTC3}	RF available input to clock hold	rising INCLK edge	-	-	ns [1)]
t_{GRTC4}	RF available input to clock setup	rising INCLK edge	-	-	ns [1)]

Note 1: The TCRFAVL[4:0] inputs are re-synchronized to the internal system clock with a T_{CLK} period.

2.4.19 CCSDS / ECSS Telemetry Encoder

The timing waveforms and timing parameters are shown in figure 23 and are defined in table 30.

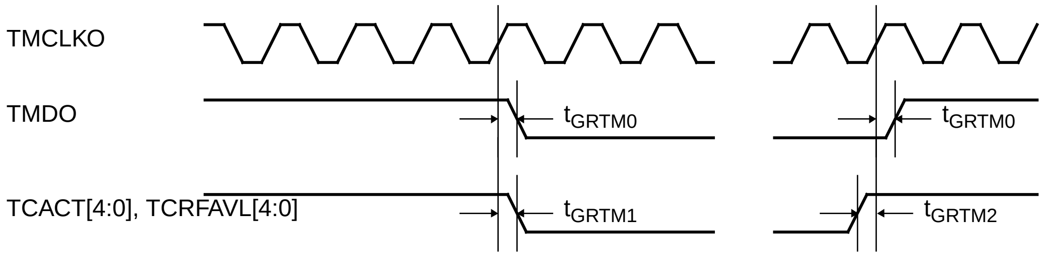

Figure 23. Timing waveforms

Table 30. Timing parameters (V_{DD} = 1.8 V +/- 0.15 V, V_{DDIO} = 3.3 V +/- 0.3 V, T_{case} = -55˚C to +125˚C)

Name	Parameter	Reference edge	Min	Max	Unit
t_{GRTM0}	clock to output delay	any TMCLKO edge	-15 [3)]	15 [3)]	ns [1)]
t_{GRTM1}	input to clock hold	rising INCLK edge	-	-	ns [2)]
t_{GRTM2}	input to clock setup	rising INCLK edge	-	-	ns [2)]
t_{GRTM3}	input to output delay	TMCLKI to TMCLKO	0 [3)]	23 [3)]	ns
t_{GRTM4}	TMCLKI clock period	-	20 [3)]		ns

Note 1: The TMDO signal is output simultaneously with the programmable TMCLKO clock edge. The opposite clock edge should be used for sampling TMDO.

Note 2: The TCACT[4:0] and TCRFAVL[4:0] inputs are re-synchronized to the T_{CLK} period.

Note 3: Parameter not measured during production test.

3 Mechanical description

3.1 Package

Ceramic hermetically sealed CQFP-240L package with 0.5 mm lead pitch, with gold plated leads.

See drawing in section 3.3.

All devices are marked on top lid with GR712RC. For space class marking see the product specification [PS].

Lead trimming and forming are performed by customer prior to assembly on printed circuit board.

3.2 Pin assignment

The pin assignment in table 31 shows the implementation characteristics of each signal, indicating how each pin has been configured in terms of maximum load, polarity and reset value.

Table 31. Pin assignment

Pin no.	Pin name	Dir.	Max load [pF]	Polarity	Reset value	Note
1	SWMX[3]	In		-		I/O Switch Matrix 3
2	SWMX[2]	Out	50	-	High	I/O Switch Matrix 2
3	SWMX[1]	In		-		I/O Switch Matrix 1
4	SWMX[0]	Out	50	-	High	I/O Switch Matrix 0
5	CB[6]	In/Out	50	-	High-Z	Check Bit 6
6	VDDIO					I/O Supply Voltage
7	GNDIO [2)]					I/O Supply Ground
8	CB[5]	In/Out	50	-	High-Z	Check Bit 5
9	CB[4]	In/Out	50	-	High-Z	Check Bit 4
10	CB[3]	In/Out	50	-	High-Z	Check Bit 3
11	CB[2]	In/Out	50	-	High-Z	Check Bit 2
12	CB[1]	In/Out	50	-	High-Z	Check Bit 1
13	VDD					Core Supply Voltage
14	GND					Core Supply Ground
15	CB[0]	In/Out	50	-	High-Z	Check Bit 0
16	DATA[31]	In/Out	50	-	High-Z	Data Bit 31
17	DATA[30]	In/Out	50	-	High-Z	Data Bit 30
18	VDDIO					I/O Supply Voltage
19	GNDIO					I/O Supply Ground
20	DATA[29]	In/Out	50	-	High-Z	Data Bit 29
21	DATA[28]	In/Out	50	-	High-Z	Data Bit 28
22	DATA[27]	In/Out	50	-	High-Z	Data Bit 27
23	DATA[26]	In/Out	50	-	High-Z	Data Bit 26
24	DATA[25]	In/Out	50	-	High-Z	Data Bit 25
25	DATA[24]	In/Out	50	-	High-Z	Data Bit 24
26	DATA[23]	In/Out	50	-	High-Z	Data Bit 23
27	DATA[22]	In/Out	50	-	High-Z	Data Bit 22
28	VDDIO					I/O Supply Voltage
29	GNDIO					I/O Supply Ground
30	VDD					Core Supply Voltage
31	GND					Core Supply Ground

Table 31. Pin assignment

Pin no.	Pin name	Dir.	Max load [pF]	Polarity	Reset value	Note
32	DATA[21]	In/Out	50	-	High-Z	Data Bit 21
33	DATA[20]	In/Out	50	-	High-Z	Data Bit 20
34	DATA[19]	In/Out	50	-	High-Z	Data Bit 19
35	DATA[18]	In/Out	50	-	High-Z	Data Bit 18
36	DATA[17]	In/Out	50	-	High-Z	Data Bit 17
37	DATA[16]	In/Out	50	-	High-Z	Data Bit 16
38	VDDIO					I/O Supply Voltage
39	GNDIO					I/O Supply Ground
40	DATA[15]	In/Out	50	-	High-Z	Data Bit 15
41	DATA[14]	In/Out	50	-	High-Z	Data Bit 14
42	DATA[13]	In/Out	50	-	High-Z	Data Bit 13
43	DATA[12]	In/Out	50	-	High-Z	Data Bit 12
44	DATA[11]	In/Out	50	-	High-Z	Data Bit 11
45	DATA[10]	In/Out	50	-	High-Z	Data Bit 10
46	DATA[9]	In/Out	50	-	High-Z	Data Bit 9
47	VDD					Core Supply Voltage
48	GND					Core Supply Ground
49	DATA[8]	In/Out	50	-	High-Z	Data Bit 8
50	VDDIO					I/O Supply Voltage
51	GNDIO					I/O Supply Ground
52	DATA[7]	In/Out	50	-	High-Z	Data Bit 7
53	DATA[6]	In/Out	50	-	High-Z	Data Bit 6
54	DATA[5]	In/Out	50	-	High-Z	Data Bit 5
55	DATA[4]	In/Out	50	-	High-Z	Data Bit 4
56	DATA[3]	In/Out	50	-	High-Z	Data Bit 3
57	DATA[2]	In/Out	50	-	High-Z	Data Bit 2
58	DATA[1]	In/Out	50	-	High-Z	Data Bit 1
59	DATA[0]	In/Out	50	-	High-Z	Data Bit 0
60	VDDIO					I/O Supply Voltage
61	GNDIO					I/O Supply Ground
62	ADDRESS[0]	Out	50	-	Low	Address Bit 0
63	ADDRESS[1]	Out	50	-	Low	Address Bit 1
64	ADDRESS[2]	Out	100	-	Low	Address Bit 2
65	ADDRESS[3]	Out	100	-	Low	Address Bit 3
66	VDD					Core Supply Voltage
67	GND					Core Supply Ground
68	ADDRESS[4]	Out	100	-	Low	Address Bit 4
69	VDDIO					I/O Supply Voltage
70	GNDIO					I/O Supply Ground
71	ADDRESS[5]	Out	100	-	Low	Address Bit 5
72	ADDRESS[6]	Out	100	-	Low	Address Bit 6
73	ADDRESS[7]	Out	100	-	Low	Address Bit 7
74	ADDRESS[8]	Out	100	-	Low	Address Bit 8
75	VDDIO					I/O Supply Voltage
76	GNDIO					I/O Supply Ground
77	ADDRESS[9]	Out	100	-	Low	Address Bit 9
78	VDD					Core Supply Voltage

Table 31. Pin assignment

Pin no.	Pin name	Dir.	Max load [pF]	Polarity	Reset value	Note
79	GND					Core Supply Ground
80	ADDRESS[10]	Out	100	-	Low	Address Bit 10
81	ADDRESS[11]	Out	100	-	Low	Address Bit 11
82	ADDRESS[12]	Out	100	-	Low	Address Bit 12
83	VDDIO					I/O Supply Voltage
84	GNDIO					I/O Supply Ground
85	ADDRESS[23]	Out	50	-	Low	Address Bit 23
86	ADDRESS[13]	Out	100	-	Low	Address Bit 13
87	ADDRESS[22]	Out	50	-	Low	Address Bit 22
88	ADDRESS[21]	Out	50	-	Low	Address Bit 21
89	ADDRESS[14]	Out	100	-	Low	Address Bit 14
90	VDD					Core Supply Voltage
91	GND					Core Supply Ground
92	ADDRESS[20]	Out	50	-	Low	Address Bit 20
93	VDDIO					I/O Supply Voltage
94	GNDIO					I/O Supply Ground
95	ADDRESS[19]	Out	50	-	Low	Address Bit 19
96	ADDRESS[15]	Out	100	-	Low	Address Bit 15
97	ADDRESS[18]	Out	50	-	Low	Address Bit 18
98	ADDRESS[16]	Out	100	-	Low	Address Bit 16
99	ADDRESS[17]	Out	50	-	Low	Address Bit 17
100	SCANEN	In		High		Scan enable (tie to ground)
101	ROMSN[0]	Out	50	Low	High	PROM Select 0
102	VDD					Core Supply Voltage
103	GND					Core Supply Ground
104	VDDIO					I/O Supply Voltage
105	GNDIO					I/O Supply Ground
106	ROMSN[1]	Out	50	Low	High	PROM Select 1
107	WRITEN	Out	50	Low	High	Write Strobe for PROM, I/O
108	IOSN	Out	50	Low	High	I/O Select
109	RAMSN[0]	Out	50	Low	High	SRAM Select 0
110	RAMSN[1]	Out	50	Low	High	SRAM Select 1
111	RAMOEN	Out	50	Low	High	SRAM Output Enable
112	RAMWEN	Out	50	Low	High	SRAM Write Enable
113	BRDYN	In		Low		Bus Ready
114	VDD					Core Supply Voltage
115	GND					Core Supply Ground
116	VDDIO					I/O Supply Voltage
117	GNDIO					I/O Supply Ground
118	BEXCN	In		Low		Bus Exception
119	WDOGN	Out	50	Low	High-Z	Watchdog Indicator (output is driven active low, else it is in tri-state and therefore requires external pull-up)
120	READ	Out	50	High	High	SRAM, PROM, I/O read indicator
121	TDI	In		-		Jtag Test Data In
122	TCK	In		-		Jtag Test Clock
123	TMS	In		High		Jtag Test Mode Select
124	TDO	Out	50	-	Low	Jtag Test Data Out

Table 31. Pin assignment

Pin no.	Pin name	Dir.	Max load [pF]	Polarity	Reset value	Note
125	TESTEN	In		High		Test Enable (tie to ground)
126	OEN	Out		Low	High	Output Enable for PROM, I/O
127	SWMX[66]	In/Out	50	-	High-Z	I/O Switch Matrix 66
128	SWMX[65]	In/Out	50	-	High-Z	I/O Switch Matrix 65
129	SWMX[64]	In/Out	50	-	High-Z	I/O Switch Matrix 64
130	VDDIO					I/O Supply Voltage
131	GNDIO					I/O Supply Ground
132	SWMX[63]	In/Out	50	-	High-Z	I/O Switch Matrix 63
133	VDD					Core Supply Voltage
134	GND					Core Supply Ground
135	SWMX[62]	In/Out	50	-	High-Z	I/O Switch Matrix 62
136	SWMX[61]	In/Out	50	-	High-Z	I/O Switch Matrix 61
137	SWMX[60]	In/Out	50	-	High-Z	I/O Switch Matrix 60
138	VDDIO					I/O Supply Voltage
139	GNDIO					I/O Supply Ground
140	SWMX[59]	In/Out	50	-	High-Z	I/O Switch Matrix 59
141	CB[7]	In/Out	50	-	High-Z	Check Bit 7
142	SWMX[58]	In/Out	50	-	High-Z	I/O Switch Matrix 58
143	SWMX[57]	In/Out	50	-	High-Z	I/O Switch Matrix 57
144	SWMX[56]	In		-		I/O Switch Matrix 56
145	RESETN	In		Low		System Reset
146	ERRORN	Out	50	Low	High-Z	Processor Error Mode (output is driven active low, else it is in tri-state and therefore requires external pull-up)
147	DLLBPN	In		Low		DLL Bypass
148	INCLK	In		-		Input Clock
149	VDDIO					I/O Supply Voltage
150	VDD					Core Supply Voltage
151	GND					Core Supply Ground
152	GNDIO					I/O Supply Ground
153	SWMX[55]	In		-		I/O Switch Matrix 55
154	SWMX[54]	In/Out	100	-	High-Z	I/O Switch Matrix 54
155	SWMX[53]	In/Out	100	-	High-Z	I/O Switch Matrix 53
156	SDCLK	Out	100	-	-	SDRAM Clock
157	SWMX[52]	In/Out	100	-	High-Z	I/O Switch Matrix 52
158	VDDIO					I/O Supply Voltage
159	GNDIO					I/O Supply Ground
160	SWMX[51]	In		-		I/O Switch Matrix 51
161	SWMX[50]	In		-		I/O Switch Matrix 50
162	SWMX[49]	In/Out	100	-	High-Z	I/O Switch Matrix 49
163	SWMX[48]	In/Out	100	-	High-Z	I/O Switch Matrix 48
164	SWMX[47]	In		-		I/O Switch Matrix 47
165	SWMX[46]	In		-		I/O Switch Matrix 46
166	SWMX[45]	In/Out	50	-	High-Z	I/O Switch Matrix 45 [1)]
167	VDD					Core Supply Voltage
168	GND					Core Supply Ground
169	SWMX[44]	In/Out	50	-	High-Z	I/O Switch Matrix 44
170	VDDIO					I/O Supply Voltage

Table 31. Pin assignment

Pin no.	Pin name	Dir.	Max load [pF]	Polarity	Reset value	Note
171	GNDIO					I/O Supply Ground
172	SWMX[43]	In/Out	50	-	High-Z	I/O Switch Matrix 43 1)
173	SWMX[42]	In		-		I/O Switch Matrix 42
174	SWMX[41]	In/Out	50	-	High-Z	I/O Switch Matrix 41
175	SWMX[40]	In/Out	50	-	High-Z	I/O Switch Matrix 40 1)
176	SWMX[39]	In		-		I/O Switch Matrix 39
177	SWMX[38]	In		-		I/O Switch Matrix 38
178	SWMX[37]	In/Out	50	-	High-Z	I/O Switch Matrix 37 1)
179	SWMX[36]	In/Out	50	-	High-Z	I/O Switch Matrix 36
180	VDDIO					I/O Supply Voltage
181	GNDIO					I/O Supply Ground
182	SWMX[35]	In		-		I/O Switch Matrix 35
183	SWMX[34]	In		-		I/O Switch Matrix 34
184	SWMX[33]	In/Out	50	-	High-Z	I/O Switch Matrix 33
185	SWMX[32]	In/Out	50	-	High-Z	I/O Switch Matrix 32
186	VDD					Core Supply Voltage
187	GND					Core Supply Ground
188	SWMX[31]	In		-		I/O Switch Matrix 31
189	SWMX[30]	In		-		I/O Switch Matrix 30
190	SWMX[29]	In/Out	50	-	High-Z	I/O Switch Matrix 29
191	SWMX[28]	In/Out	50	-	High-Z	I/O Switch Matrix 28
192	SWMX[27]	In		-		I/O Switch Matrix 27
193	SWMX[26]	In		-		I/O Switch Matrix 26
194	VDDIO					I/O Supply Voltage
195	GNDIO					I/O Supply Ground
196	SWMX[25]	In/Out	100	-	High-Z	I/O Switch Matrix 25
197	SWMX[24]	In/Out	100	-	High-Z	I/O Switch Matrix 24
198	VDD					Core Supply Voltage
199	GND					Core Supply Ground
200	SWMX[23]	In		-		I/O Switch Matrix 23
201	SWMX[22]	In		-		I/O Switch Matrix 22
202	SWMX[21]	In/Out	100	-	High-Z	I/O Switch Matrix 21
203	SWMX[20]	In/Out	100	-	High-Z	I/O Switch Matrix 20
204	SPW_RXD[1]			-		SpaceWire Receive Data 1
205	SPW_RXS[1]			-		SpaceWire Receive Strobe 1
206	SPW_TXD[1]	Out	100	-	Low	SpaceWire Transmit Data 1
207	VDDIO					I/O Supply Voltage
208	GNDIO					I/O Supply Ground
209	SPW_TXS[1]	Out	100	-	Low	SpaceWire Transmit Strobe 1
210	VDD					Core Supply Voltage
211	GND					Core Supply Ground
212	SPWCLK	In		-		SpaceWire Receiver and Transmitter Clock
213	SPW_RXD[0]	In		-		SpaceWire Receive Data 0
214	SPW_RXS[0]	In		-		SpaceWire Receive Strobe 0
215	SPW_TXD[0]	Out	100	-	Low	SpaceWire Transmit Data 0
216	SPW_TXS[0]	Out	100	-	Low	SpaceWire Transmit Strobe 0
217	SWMX[19]	In	50	-		I/O Switch Matrix 19

Table 31. Pin assignment

Pin no.	Pin name	Dir.	Max load [pF]	Polarity	Reset value	Note
218	SWMX[18]	In		-		I/O Switch Matrix 18
219	SWMX[17]	In/Out	100	-	High-Z	I/O Switch Matrix 17
220	SWMX[16]	In/Out	100	-	High-Z	I/O Switch Matrix 16
221	VDDIO					I/O Supply Voltage
222	VDD					Core Supply Voltage
223	GND					Core Supply Ground
224	GNDIO					I/O Supply Ground
225	SWMX[15]	In		-		I/O Switch Matrix 15
226	SWMX[14]	In		-		I/O Switch Matrix 14
227	SWMX[13]	In/Out	100	-	High-Z	I/O Switch Matrix 13
228	SWMX[12]	In/Out	100	-	High-Z	I/O Switch Matrix 12
229	SWMX[11]	In		-		I/O Switch Matrix 11
230	SWMX[10]	In/Out	50	-	High-Z	I/O Switch Matrix 10
231	SWMX[9]	In		-		I/O Switch Matrix 09
232	SWMX[8]	In/Out	50	-	High-Z	I/O Switch Matrix 08
233	SWMX[7]	In		-		I/O Switch Matrix 07
234	VDD					Core Supply Voltage
235	GND					Core Supply Ground
236	VDDIO					I/O Supply Voltage
237	GNDIO					I/O Supply Ground
238	SWMX[6]	In/Out	50	-	High-Z	I/O Switch Matrix 06 [1)]
239	SWMX[5]	In		-		I/O Switch Matrix 05
240	SWMX[4]	In/Out	50	-	High-Z	I/O Switch Matrix 04 [1)]

Note 1: See tables 3 and 5 for detailed description of behavior at reset.

Note 2: GNDIO is connected internally to GND.

3.3 Mechanical package drawings

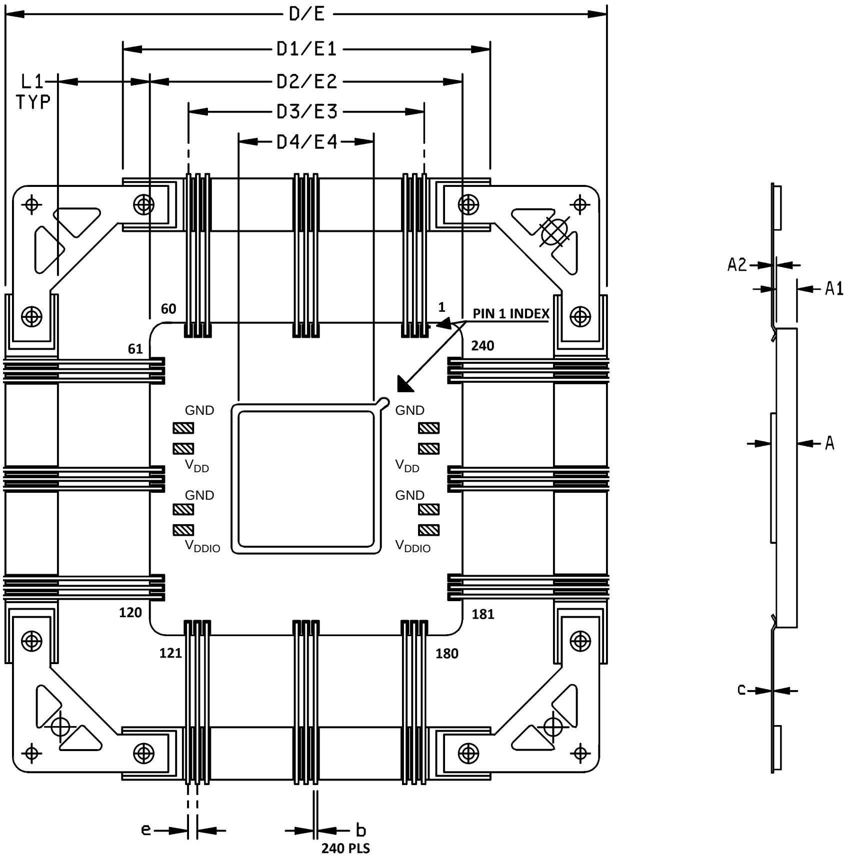

Figure 24. Top view

Table 32. Dimensions

		Millimeters	
		Min.	**Max.**
A	Total height	---	3.50
A1	Body height	---	2.75
A2		0.10	0.40
b	Lead width	0.15	0.25
c	Lead height	0.10	0.20
D/E		74.80	75.40
D1/E1		55.44	56.56
D2/E2		31.75	32.25
D3/E3		29.50 BSC	
D4/E4		21.00 TYP	
e	Lead pitch	0.50 BSC	
L1		16.50 TYP	

Note 1: The seal ring is electrically connected to GND.

Note 2: Package weight is 16   1 grams, including the lead-frame.

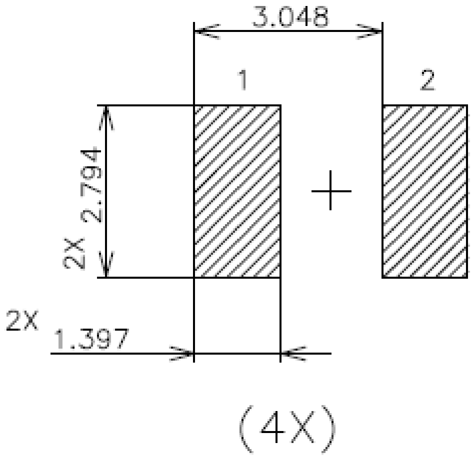

Figure 25. Capacitor pads on top of package (mm)

4 Reference documents

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[PS] Product Specification GR712RC, GR712RC-PS, Aeroflex Gaisler

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[MIL883] Test Method Standard, Microcircuits, revision H, 26 February 2010, MIL-STD-883H

[MIL38535] Integrated Circuits (Microcircuits) Manufacturing, General Specification For, revision J, 28 December 2010, MIL-PRF-38535J

5 Screening, qualification, and quality control

GR712RC is provided as a high reliability product for space, for which space level screening and qualifications tests are performed in accordance to the product specification [PS].

A Certificate of Compliance is delivered with space grade parts.

A procurement specification is provided for space grade parts.

GR712RC is also provided in prototype grade in military or commercial temperature range.

6 Ordering information

Ordering information is provided in table 33 and a legend is provided in table 34.

Table 33. Ordering information, available models

Product	Description
GR712RC-MS-CG240	Flight model
GR712RC-MP-CG240	Electrical qualification model
GR712RC-CP-CG240	Engineering model (prototype)

Table 34. Ordering legend

Designator	Option	Description
Product	GR712RC	Dual-core LEON3-FT SPARC V8 Processor
Temperature Range	M	-55˚C to +125˚C (Military range)
	I	-40˚C to +85˚C (Industrial range)
	C	0˚C to +70˚C (Commercial range)
Screening Level	S	Space grade
	P	Prototype grade
Package Type	C	Ceramic Quad Flat Pack (CQFP)
Lead Finish	G	Gold
Lead Count	240	Number of leads

7 Change record

Change record information is provided in table 35.

Table 35. Change record

Issue	Date	Sections	Note
2.0	2013 February	1.2	Key features updated
		1.4	Signal descriptions clarified
		2.1	Absolute maximum ratings updated
		2.2	Recommended operating conditions updated
		2.3	DC parameters updated
		2.4	AC parameter test conditions clarified
		2.4.1, 2.4.3, 2.4.4, 2.4.5, 2.4.6, 2.4.7, 2.4.8, 2.4.9, 2.4.10, 2.4.11, 2.4.13, 2.4.15, 2.4.19	Updated timing
		1.5, 2.4.12	Obsolete proprietary function removed
		3.1	Package marking clarified
		3.2	GNDIO connection to GND clarified
		3.3	Weight information added
		4	Reference to product specification added
1.5	2012 May	1.5	The following conflicts added to table: CCSDS TC 0 vs. Proprietary CCSDS TC 0 vs. ASCS CCSDS TC 1 vs. Proprietary CCSDS TC 1 vs. Ethernet CCSDS TC 2 vs. Ethernet Proprietary vs. SpaceWire 2
1.4	2012 January	2.4.5	TCK edges in JTAG waveform & timing parameters corrected
1.3	2011 March	1.2, 2 4, 5 Table 6	Timing parameters redefined Qualification level specified Conflict between SLINK and CCSDS TC 3 clarified
1.2	2011 August	2.3	Added detailed core power consumption
1.1	2011 February	Tables 3 and 5 Tables 3, 4 and 19, figure 19 Table 31	SDDQM signals marked as active high GPIO1/GPIO2 names changed to GPIO Reference added regarding behavior at reset
1.0	2011 February	All	New document layout All pin descriptions, reset values etc. updated

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