FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-05602-5E

Microprocessor SPARClite

CMOS

Peripheral LSI for SPARClite

MB86941/942

■ DESCRIPTION

MB86941 and MB86942 are dedicated peripheral LSIs for SPARClite*.
The MB86941 and MB86942 are designed to enable compact configuration of high-performance systems with SPARClite architecture, and provide the following features.

* : SPARC is a registered trademark of SPARC International base on technology developed by Sun Microsystems, Inc. SPARClite is a trademark of SPARC International, Inc. licensed exclusively to Fujitsu Microelectronics, Inc.

■ FEATURES

Direct connection to SPARClite
Register read/write in 2 clock cycles up to 30MHz.
Register read/write in 3 clock cycles at 40MHz (MB86941) or 50MHz (MB86942).

Built-In On-Chip Modules:

- Interrupt controller
  Interrupt input: 15 channels
  Each interrupt input has independent masking and trigger mode settings
- 16-bit timer: 4 channels
  Two of the four channels have prescalers
  Each channel has five independent mode operations
  MODE0 : Periodical-interrupt
  MODE1 : Timeout-interrupt
  MODE2 : Square wave generator

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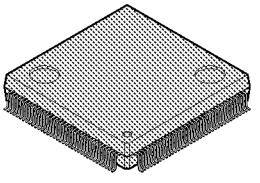
■ PACKAGE

144-pin Plastic QFP



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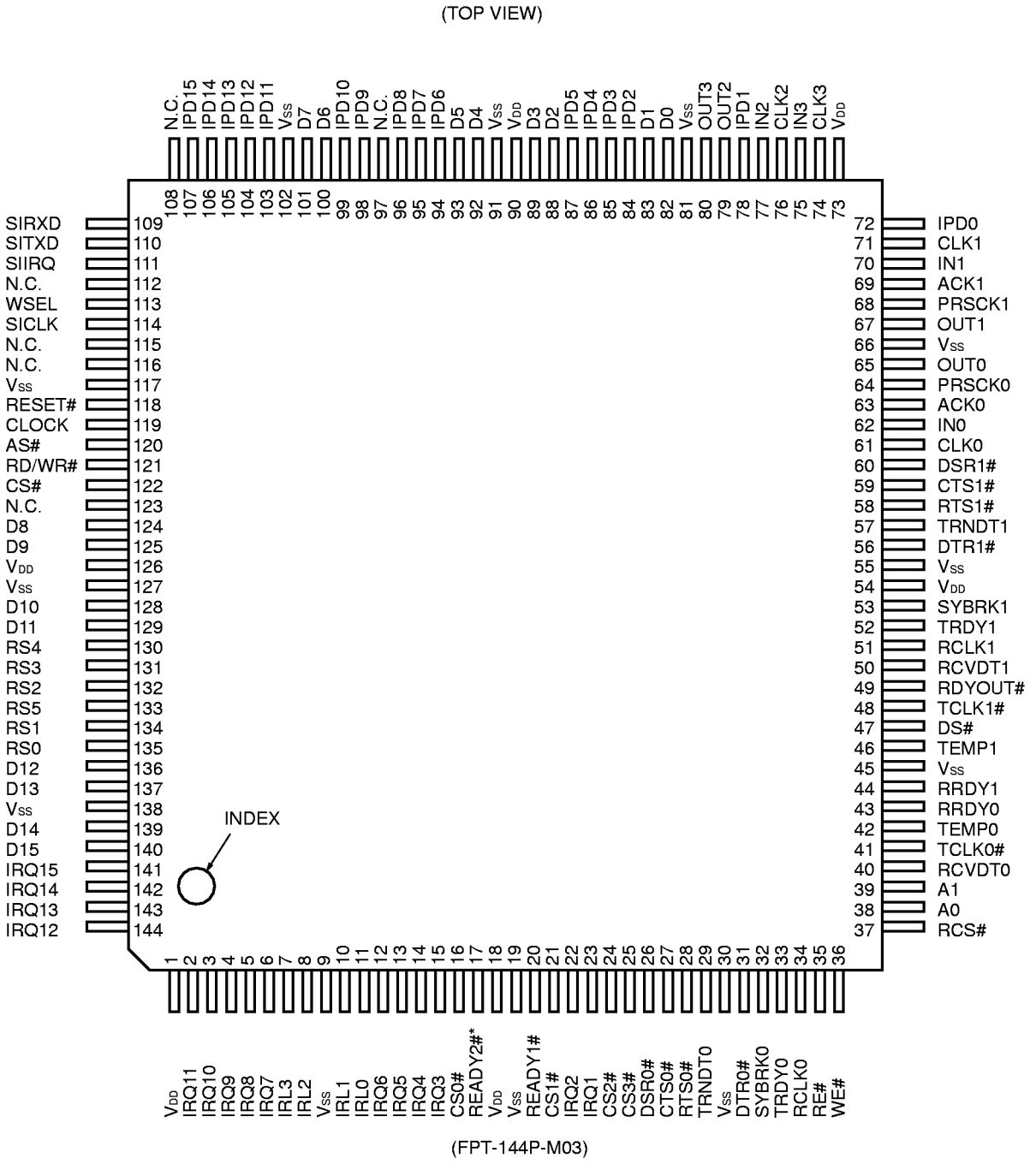
MODE3: Programmable one shot (software trigger)
MODE4: Programmable one shot (external trigger)

- SDTR (Serial data transmitter receiver): 2 channels
  MB89251A type
- Timing control, CS expansion
  Generates read, write and data strobe signals according to the requirements of external devices.
- SIO (Synchronous serial input/output)
  Simple synchronous type serial input/output
- I/O port, 16-bit
  Individual direction control by bit

5V single power supply (MB86941), 3.3V single power supply (MB86942)
Upward pin compatibility with MB86940C

■ PIN ASSIGNMENT



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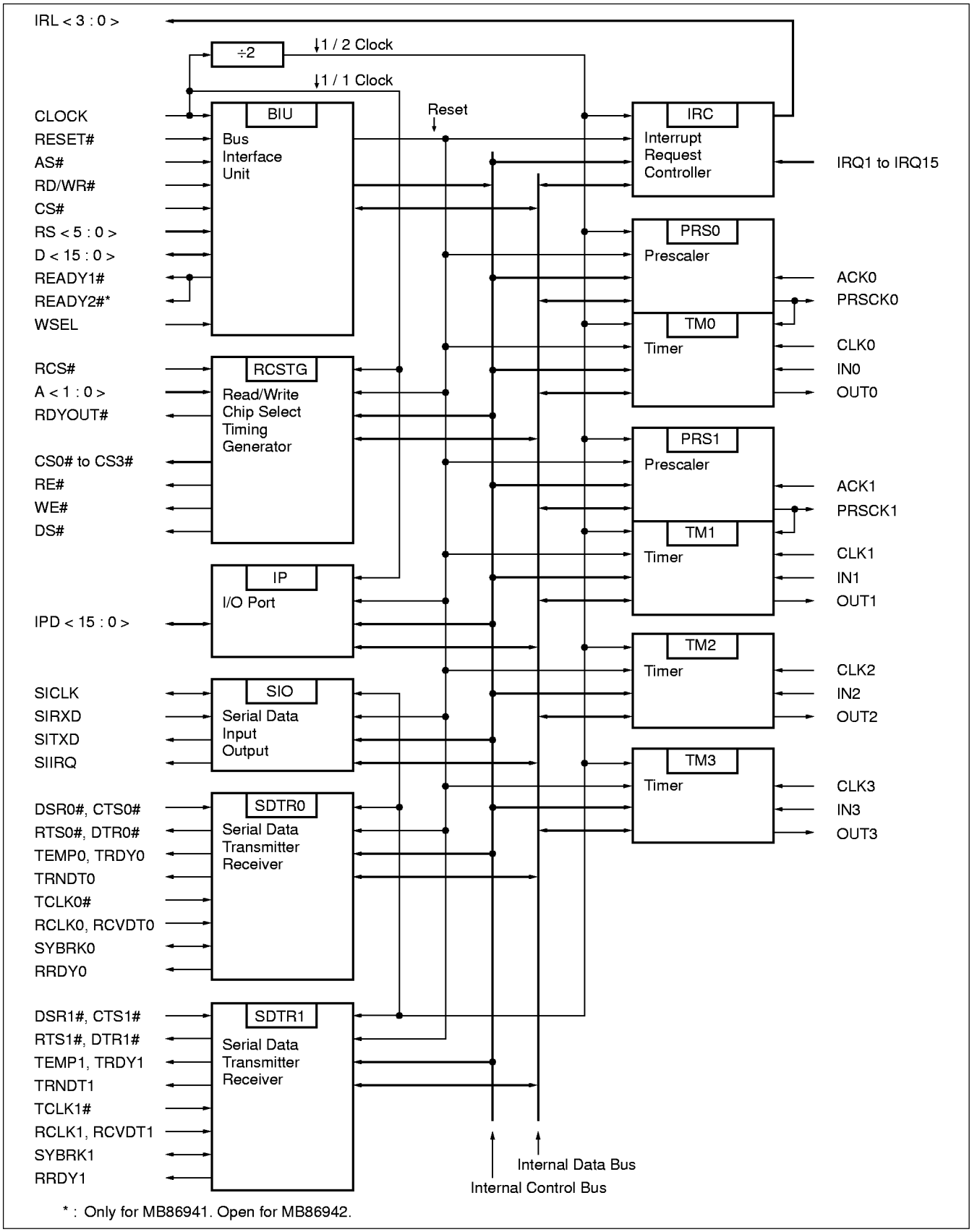
* : Only for MB86941. Open for MB86942.

■ BLOCK DIAGRAM



* : Only for MB86941. Open for MB86942.

■ DESCRIPTION OF BLOCK FUNCTIONS

1. BIU (Bus Interface Unit)

This block receives MPU (SPARClite) bus signals and bus controls signals (CLOCK, AS#, RD/WR#, CS#, ADR6 to ADR2, D<15:0>) and generates control signals for accessing MB86941/MB86942 internal resources. It also returns that Ready signal to the MPU which corresponds to the access time of each of such resources.

2. IRC (Interrupt Request Controller)

This block provides 15-channel interrupt input signals to transmit the interrupt level IRL <3:0> for each interrupt to the SPARClite.

3. TM (Timer) and PRS (Prescaler)

TM0 to TM3 are 16-bit timers serving as periodic interrupt generation timers, a watchdog timer, and an external event counter. The operating clock can be selected from among the internal clock, the clock frequency-divided by the prescaler, and the external clock.
Prescalers 0 and 1 are linked with timer channels 0 and 1, respectively. Each of the prescalers is initialized upon loading (or reloading) of the timer initial value of the corresponding timer.

4. SDTR (Serial Data Transmitter Receiver)

SDTR0 and SDTR1 are serial data transmitter/receiver modules programmable for control of transmission and reception.
The programming model is the same as that for the MB89251A.

5. RCSTG (Read/Write Timing Generator)

This module generates read, write, and data strobe signals conforming to the required timings for external connection of other devices. The assert timing and pulse width of each signal to be generated is programmable.

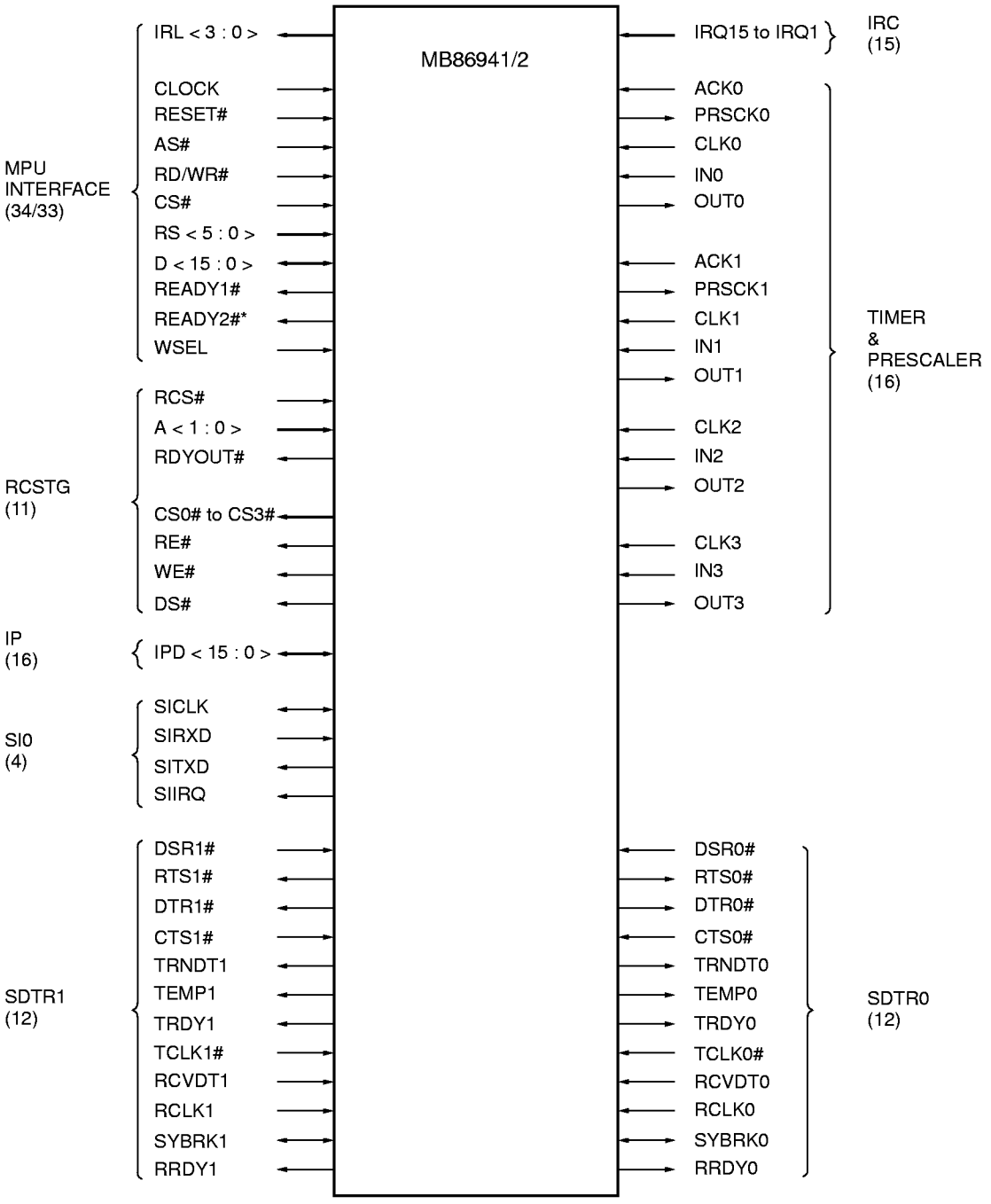
6. IP (I/O Port)

There are 16 I/O ports. The input/output direction of each port can be set by the control register.

7. SIO (Serial Data Input Output)

This block is a clock-synchronous serial interface. The transfer clock signal can be set to the internally generated or externally input one. The SIO outputs data to be transmitted and inputs received data in synchronization with the transfer clock signal.

■ PIN DESCRIPTION



V_{DD}: (6)
V_{SS}: (12)
N.C.: (6/7)

Note: Numerical value of a parenthesis shows numbers of PIN.

* : Only for MB86941. Open for MB86942.

1. MPU INTERFACE SIGNALS (34/33)

Pin symbol	I/O	Pin no.	Pin name	Description
RESET#	I	118	Reset	Reset input pin Input an "L" signal to this pin to reset the chip.
CLOCK	I	119	Clock	System clock input pin The chip contains some modules that use the clock signal from this pin (not divided), and other modules that use the clock signal divided in half. Clock not divided: BIU, RCSTG, IP Clock divided: IRC, PRS0, PRS1, TM0 to TM3, SDTR0, SDTR1, SIO
AS#	I	120	Address Strobe	Address strobe input pin Input an "L" signal to this pin to determine register access according to the signals input to the RS<5:0>, CS#, and RD/WR# pins.
RD/WR#	I	121	Read/Write	Read/write input pin Input an "H" signal to designate a read cycle, or an "L" signal to designate a write cycle.
CS#	I	122	Chip Select	Chip select input pin
RS0	I	135	Register Select 0	Register select input pin The combination of input signals to the RS<5:0> and CS# pins determines which register is accessed. The RS5 pin has internal pull-down resistance (MB86941 only).
RS1	I	134	Register Select 1	
RS2	I	132	Register Select 2	
RS3	I	131	Register Select 3	
RS4	I	130	Register Select 4	
RS5	I	133	Register Select 5	
READY1#	O	20	Ready 1	Data ready output pin MB86941: Open drain output with 12mA "L" drive capability. Drives an "H" level signal for 3ns before going to High-Z state. MB86942: Normal output. READY2# signal deleted. If the READY generator circuit in the MPU is used, it is not necessary to connect this pin to the MPU.
READY2#	O	17	Ready 2	
WSEL	I	113	Wait Select	Wait select input pin Input to this pin determines the interface timing with the MPU. Fix "L" to set register read/write access to 3 cycles, or fix "H" to set register read/write access to 2 cycles. This pin has internal pull-up resistance (MB86941 only).

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Pin symbol	I/O	Pin no.	Pin name	Description
D0	I/O	82	Data Bus 0	Data I/O port These pins are used to transfer register read/write data.
D1	I/O	83	Data Bus 1	
D2	I/O	88	Data Bus 2	
D3	I/O	89	Data Bus 3	
D4	I/O	92	Data Bus 4	
D5	I/O	93	Data Bus 5	
D6	I/O	100	Data Bus 6	
D7	I/O	101	Data Bus 7	
D8	I/O	124	Data Bus 8	
D9	I/O	125	Data Bus 9	
D10	I/O	128	Data Bus 10	
D11	I/O	129	Data Bus 11	
D12	I/O	136	Data Bus 12	
D13	I/O	137	Data Bus 13	
D14	I/O	139	Data Bus 14	
D15	I/O	140	Data Bus 15	
IRL0	O	11	Interrupt Request Level 0	Interrupt request output pin These pins are used to generate interrupts to the MPU and notify the interrupt level.
IRL1	O	10	Interrupt Request Level 1	
IRL2	O	8	Interrupt Request Level 2	
IRL3	O	7	Interrupt Request Level 3	

2. INTERRUPT REQUESTS (15)

Pin symbol	I/O	Pin no.	Pin name	Description
IRQ1	I	23	Interrupt Request 1	Interrupt request pin Interrupt receiving priority: IRQ15 is highest priority and IRQ1 is lowest. A choice of four interrupt waveforms is available by mode setting for each of the 15 pins independently, including “H” level, “L” level, rising edge, and falling edge. Each input has a filtering function for short pulse signals, by which an interrupt request is recognized once a signal is detected at active level at three successive rising edges of the internal clock signal. Once an interrupt request is detected, it passes through priority control and masking control and is output at the IRL<3:0> pins as an interrupt request to the MPU. If these pins are not used, they should be fixed at inactive level.
IRQ2	I	22	Interrupt Request 2	
IRQ3	I	15	Interrupt Request 3	
IRQ4	I	14	Interrupt Request 4	
IRQ5	I	13	Interrupt Request 5	
IRQ6	I	12	Interrupt Request 6	
IRQ7	I	6	Interrupt Request 7	
IRQ8	I	5	Interrupt Request 8	
IRQ9	I	4	Interrupt Request 9	
IRQ10	I	3	Interrupt Request 10	
IRQ11	I	2	Interrupt Request 11	
IRQ12	I	144	Interrupt Request 12	
IRQ13	I	143	Interrupt Request 13	
IRQ14	I	142	Interrupt Request 14	
IRQ15	I	141	Interrupt Request 15	

3. TIMER SIGNALS (16)

Pin symbol	I/O	Pin no.	Pin name	Description
CLK0	I	61	CLK0 : Timer Clock 0 to CLK3 : Timer Clock 3	Timer control signal pin These pins are used to input an external clock signal to the timer. In external clock mode these signals are synchronized with the internal clock.
IN0	I	62		
OUT0	O	65		
CLK1	I	71	IN0 : Timer Input 0 to IN3 : Timer Input 3	Input pin for count operation control signals to the timer In MODE0 through MODE3, the input signal is a gate signal. In MODE4, the pins input an external trigger signal.
IN1	I	70		
OUT1	O	67		
CLK2	I	76	OUT0 : Timer Output 0 to OUT3 : Timer Output 3	Timer output pin The output waveform is determined by the mode setting: • Periodic signal waveform output • Square wave output • One-shot pulse waveform output At reset, an “L” level signal is output.
IN2	I	77		
OUT2	O	79		
CLK3	I	74		
IN3	I	75		
OUT3	O	80		
ACK0	I	63	Asynchronous Clock 0	Prescaler asynchronous clock pin Input can be asynchronous with respect to the system clock signal input at the CLOCK pin. If an external clock signal is selected by the PRS0 and PRS1 registers, this signal can be used as a source clock for the prescaler. The clock signal divided by the prescaler is output at the PRSCK0, PRSCK1 pins. If these pins are not used, they should be fixed at “L” level.
ACK1	I	69	Asynchronous Clock 1	
PRSCK0	O	64	Prescaler Clock Output 0	Prescaler clock output pin An “L” level signal is output at reset.
PRSCK1	O	68	Prescaler Clock Output 1	

4. SDTR SIGNALS (24)

Pin symbol	I/O	Pin no.	Pin name	Description
DSR0#	I	26	Data Set Ready 0	Modem control signal DSR input pin The status of these pins is indicated at the status register bit 7.
DSR1#	I	60	Data Set Ready 1	
RTS0#	O	28	Request To Send 0	Modem control signal RTS output pin Set the command register bit 5 to “1” to output an “L” signal, or to “0” to output an “H” signal.
RTS1#	O	58	Request To Send 1	
DTR0#	O	31	Data Terminal Ready 0	These pins can be used as a DATA TERMINAL READY signal or a RATE SELECT signal of modem.Set the command register bit 1 to “1” to output an “L” signal, or to “0” to output an “H” signal.
DTR1#	O	56	Data Terminal Ready 1	
CTS0#	I	27	Clear To Send 0	Modem CLEAR TO SEND pin To enable sending, the command register bit 0 must be set to “1” and also an “L” level signal must be input at these pins.
CTS1#	I	59	Clear To Send 1	
TRNDT0	O	29	Transmit Data 0	Transmit Data pin Parallel data written to the data register is converted to serial data and output from these pins. In asynchronous mode, a start bit and stop bit are attached, and a parity bit may be attached if necessary. If there is no data to be sent in the SDTR module, in synchronous mode a synchronizing character is output and in asynchronous mode the pins go to mark mode. If a send-prohibited setting (command register bit 0 set to “0”) is in effect, or if an “H” signal is input at the CTS# pin, these pins to mark mode. However if a send-prohibited setting is entered while a sending operation is in progress, all sending data already written will be sent before these pins go to mark mode. In addition, in bisynchronous mode if the first synchronization character is being sent (synchronization standby), then these pins will go to mark mode after sending the second synchronization character.
TRNDT1	O	57	Transmit Data 1	
TEMP0	O	42	Transmit Empty 0	These pins indicate whether sending data is present. If there is no data to be sent in the SDTR module, the signal level is “H.” As soon as one byte of sending data is written, these pins go to “L” level at the fall of the write signal.
TEMP1	O	46	Transmit Empty 1	
TRDY0	O	33	Transmit Ready 0	Transmit Ready output pin When the CTS# signal is “L” and the command register is set to enable sending, these pins send an “H” level signal whenever the sending data buffer is empty.
TRDY1	O	52	Transmit Ready 1	

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Pin symbol	I/O	Pin no.	Pin name	Description
TCLK0#	I	41	Transmit Clock 0	Transmit Clock input pin In synchronous mode, the sending bit rate is fixed at the sending clock ×1, so that the clock signal input at these pins becomes the sending bit rate. In asynchronous mode, the sending bit rate will be the sending clock signal ×1, or ×1/16, or ×1/64 depending on the bit rate setting in the mode register. For example, if a 19.2 kHz clock signal is input at the TCLK# pin, the sending bit rate will be 19200 pbs with an ×1 setting, or 1200 pbs with an ×1/16 setting, or 300 pbs with an ×1/64 setting. Sending data is output in synchronization with the falling edge of the sending clock signal.
TCLK1#	I	48	Transmit Clock 1	
RCVDT0	I	40	Receive Data 0	Receive Data input pin Serial data input to these pins is converted to parallel data in the SDTR module and then can be read by the data bus.
RCVDT1	I	50	Receive Data 1	
RCLK0	I	34	Receive Clock 0	Receive Clock input pin In synchronous mode, the receiving bit rate is fixed at the receiving clock ×1, so that the clock signal input at these pins becomes the receiving bit rate. In asynchronous mode, the receiving bit rate will be the sending clock signal ×1, or ×1/16, or ×1/64 depending on the bit rate setting in the mode register. For example, if a 19.2 kHz clock signal is input at the RCLK pin, the receiving bit rate will be 19200 pbs with an ×1 setting, or 1200 pbs with an ×1/16 setting, or 300pbs with an ×1/64 setting. Receiving data is sampled in synchronization with the rising edge of the receiving clock signal. Note that in asynchronous mode ×1 speed differs from ×1/16 and ×1/64 speeds in that external synchronization of the RCLK and RCVDT signals is required.
RCLK1	I	51	Receive Clock 1	

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Pin symbol	I/O	Pin no.	Pin name	Description
SYBRK0	I/O	32	Synchronous/Break Detect 0	These pins can function as synchronization detect input, synchronization detect output, or break detect output pins, depending on the mode setting. • External synchronization mode setting: Synchronization signals are input at these pins. When the RCLK is "H" level and these pins receive an "H" signal in hunting operation, the data sampled at the next rise of RCLK is the starting bit of the receiving data. • Internal synchronization mode: These pins are used as the synchronization character detect output pins. When incoming data matches the synchronization character register setting (both characters must match in bisynchronous mode), an "H" signal is output here. Next, the status register is read and this signal returns to "L" at the end of the read signal. • Asynchronous mode: These pins function as break detect output pins. Immediately after a framing error, an "H" signal is output if all receiving data values (one frame including start bit, parity bit, and stop bit) are "0." This "H" signal is cancelled if a "1" data is received before a reset is applied.
SYBRK1	I/O	53	Synchronous/Break Detect 1	
RRDY0	O	43	Receive Ready 0	Receive Ready output pin These pins are "H" level, when serial data received at the RCVDT0, RCVDT1 pins is converted to parallel data in the SDTR module and is in readable form. Then after the received data is read, these pins becomes "L" level at the end of the read signal.
RRDY1	O	44	Receive Ready 1	

5. RCSTG SIGNALS (11)

Pin symbol	I/O	Pin no.	Pin name	Description
CS0#	O	16	Expansion Chip Select 0	Expansion Chip Select output pin When the input to the RCS# pin is "L," one of these chip select signals will be active depending on the combination of input signals to the A0, A1 pins.
CS1#	O	21	Expansion Chip Select 1	
CS2#	O	24	Expansion Chip Select 2	
CS3#	O	25	Expansion Chip Select 3	
RE#	O	35	Expansion Read Enable	Expansion Read Enable output pin When the input to the RCS# pin is "L" and a bus cycle begins with an "H" input to the RD/WR# pin, this pin produces a pulse of the designated width and the designated timing.
WE#	O	36	Expansion Write Enable	Expansion Write Enable output pin When the input to the RCS# pin is "L" and a bus cycle begins with an "L" input to the RD/WR# pin, this pin produces a pulse of the designated width and the designated timing.
DS#	O	47	Expansion Data Strobe	Expansion Data Strobe output pin When a bus cycle begins with the RCS# pin input at "L" level, this pin produces a pulse of the designated width and the designated timing.
RCS#	I	37	Resource Chip Select	Resource Chip Select pin. This pin is used to input the chip select signal supplied to the module RCSTG. When the module RCSTG is used to generate the external resource chip select signals CS0# to CS3#, read strobe RE#, write strobe WE#, and data strobe DS#, the corresponding areas must be decoded. This pin has internal pull-up resistance (MB86941 only).
A0	I	38	Address 0	These are the input pins for the address signal to the module RCSTG. When the module RCSTG is used to generate the external resource chip select signals CS0# to CS3#, read strobe signal RE#, write strobe signal WE#, and data strobe signal DS#, this address input signal is used to designate the byte position in the corresponding area. When the input to the RCS# pins is "L"' level, the input signal to these pins determines which of the external resource chip select signals CS0# to CS3# goes active. These pins have internal pull-up resistance (MB86941 only).
A1	I	39	Address 1	
RDYOUT#	O	49	Ready Out	This is the output pin for the ready signal generated by the module RCSTG. When the module RCSTG is used to generate the external resource chip select signals CS0#-CS3#, read strobe signal RE#, write strobe signal WE#, and data strobe signal DS#, the ready signal is output from these pins to the MPU. When any of the signals CS0# to CS1# is at "L" level, this signal is asserted with the designated timing interval.

6. I/O PORT SIGNALS (16)

Pin symbol	I/O	Pin no.	Pin name	Description
IPD0	I/O	72	I/O Port 0	Signal I/O port These pins may be used for input or output, as determined by register setting. These pins have internal pull-up resistance (MB86941 only).
IPD1	I/O	78	I/O Port 1	
IPD2	I/O	84	I/O Port 2	
IPD3	I/O	85	I/O Port 3	
IPD4	I/O	86	I/O Port 4	
IPD5	I/O	87	I/O Port 5	
IPD6	I/O	94	I/O Port 6	
IPD7	I/O	95	I/O Port 7	
IPD8	I/O	96	I/O Port 8	
IPD9	I/O	98	I/O Port 9	
IPD10	I/O	99	I/O Port 10	
IPD11	I/O	103	I/O Port 11	
IPD12	I/O	104	I/O Port 12	
IPD13	I/O	105	I/O Port 13	
IPD14	I/O	106	I/O Port 14	
IPD15	I/O	107	I/O Port 15	

7. SIO SIGNALS (4)

Pin symbol	I/O	Pin no.	Pin name	Description
SICLK	I/O	114	SIO Clock	This is the input/output pin for the clock signal used for SIO serial data transfer. In external clock mode, the clock signal for serial data transfer is input at this pin. In internal clock mode, the clock signal from the internal clock generator is output at this pin. This pin has internal pull-up resistance (MB86941 only).
SIRXD	I	109	SIO Receive Data	SIO Receive Data input pin This pin receives data input LSB first, synchronously with the SICLK pin clock signal. This pin has internal pull-up resistance (MB86941 only).
SITXD	O	110	SIO Transmit Data	SIO Transmit Data output pin This pin outputs data LSB first, synchronously with the SICLK pin clock signal.
SIIRQ	O	111	SIO Interrupt Request	SIO Interrupt Request output pin

8. V_{DD}, V_{SS}, N.C. (24/25)

Pin symbol	I/O	Pin no.	Pin name	Description
V_{DD}	—	1, 18, 54, 73, 90, 126	—	Power supply input pin
V_{SS}	—	9, 19, 30, 45, 55, 66, 81, 91, 102, 117, 127, 138	—	Grand pin
N.C.	—	97, 108, 112, 115, 116, 123 (17*)	—	These pins shall be used as an open pin. No. 17 is also an open pin for MB86942.

* : No.17 is a READY2# pin for MB86941.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating						Unit
		MB86941				MB86942		
Power supply voltage	V_{DD}	–0.5 to +0.6*1				–0.5 to +4.0*1		V
Input voltage	V_I	–0.5 to V_{DD} + 0.5*1						V
Output voltage	V_O	–0.3 to V_{DD} + 0.5*1				–0.5 to V_{DD} + 0.5*1		V
Storage temperature	T_{STG}	–40 to 125						°C
Output current*2	I_O	At maximum V_{DD}	*3	V_O = V_{DD}	+40	V_O = V_{DD}	+60	mA
				V_O = 0	–40			
			*4	V_O = V_{DD}	+80			
				V_O = 0	–40	V_O = 0	–60	
			*5	V_O = V_{DD}	+120			
				V_O = 0	–80			

*1: V_{SS} = 0 V
*2: At 1 pin for 1 second
*3: Output pins other than D < 15 : 0 >, READY1# and REDY2#
*4: D < 15 : 0 >
*5: READY1#, READY2#

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value		Unit
		MB86941	MB86942	
Power supply voltage	V_{DD}	4.75 to 5.25	3.15 to 3.45	V
Operating temperature	T_A	0 to +70		°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.
No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRIC CHARACTERISTICS

1. DC Characteristics

(1) Input Characteristics

(MB86941: V_{DD} = 5 V ± 5%, T_A = 0 to +70°C)
(MB86942: V_{DD} = 3.3 V ± 0.15 V, T_A = 0 to +70°C)

Parameter	Symbol	Condition	MB86941		MB86942		Unit
			Min.	Max.	Min.	Max.	
"H" level input voltage	V_{IH}	CLOCK	2.8	V_{DD}	$V_{DD} \times 0.65$	$V_{DD} + 0.15$	V
		IRQ15 to IRQ1	2.4	V_{DD}			
		Other	2.2	V_{DD}			
"L" level input voltage	V_{IL}	IRQ15 to IRQ1	V_{SS}	0.6	V_{SS}	$V_{DD} \times 0.25$	V
		Other	V_{SS}	0.8			

(2) Output Characteristics

(MB86941: V_{DD} = 5 V ± 5%, T_A = 0 to +70°C)
(MB86942: V_{DD} = 3.3 V ± 0.15 V, T_A = 0 to +70°C)

Parameter	Symbol	Condition	MB86941		MB86942		Unit
			Min.	Max.	Min.	Max.	
"H" level output voltage	V_{OH}	I_{OH} = –8 mA*2	4.0	V_{DD}	—	—	V
		I_{OH} = –3.2 mA*3					
		I_{OH} = –4 mA*4	—	—	$V_{DD} - 0.5$	V_{DD}	
"L" level output voltage	V_{OL}	I_{OL} = +12 mA*1	V_{SS}	0.4	—	—	V
		I_{OL} = +8 mA*2					
		I_{OL} = +3.2 mA*3					
		I_{OL} = +4 mA*4	—	—	V_{SS}	0.4	

*1: MB86941 READY1#, READY2#
*2: MB86941 D < 15 : 0 >
*3: MB86941 Other than READY1#, READY2# and D < 15 : 0 >
*4: MB86942

(3) Power Supply Current

(MB86941: V_{DD} = 5 V ± 5%, T_A = 0 to +70°C)
(MB86942: V_{DD} = 3.3 V ± 0.15 V, T_A = 0 to +70°C)

Parameter	Symbol	Condition	MB86941		MB86942		Unit
			Min.	Max.	Min.	Max.	
Power supply current	I_{CC}	—	—	230	—	190	mA

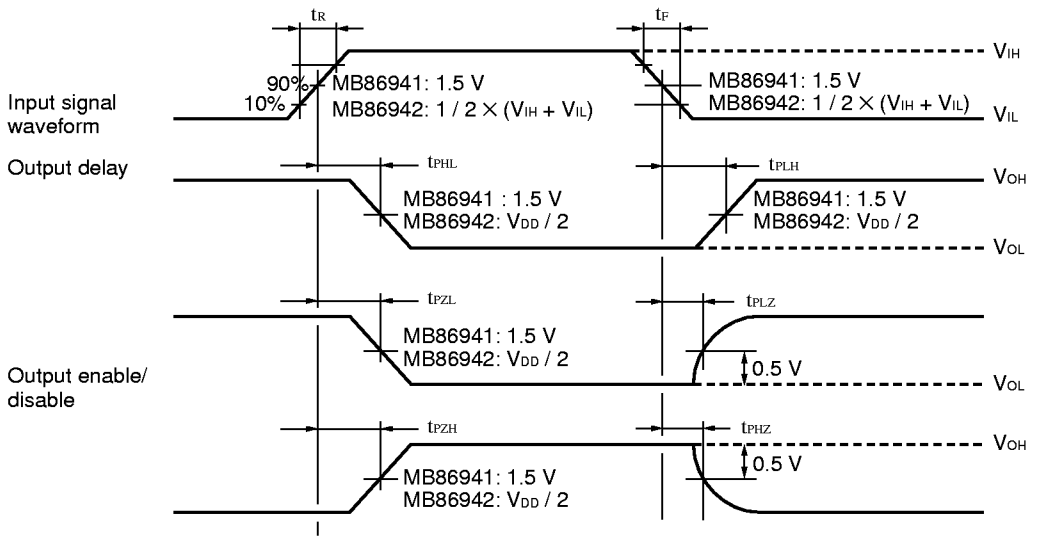
2. Capacitances

(V_{DD} = V_I = 0 V, f = 1 MHz, T_A = +25°C)

Parameter	Symbol	Value		Unit
		Min.	Max.	
Input Capacitance	C_{IN}	—	16	pF
Output Capacitance	C_{OUT}	—	16	pF
I/O Capacitance	$C_{I/O}$	—	16	pF

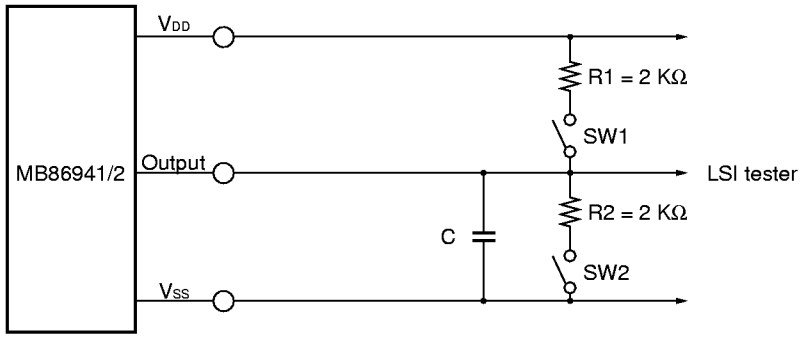
3. AC Test Conditions

(1) Input/Output Signal Waveform



t_R, t_F < 5 ns
MB86941: V_{IH} = CLOCK 2.8V, IRQ15 to IRQ1 2.4 V, Other 2.2 V, V_{IL} = 0.4 V
MB86942: V_{IH} = V_{DD} × 0.65, V_{IL} = V_{DD} × 0.25

(2) Load Circuit



Condition	Load capacitance	
	MB86941	MB86942
Normal output	60 pF	30 pF
Tri-state output (READY1#, READY2#)	65 pF	—
Bi-directional pin (D bus)	85 pF	30 pF

Signal transmit	SW1	SW2
L→H, H→L	OFF	OFF
L→Z, Z→L	ON	OFF
L→Z, Z→L	OFF	ON

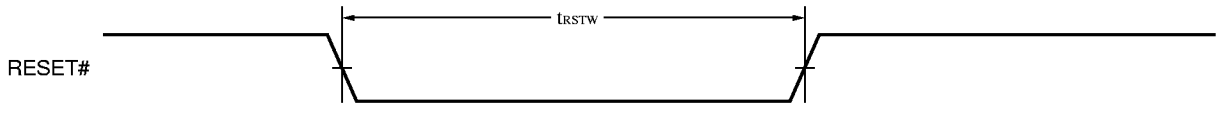
4. AC Characteristics

(1) Reset signal (Hardware reset)

(MB86941: V_{DD} = 5 V ± 5%, T_A = 0 to +70°C)
(MB86942: V_{DD} = 3.3 V ± 0.15 V, T_A = 0 to +70°C)

Parameter	Symbol	Value		Unit
		Min.	Max.	
Reset pulse width	t_{RSTW}	20	—	t_{CLK}

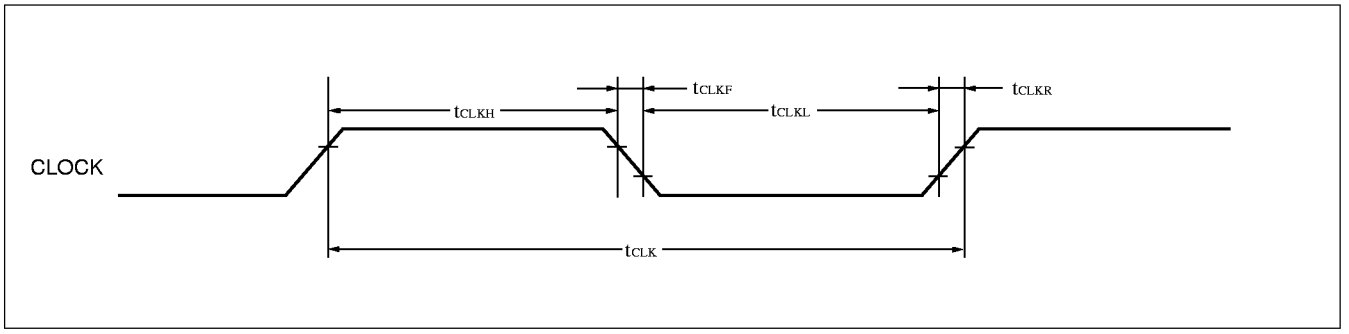
t_{CLK}: See “(2) Clock Signals.”



(2) Clock signal (CLOCK)

(MB86941: V_{DD} = 5 V ± 5%, T_A = 0 to +70°C)
(MB86942: V_{DD} = 3.3 V ± 0.15 V, T_A = 0 to +70°C)

Parameter	Symbol	MB86941		MB86942		Unit
		Min.	Max.	Min.	Max.	
Clock cycle time	t_{CLK}	25	—	20	—	ns
Clock "H" pulse width	t_{CLKH}	9	—	8	—	ns
Clock "L" pulse width	t_{CLKL}	9	—	8	—	ns
Clock rise time	t_{CLKR}	—	4	—	2	ns
Clock fall time	t_{CLKF}	—	4	—	2	ns



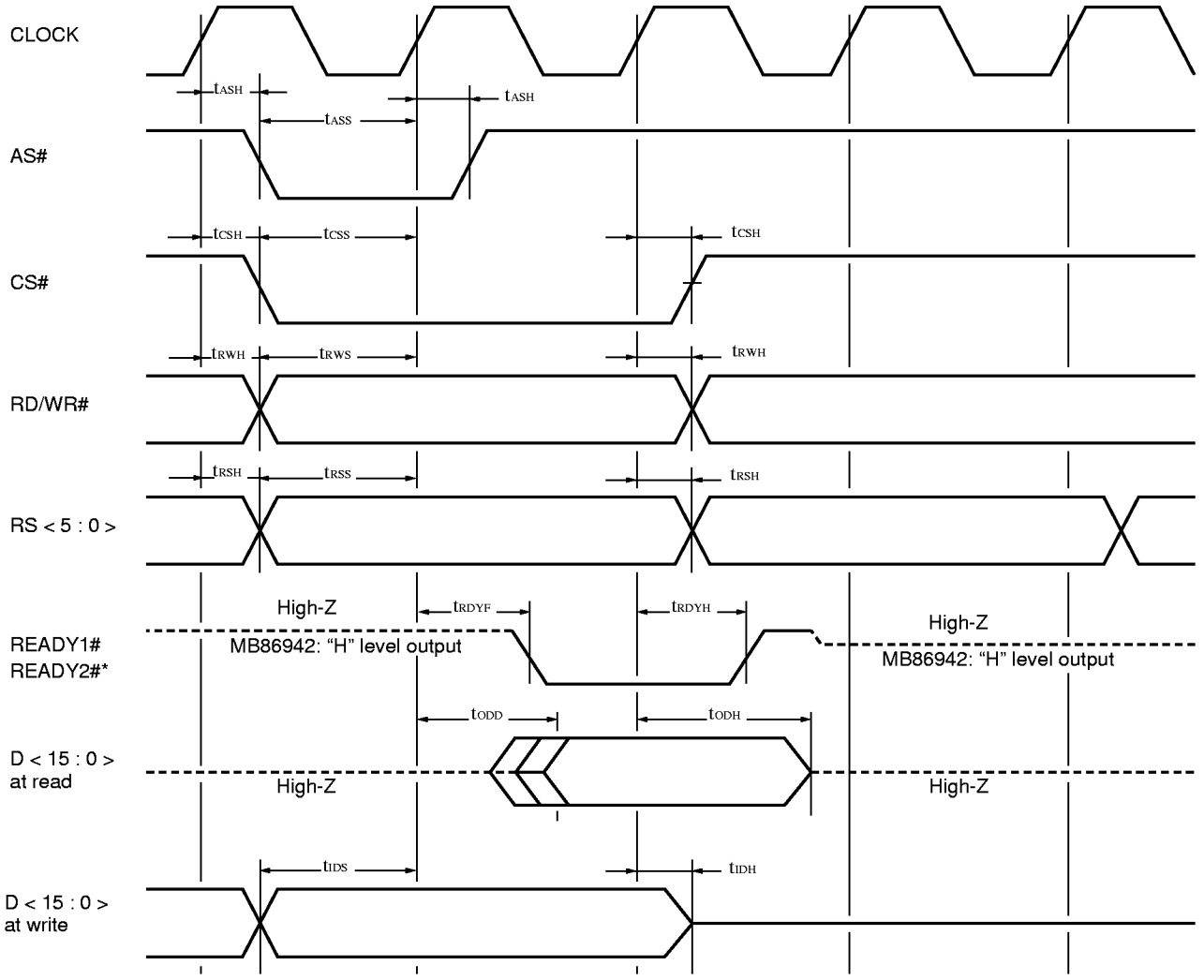
(3) MPU interface (Register read/write)

(MB86941: V_{DD} = 5 V ± 5%, T_A = 0 to +70°C)
(MB86942: V_{DD} = 3.3 V ± 0.15 V, T_A = 0 to +70°C)

Parameter	Symbol	MB86941				MB86942		Unit
		WSEL = "H"		WSEL = "L"				
		Min.	Max.	Min.	Max.	Min.	Max.	
AS# setup time	t_{ASS}	11	—	7	—	7	—	ns
AS# hold time	t_{ASH}	0	—	0	—	2	—	ns
CS# setup time	t_{CSS}	8	—	5	—	7	—	ns
CS# hold time	t_{CSH}	0	—	0	—	2	—	ns
RD/WR# setup time	t_{RWS}	13	—	9	—	7	—	ns
RD/WR# hold time	t_{RWH}	0	—	0	—	2	—	ns
RS < 5 : 0 > setup time	t_{RSS}	8	—	5	—	7	—	ns
RS < 5 : 0 > hold time	t_{RSH}	0	—	0	—	2	—	ns
READY1#, READY2# output delay time	t_{RDYF}	0	18	0	18	0	18	ns
READY1#, READY2# hold time	t_{RDYH}	5	20	5	20	5	20	ns
D < 15 : 0 > Output delay time at reading	t_{ODD}	0	21	0	23	0	23	ns
D < 15 : 0 > Output hold time at reading	t_{ODH}	5	25	5	25	5	20	ns
D < 15 : 0 > Input setup time at writing	t_{IDS}	11	—	7	—	7	—	ns
D < 15 : 0 > Input hold time at writing	t_{IDH}	0	—	0	—	0	—	ns

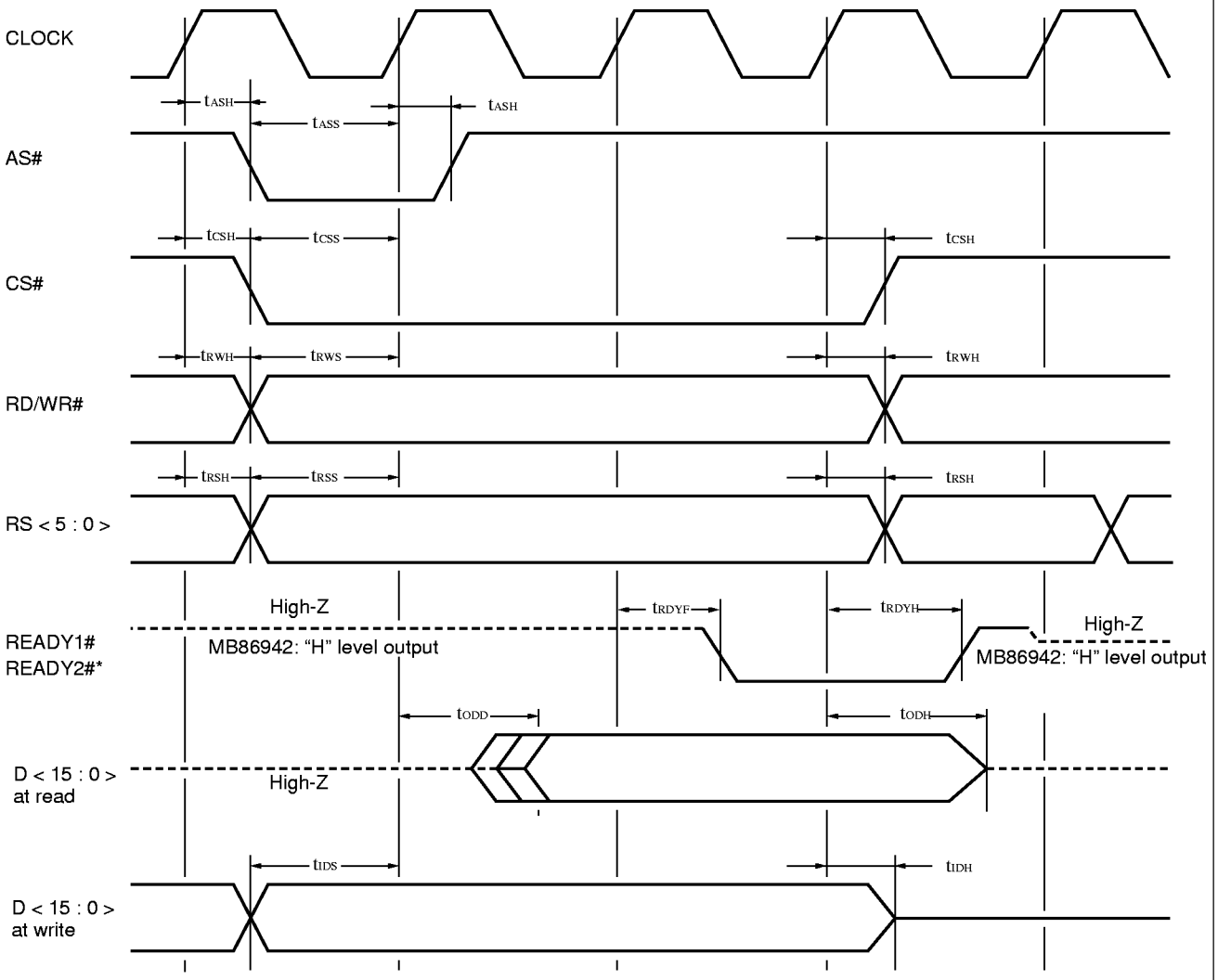
* : READY2# is available for MB86941.

• WSEL = “H”



* : Only for MB86941.

• WSEL = “L”



* : Only for MB86941.

(4) Interrupt signal

• Interrupt input pulse width

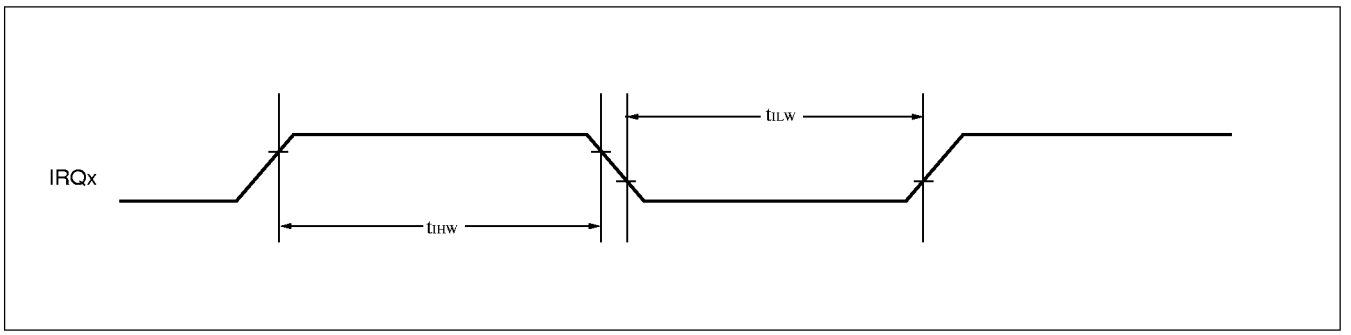
(MB86941: V_{DD} = 5 V ± 5%, T_A = 0 to +70°C)
(MB86942: V_{DD} = 3.3 V ± 0.15 V, T_A = 0 to +70°C)

Parameter	Symbol	Value		Unit
		Min.	Max.	
IRQ input "H" level pulse width*1	t_{IHW}	6 t_{CLK} + 10	—	ns
IRQ input "L" level pulse width*2	t_{ILW}	6 t_{CLK} + 10	—	ns

t_{CLK}: See "(2) Clock Signals."

*1: When the trigger mode is set for "H" level signal input or RISE-EDGE, a pulse of at least this width is received as a REQ-FF signal. Note that this rule does not guarantee that no interrupts less than this width will be received.

*2: When the trigger mode is set for "L" level signal input or FALL-EDGE, a pulse of at least this width is received as a REQ-FF signal. Note that this rule does not guarantee that no interrupts less than this width will be received.



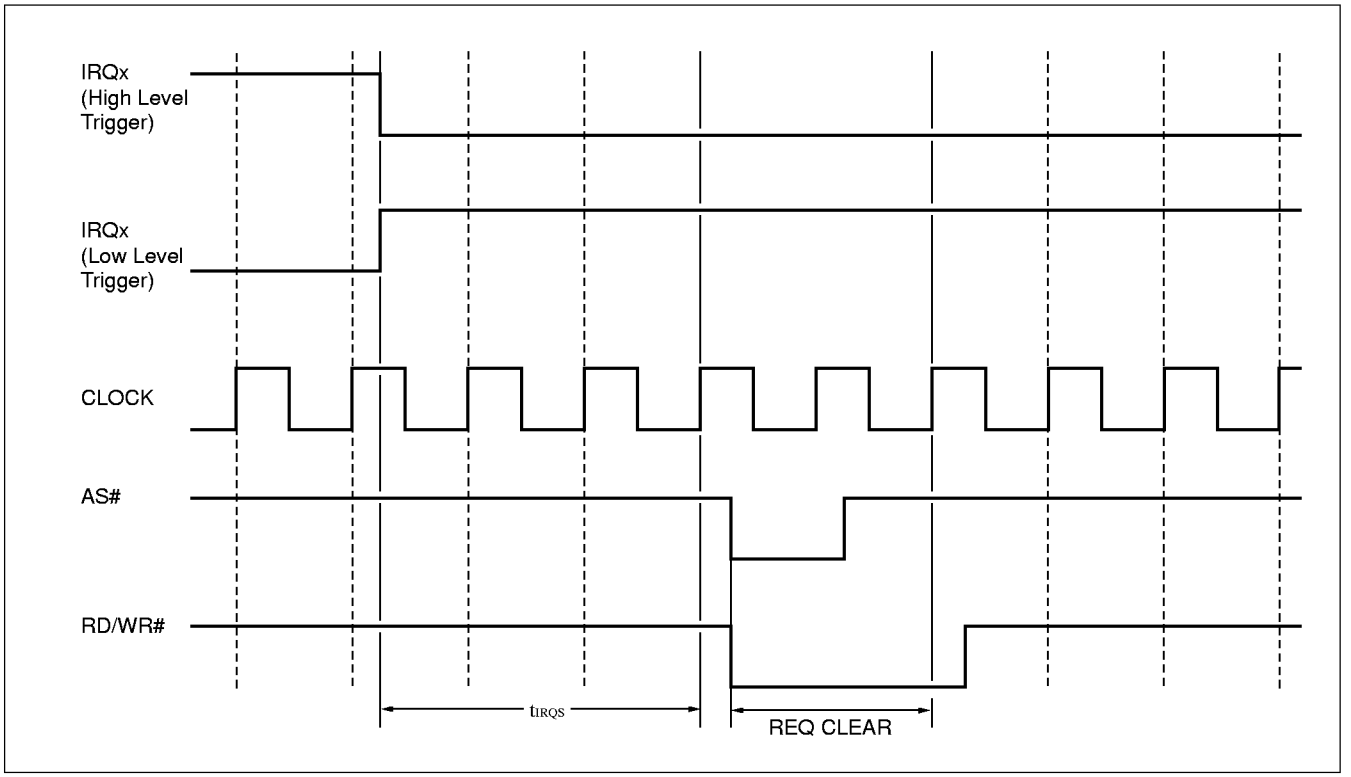
- Interrupt input clear

(MB86941: V_{DD} = 5 V ± 5%, T_A = 0 to +70°C)
(MB86942: V_{DD} = 3.3 V ± 0.15 V, T_A = 0 to +70°C)

Parameter	Symbol	Value		Unit
		Min.	Max.	
IRQx clear setup time*	t_{IRQS}	2 t_{CLK} + 10	—	ns

t_{CLK}: See "(2) Clock Signals."

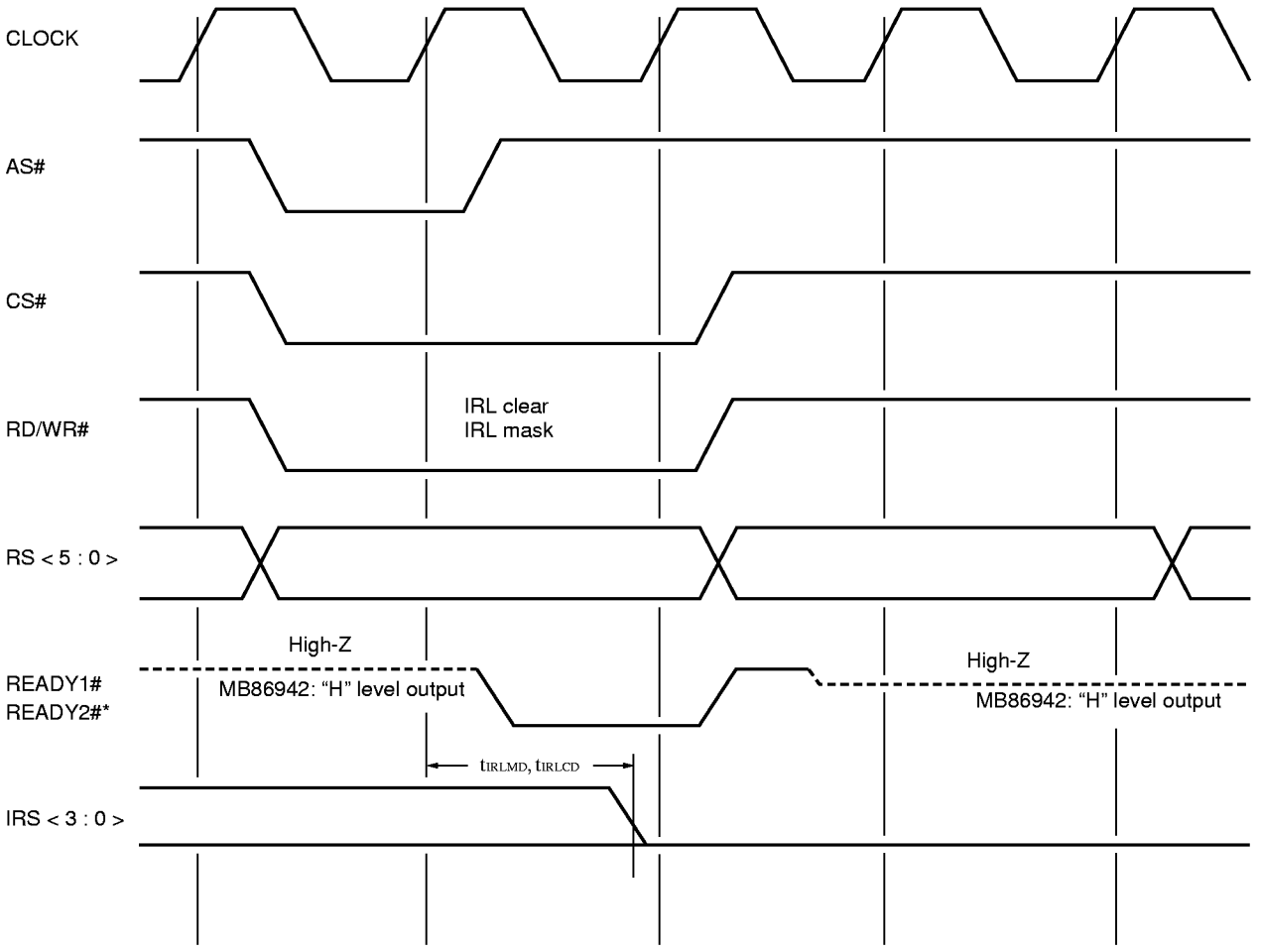
* : This parameter means the condition of REQUEST CLEAR execution and is applied at level trigger modes.



• Interrupt level output

(MB86941: V_{DD} = 5 V ± 5%, T_A = 0 to +70°C)
(MB86942: V_{DD} = 3.3 V ± 0.15 V, T_A = 0 to +70°C)

Parameter	Symbol	Value		Unit
		Min.	Max.	
IRL < 3 : 0 > clear delay time	t_{IRLCD}	—	80	ns
IRL < 3 : 0 > mask delay time	t_{IRLMD}	—	80	ns



* : Only for MB86941.

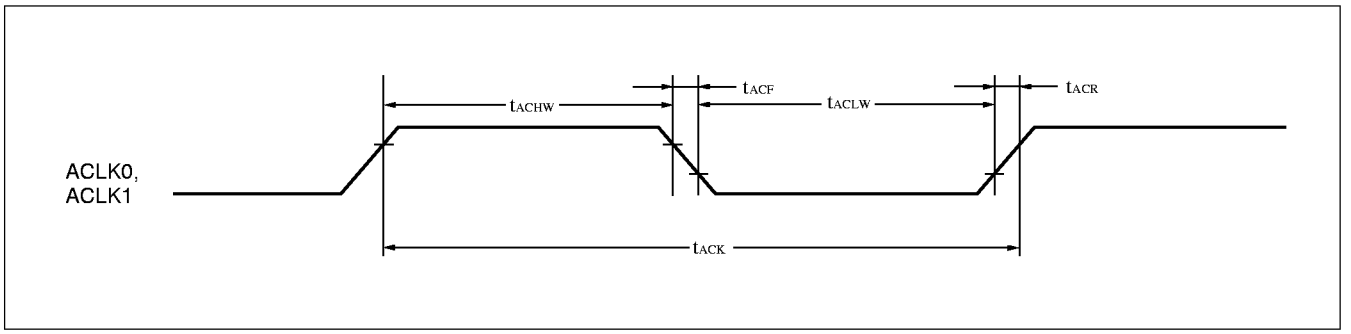
(5) Prescaler timer

• Prescaler input

(MB86941: V_{DD} = 5 V ± 5%, T_A = 0 to +70°C)
(MB86942: V_{DD} = 3.3 V ± 0.15 V, T_A = 0 to +70°C)

Parameter	Symbol	MB86941		MB86942		Unit
		Min.	Max.	Min.	Max.	
Prescaler input clock cycle time*	t_{ACK}	50	—	40	—	ns
Prescaler input clock "H" level width*	t_{ACHW}	22	—	15	—	ns
Prescaler input clock "L" level width*	t_{ACLW}	22	—	15	—	ns
Prescaler input clock rise time*	t_{ACR}	—	5	—	5	ns
Prescaler input clock fall time*	t_{ACF}	—	5	—	5	ns

* : Applied in prescaler external clock mode. When the prescaler output is used as a timer signal, the timer input clock requirements must be met.

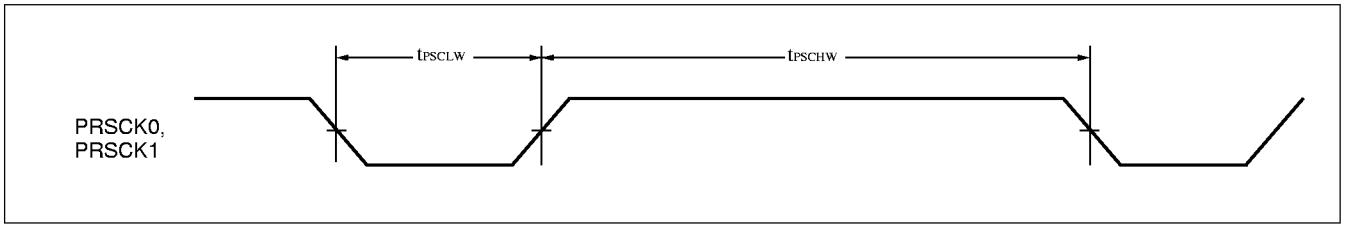


• Prescaler output

(MB86941: V_{DD} = 5 V ± 5%, T_A = 0 to +70°C)
(MB86942: V_{DD} = 3.3 V ± 0.15 V, T_A = 0 to +70°C)

Parameter	Symbol	Standard Value	Unit
Prescaler output "L" level width*1, *3	t_{PSCLW}	1	t_{PCK}*4
Prescaler output "H" level width*1, *3	t_{PSCHW}	N – 1	t_{PCK}*4
Prescaler output "L" level width*2, *3	t_{PSCLW}	$N \cdot 2^{M-1}$	t_{PCK}*4
Prescaler output "H" level width*2, *3	t_{PSCHW}	$N \cdot 2^{M-1}$	t_{PCK}*4

*1: Applied when the prescaler register SELECT field is set to "0."
N: Value set in the prescaler register PRESCALE VALUE field
*2: Applied when the prescaler register SELECT field is set to any value other than "0."
M: Value set in the prescaler register SELECT field.
N: Value set in the prescaler register PRESCALE VALUE field.
*3: When the prescaler register SELECT field is set to "0," the PRSCKx output is fixed at "L" level.
*4: t_{PCK} has the following prescaler input clock period.
Internal clock mode: $t_{PCK} = 2 \cdot t_{CLK}$ (For t_{CLK}, see "(2) Clock Signals")
External clock mode: $t_{PCK} = t_{ACK}$ (For t_{ACK}, see "(5) Prescaler Timer Unit/Prescaler Input")

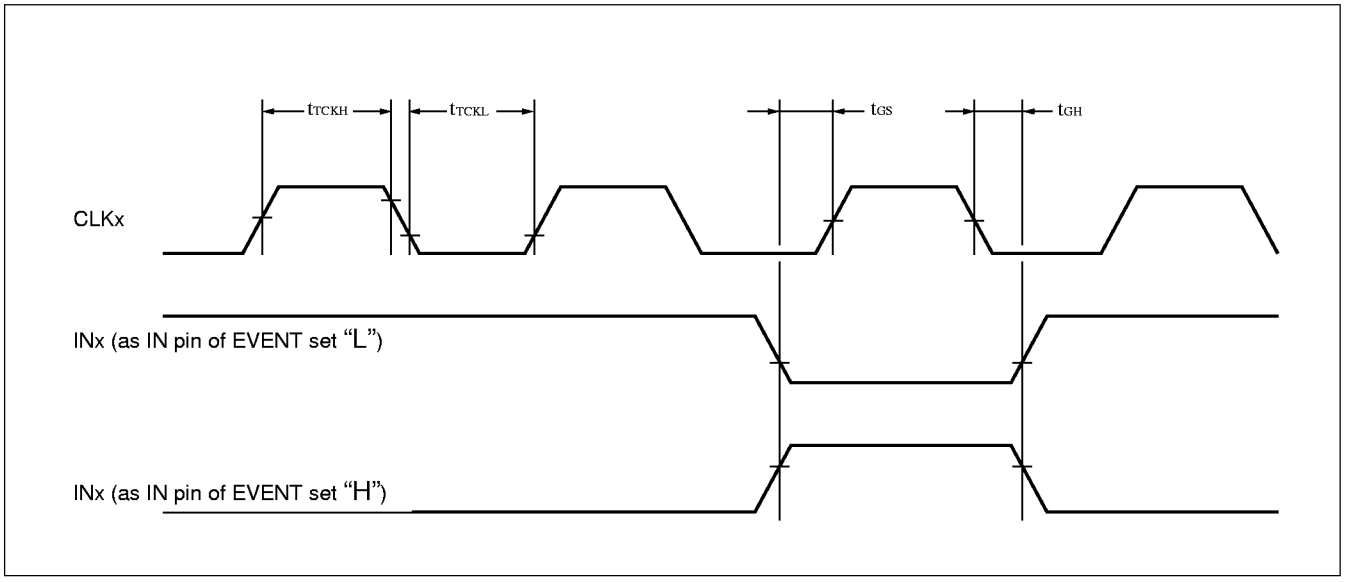


• Timer (at external clock mode)

(MB86941: V_{DD} = 5 V ± 5%, T_A = 0 to +70°C)
(MB86942: V_{DD} = 3.3 V ± 0.15 V, T_A = 0 to +70°C)

Parameter	Symbol	Value		Unit
		Min.	Max.	
Timer input clock "H" level width	t_{TCKH}	3	—	t_{CLK}
Timer input clock "L" level width	t_{TCKL}	3	—	t_{CLK}
GATE signal (IN pin) setup time (for CLKx)	t_{GS}	10	—	ns
GATE signal (IN pin) hold time (for CLKx)	t_{GH}	0	—	ns

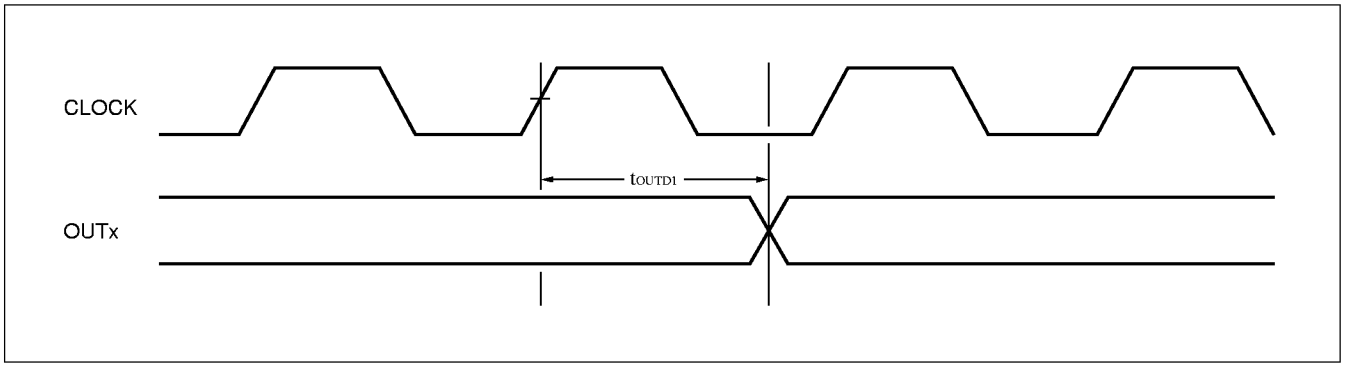
t_{CLK}: See "(2) Clock Signals".



• Timer output 1

(MB86941: V_{DD} = 5 V ± 5%, T_A = 0 to +70°C)
(MB86942: V_{DD} = 3.3 V ± 0.15 V, T_A = 0 to +70°C)

Parameter	Symbol	Value		Unit
		Min.	Max.	
OUT output delay time (for CLOCK)	t_{OUTD1}	—	30	ns



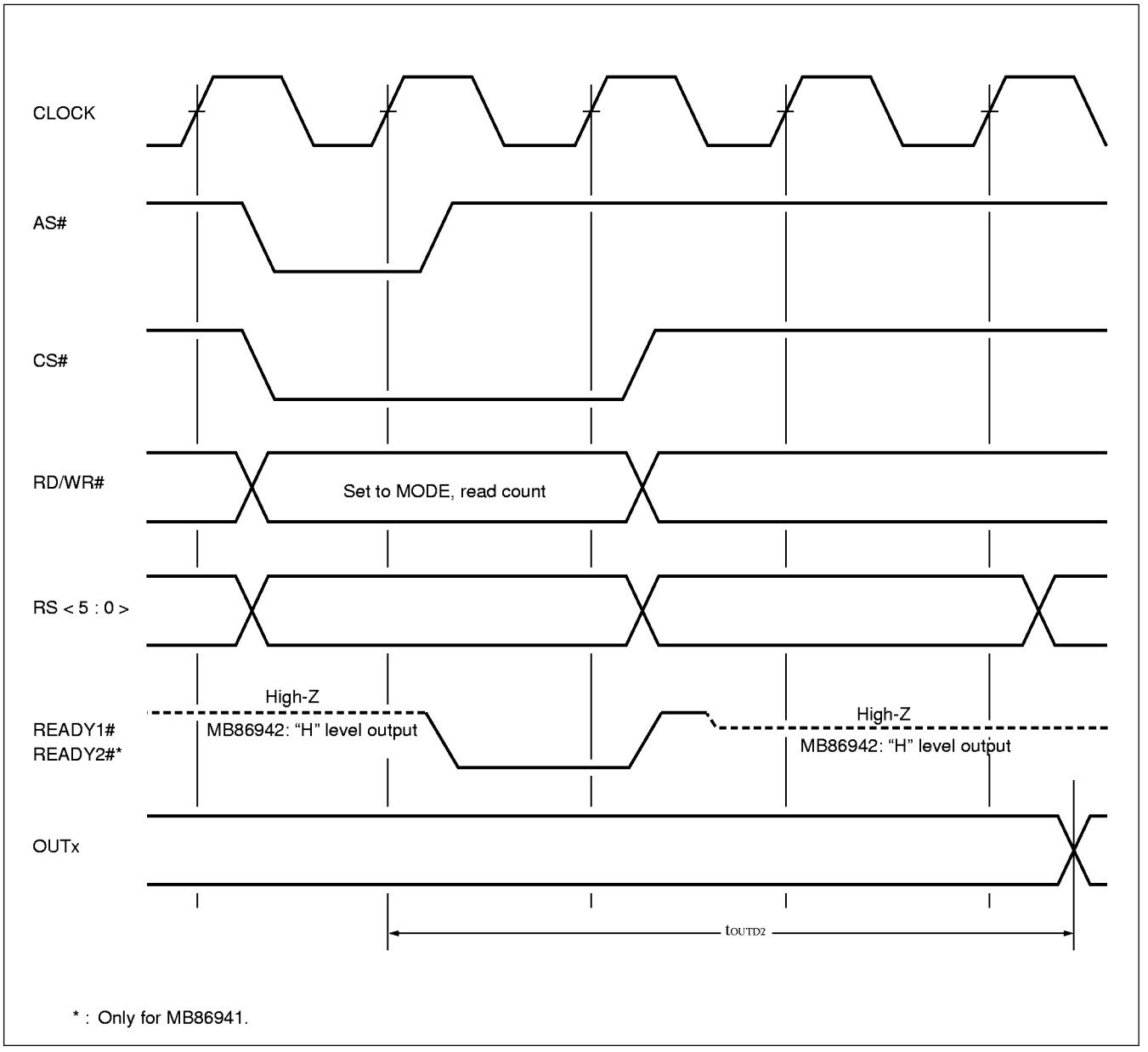
- Timer output 2

(MB86941: V_{DD} = 5 V ± 5%, T_A = 0 to +70°C)
(MB86942: V_{DD} = 3.3 V ± 0.15 V, T_A = 0 to +70°C)

Parameter	Symbol	Value		Unit
		Min.	Max.	
OUT output delay time*	t_{OUTD2}	—	3 t_{CLK} + 30	ns

t_{CLK}: See "(2) Clock Signals".

* : Applied to the following cases.
- Setting mode (write to TCR).
- After setting to MODE0, write to RELOAD register/read COUNT register.
- After setting to MODE1, write to RELOAD register/read COUNT register.
- After setting to MODE3, write to RELOAD register.



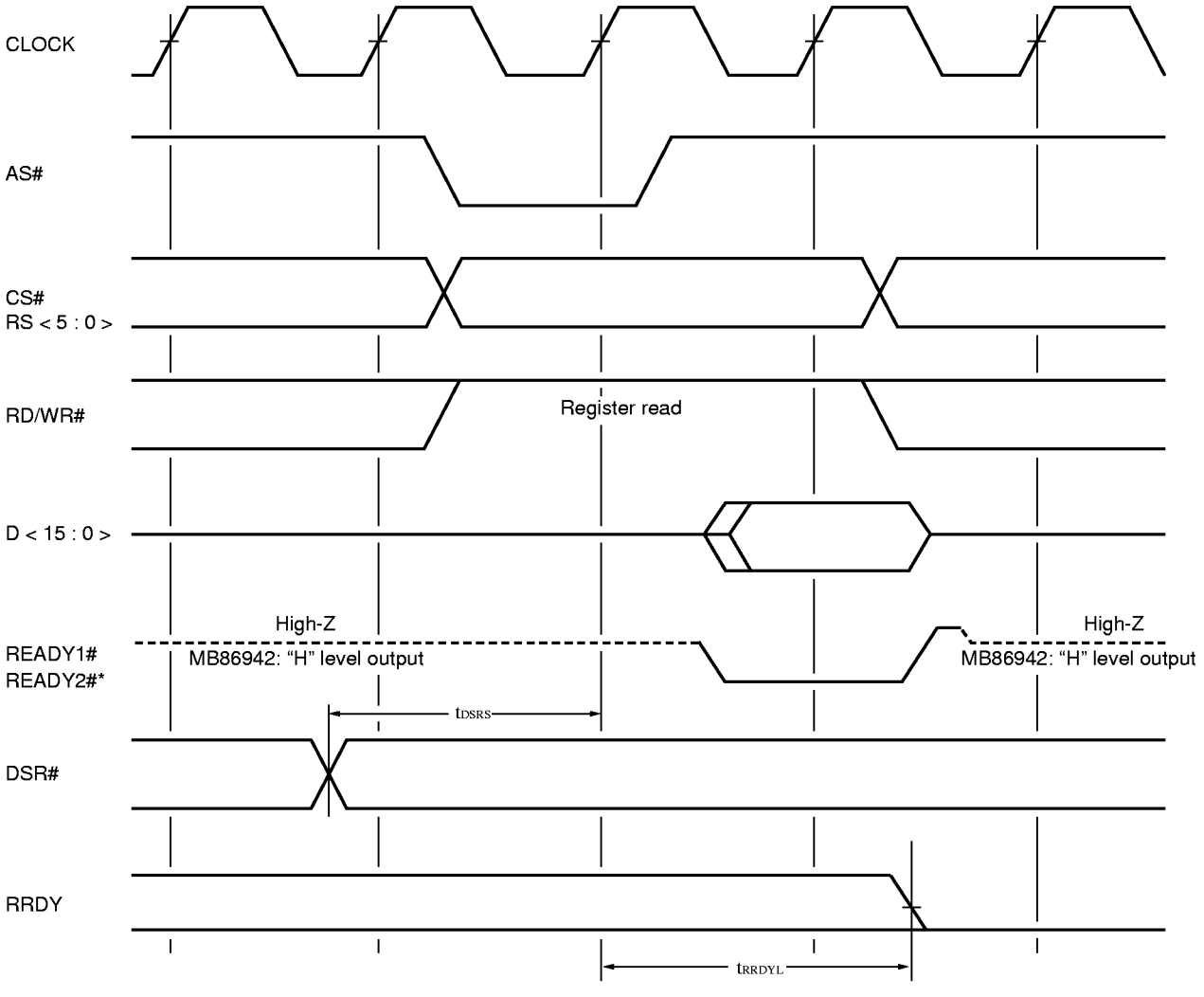
(6) SDTR

• DSR#, RRDY

(MB86941: V_{DD} = 5 V ± 5%, T_A = 0 to +70°C)
(MB86942: V_{DD} = 3.3 V ± 0.15 V, T_A = 0 to +70°C)

Parameter	Symbol	Value		Unit
		Min.	Max.	
DSR# setup time for resistor read	t_{DSRS}	28	—	t_{CLK}
Interval from register read to RRDY off	t_{RRDYL}	0	100	ns

t_{CLK}: See “(2) Clock Signals”.



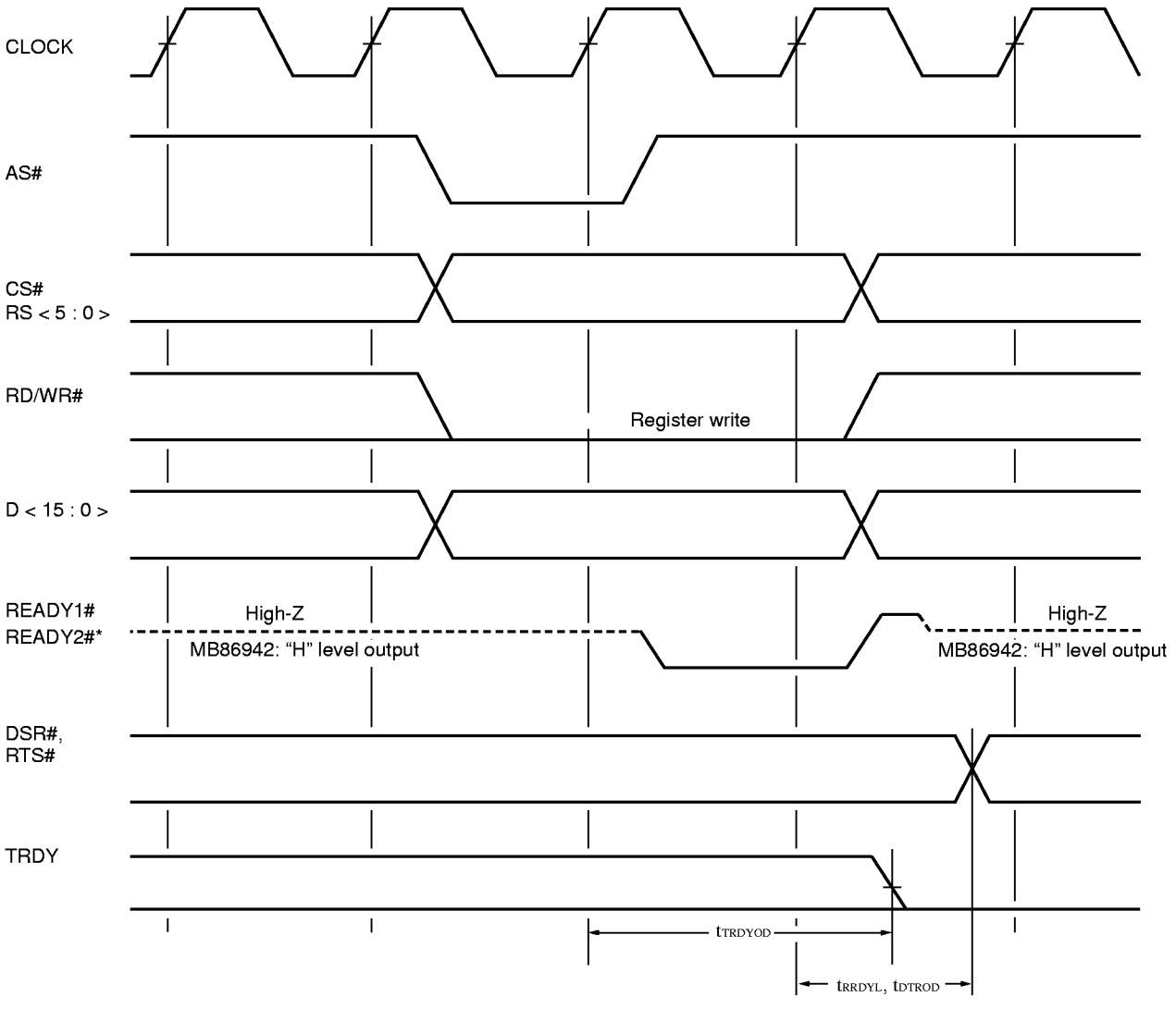
* : Only for MB86941.

• DTR#, RTS#, TRDY

(MB86941: V_{DD} = 5 V ± 5%, T_A = 0 to +70°C)
(MB86942: V_{DD} = 3.3 V ± 0.15 V, T_A = 0 to +70°C)

Parameter	Symbol	Value		Unit
		Min.	Max.	
Delay time from register write to DTR# output	t_{DTROD}	0	40	t_{CLK}
Delay time from register write to RTS# output	t_{RTSOD}	0	40	t_{CLK}
Delay time from register write to TRDY output	t_{TRDYOD}	0	100	ns

t_{CLK}: See “(2) Clock Signals”.



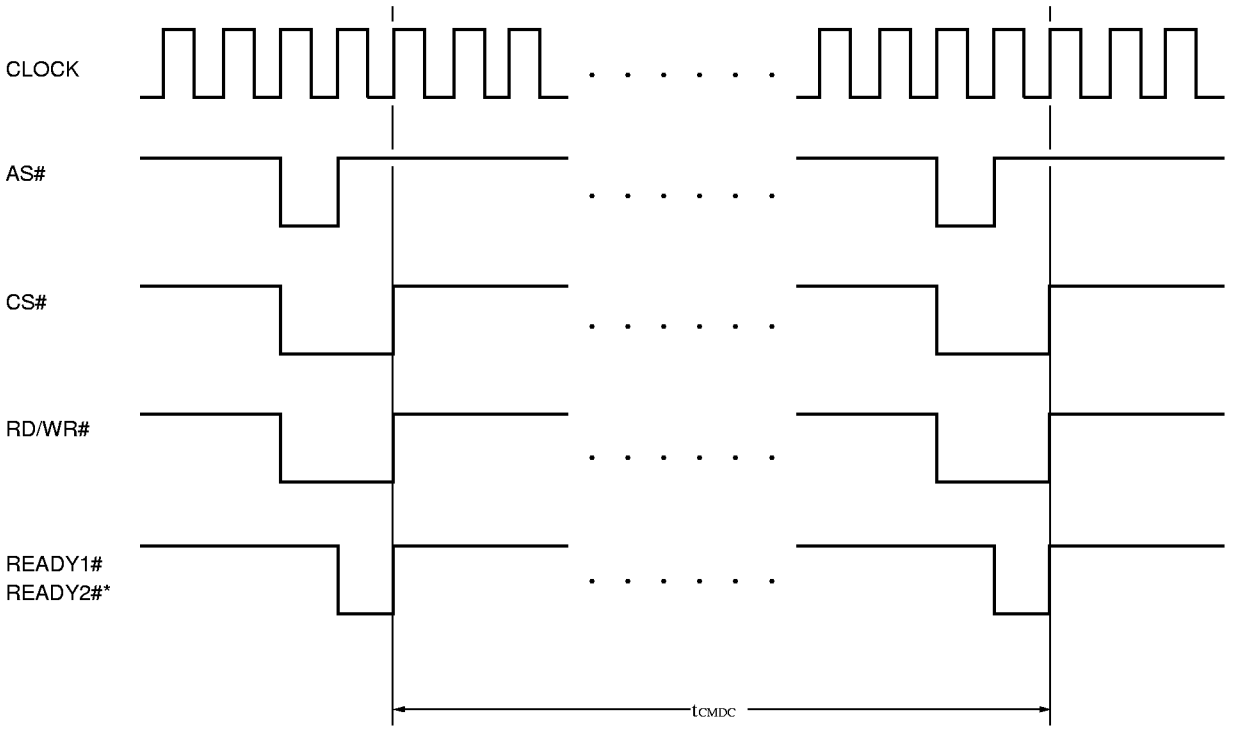
* : Only for MB86941.

• Command write cycle

(MB86941: V_{DD} = 5 V ± 5%, T_A = 0 to +70°C)
(MB86942: V_{DD} = 3.3 V ± 0.15 V, T_A = 0 to +70°C)

Parameter	Symbol	Value		Unit
		Min.	Max.	
Command write cycle time (for initial value setup)	t_{CMDC}	14	—	t_{CLK}
Command write cycle time (for asynchronous mode)	t_{CMDC}	20	—	t_{CLK}
Command write cycle time (for synchronous mode)	t_{CMDC}	40	—	t_{CLK}

t_{CLK}: See “(2) Clock Signals”.



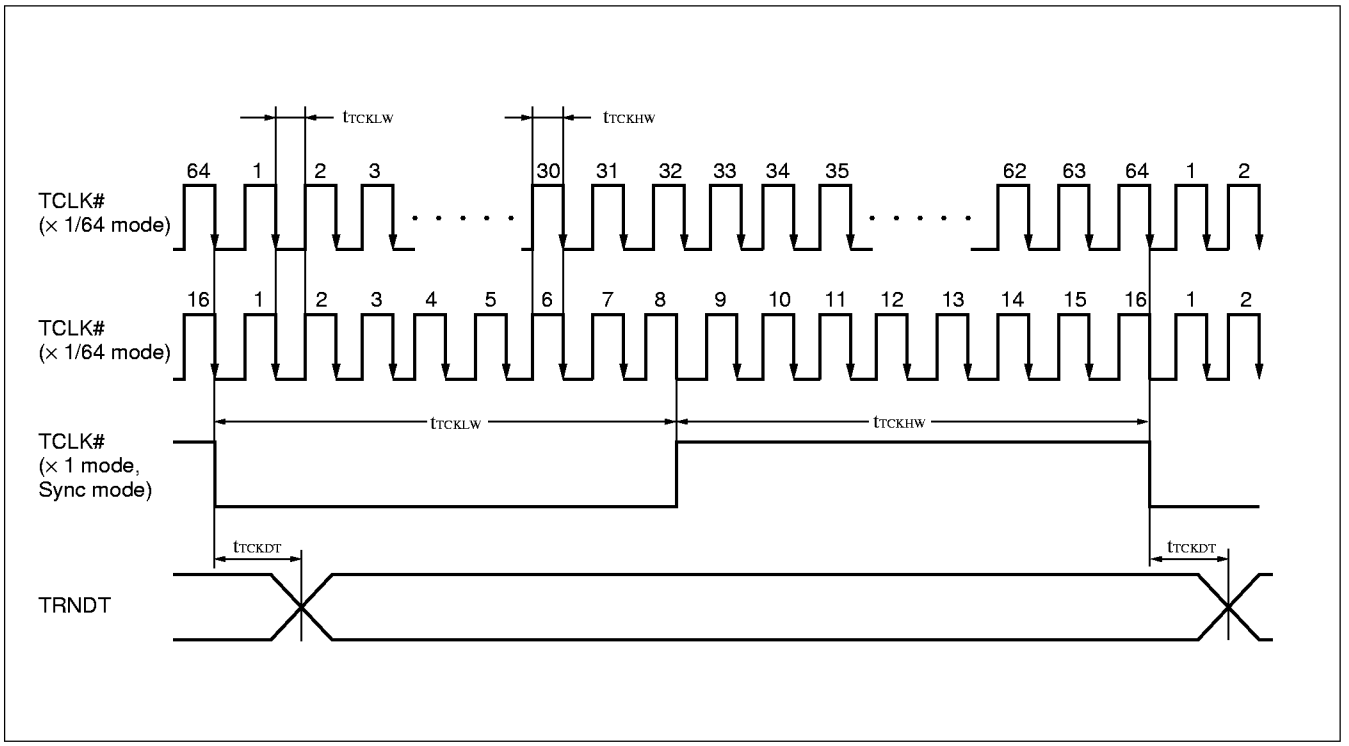
* : Only for MB86941.

• Transmit Clock and Transmit Data

(MB86941: V_{DD} = 5 V ± 5%, T_A = 0 to +70°C)
(MB86942: V_{DD} = 3.3 V ± 0.15 V, T_A = 0 to +70°C)

Parameter	Symbol	Syncroh mode, × 1 mode		×1/16, ×1/64 mode		Unit
		Min.	Max.	Min.	Max.	
Transmit Clock "H" width	t_{TCKHW}	32	—	4	—	t_{CLK}
Transmit Clock "L" width	t_{TCKLW}	14	—	4	—	t_{CLK}
Interval from transmit clock falling to transmit data output	t_{TCKDT}	0	100	0	100	ns

t_{CLK}: See "(2) Clock Signals".

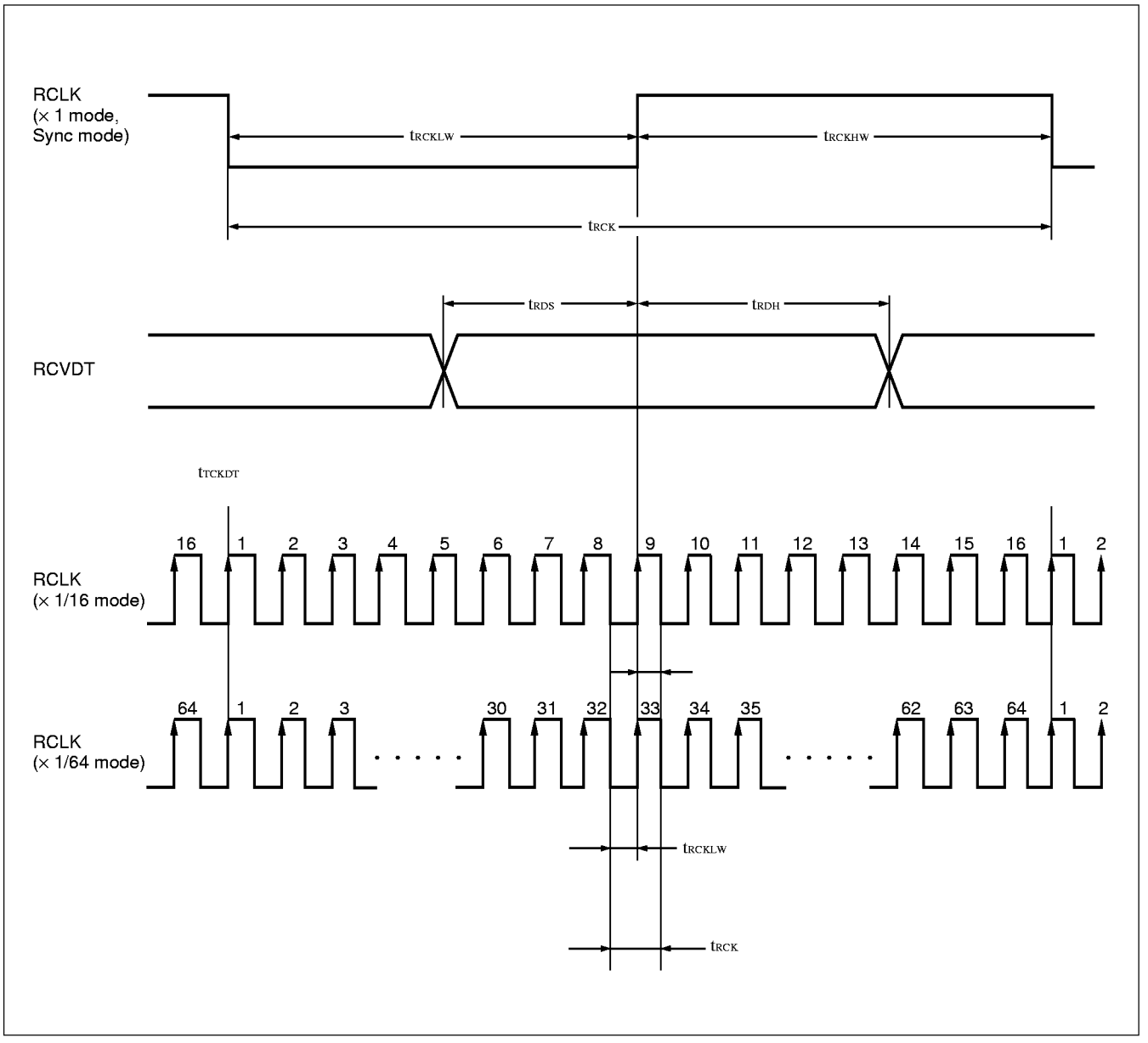


• Receive Clock and Receive Data

(MB86941: V_{DD} = 5 V ± 5%, T_A = 0 to +70°C)
(MB86942: V_{DD} = 3.3 V ± 0.15 V, T_A = 0 to +70°C)

Parameter	Symbol	Syncroh mode, × 1 mode		×1/16, ×1/64 mode		Unit
		Min.	Max.	Min.	Max.	
Receive clock period	t_{RCK}	62	—	8	—	t_{CLK}
Receive clock "H" width	t_{RCKHW}	12	—	4	—	t_{CLK}
Receive clock "L" width	t_{RCKLW}	7	—	4	—	t_{CLK}
Receive data setup time	t_{RDS}	6	—	6	—	t_{CLK}
Receive data hold time	t_{RDH}	6	—	6	—	t_{CLK}

t_{CLK}: See "(2) Clock Signals".

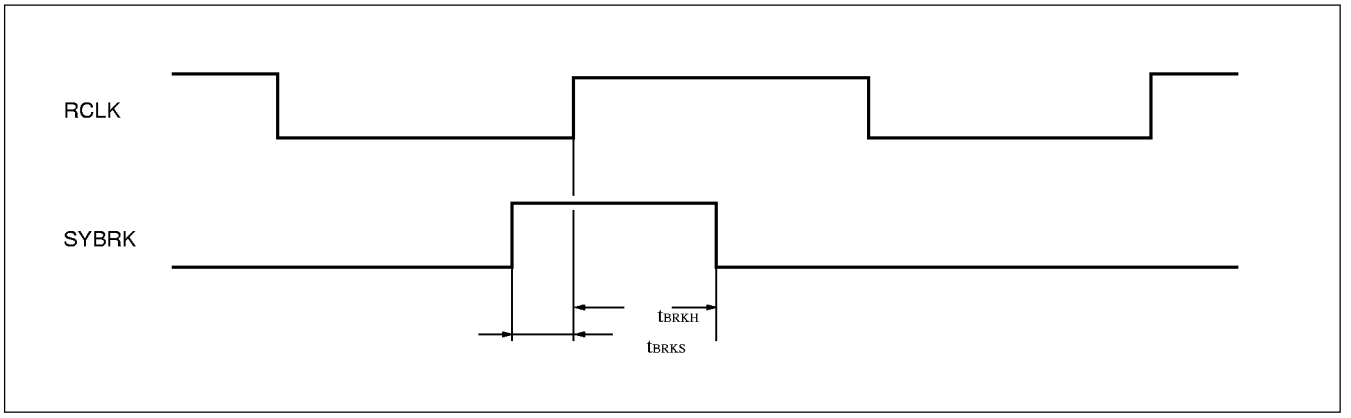


• SYBRK Signal Timing for External Synchronous mode

(MB86941: V_{DD} = 5 V ± 5%, T_A = 0 to +70°C)
(MB86942: V_{DD} = 3.3 V ± 0.15 V, T_A = 0 to +70°C)

Parameter	Symbol	Value		Unit
		Min.	Max.	
SYBRK setup time (for RCLK)	t_{BRKS}	0	—	t_{CLK}
SYBRK hold time (for RCLK)	t_{BRKH}	10	—	t_{CLK}

t_{CLK}: See “(2) Clock Signals”.



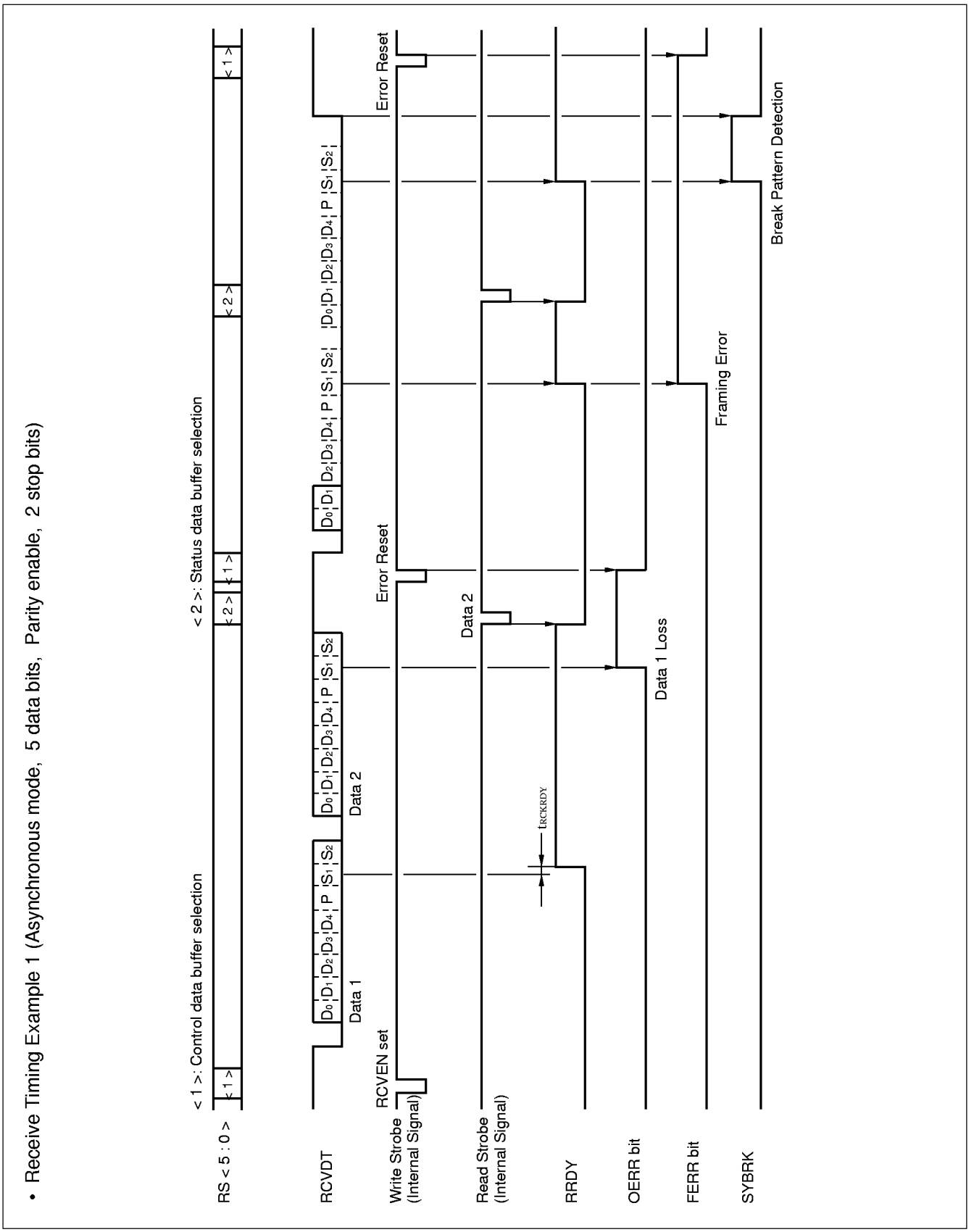
• Transmit and Receive Control Signal Timing

(MB86941: V_{DD} = 5 V ± 5%, T_A = 0 to +70°C)
(MB86942: V_{DD} = 3.3 V ± 0.15 V, T_A = 0 to +70°C)

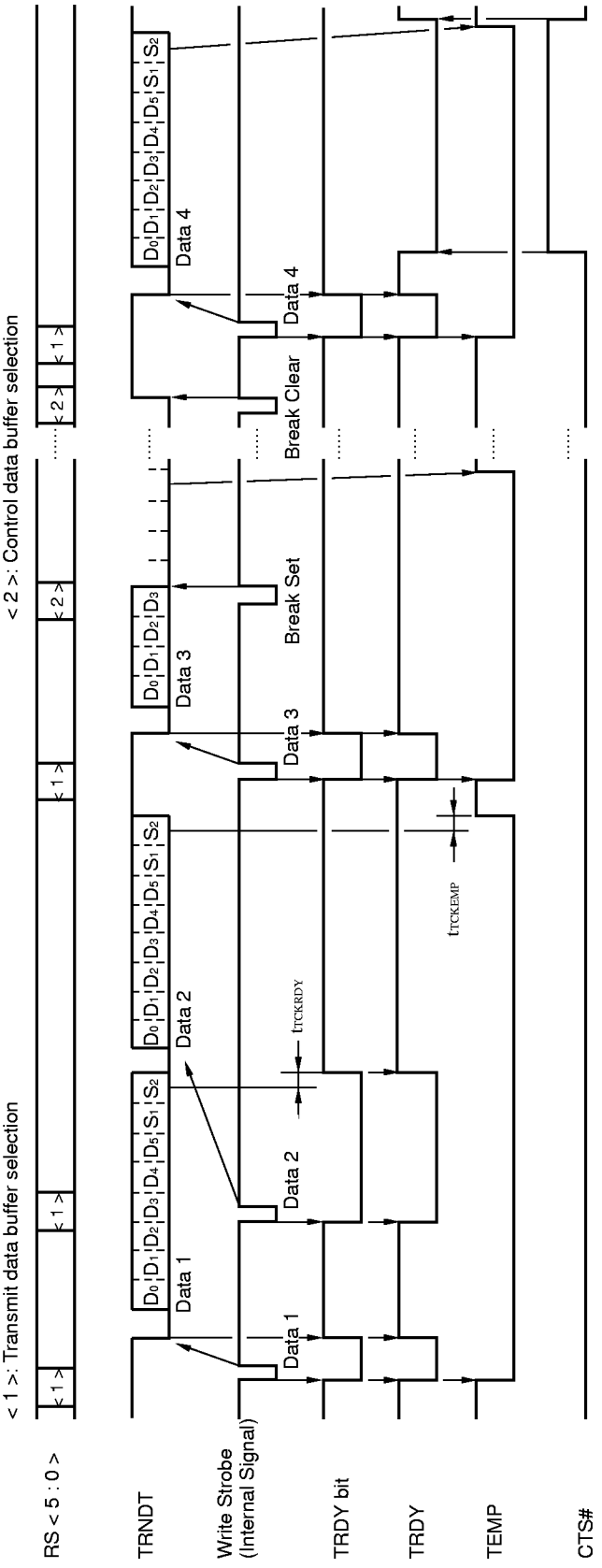
Parameter	Symbol	Value		Unit
		Min.	Max.	
Delay time from TCLK# rising (last bit) to TRDY rising	t_{TCKRDY}	—	36	t_{CLK}
Delay time from TCLK# rising (last bit) to TEMP rising	t_{TCKEMP}	—	24	t_{CLK}
Delay time from RCLK rising (last bit) to RRDY rising	t_{RCKRDY}	—	35	t_{CLK}
Detection time from RCLK rising (last bit) to internal SYNC (SYBRK pin)	t_{SYCD1}	—	62	t_{CLK}
Detection time RCLK rising (last bit) to internal SYNC (status data buffer register)	t_{SYCD2}	—	70	t_{CLK}

t_{CLK}: See “(2) Clock Signals”.

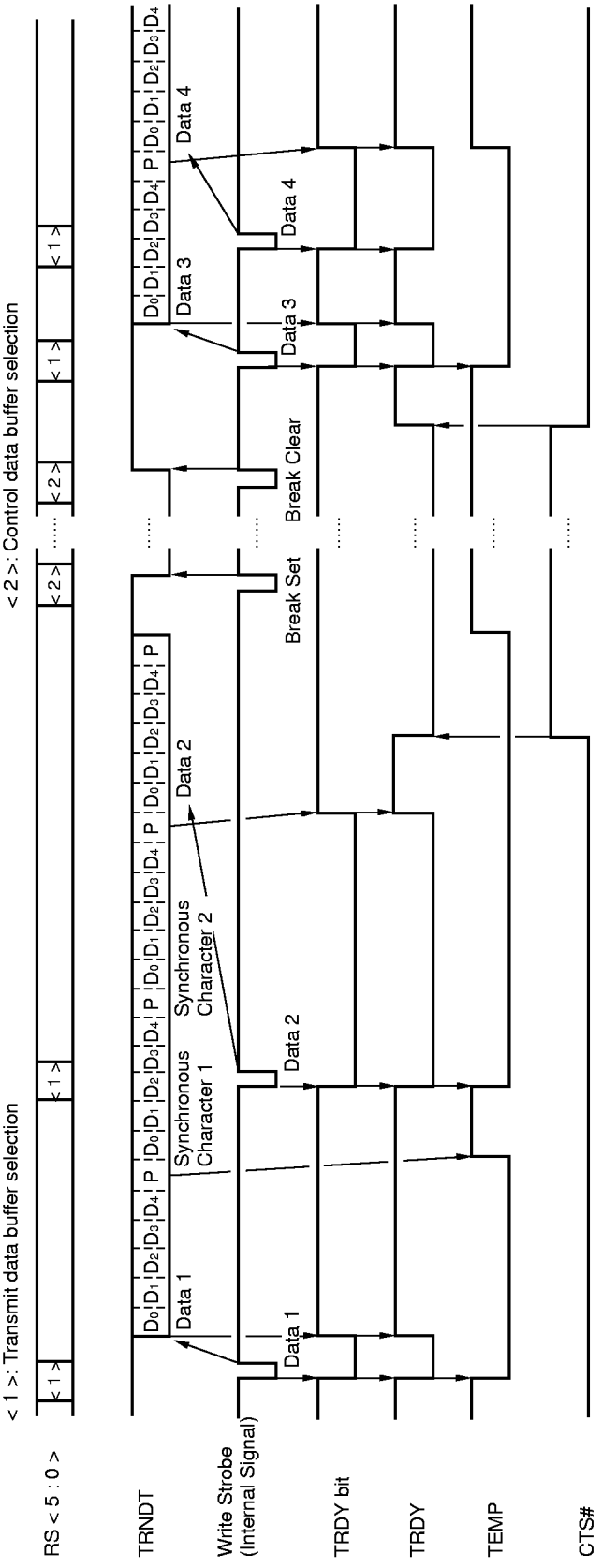
• Receive Timing Example 1 (Asynchronous mode, 5 data bits, Parity enable, 2 stop bits)



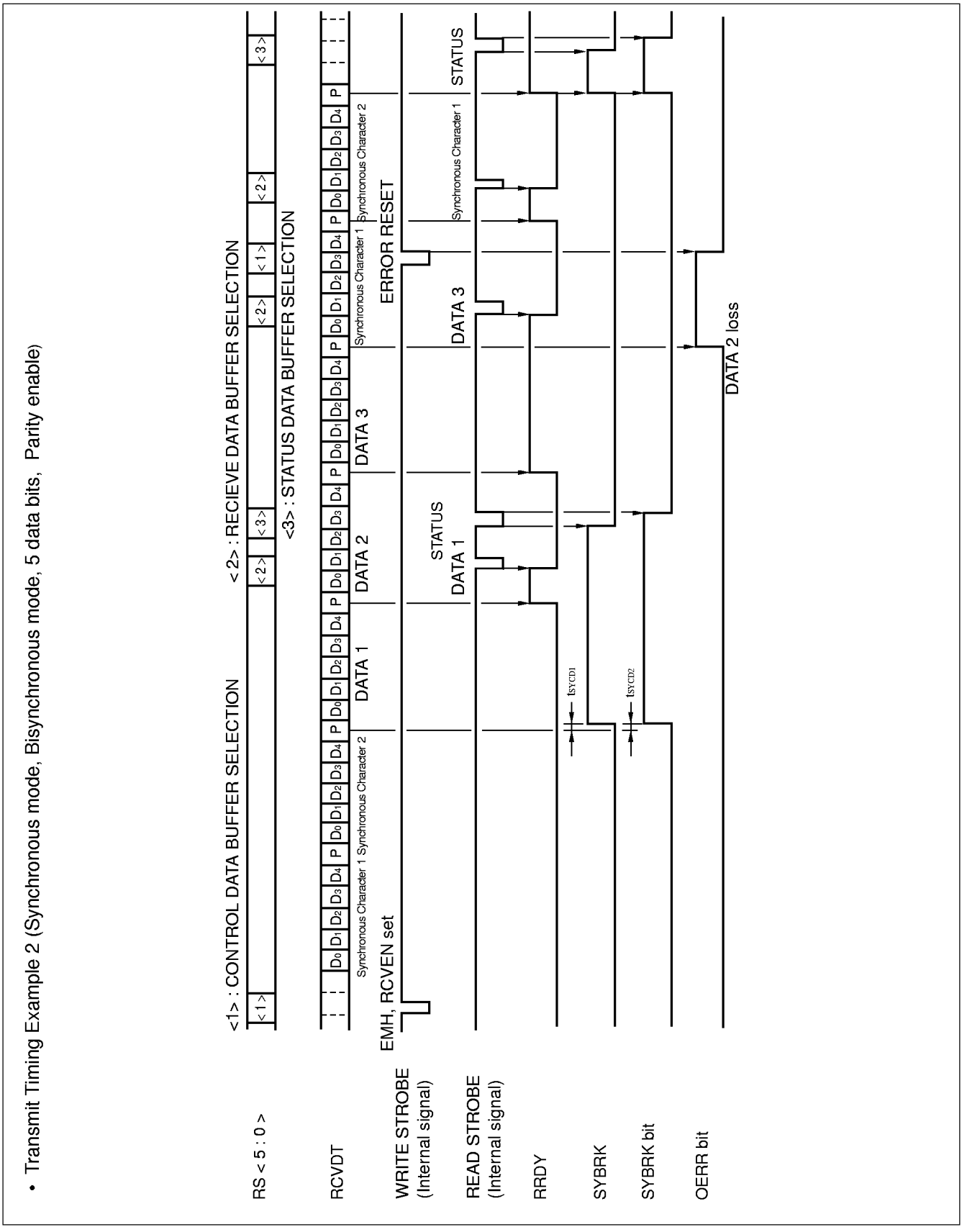
• Transmit Timing Example 1 (Asynchronous mode, 6 data bits, Parity enable, 2 stop bits)



• Transmit Timing Example 2 (Synchronous mode, Bisynchronous mode, 5 data bits, Parity enable)



• Transmit Timing Example 2 (Synchronous mode, Bisynchronous mode, 5 data bits, Parity enable)



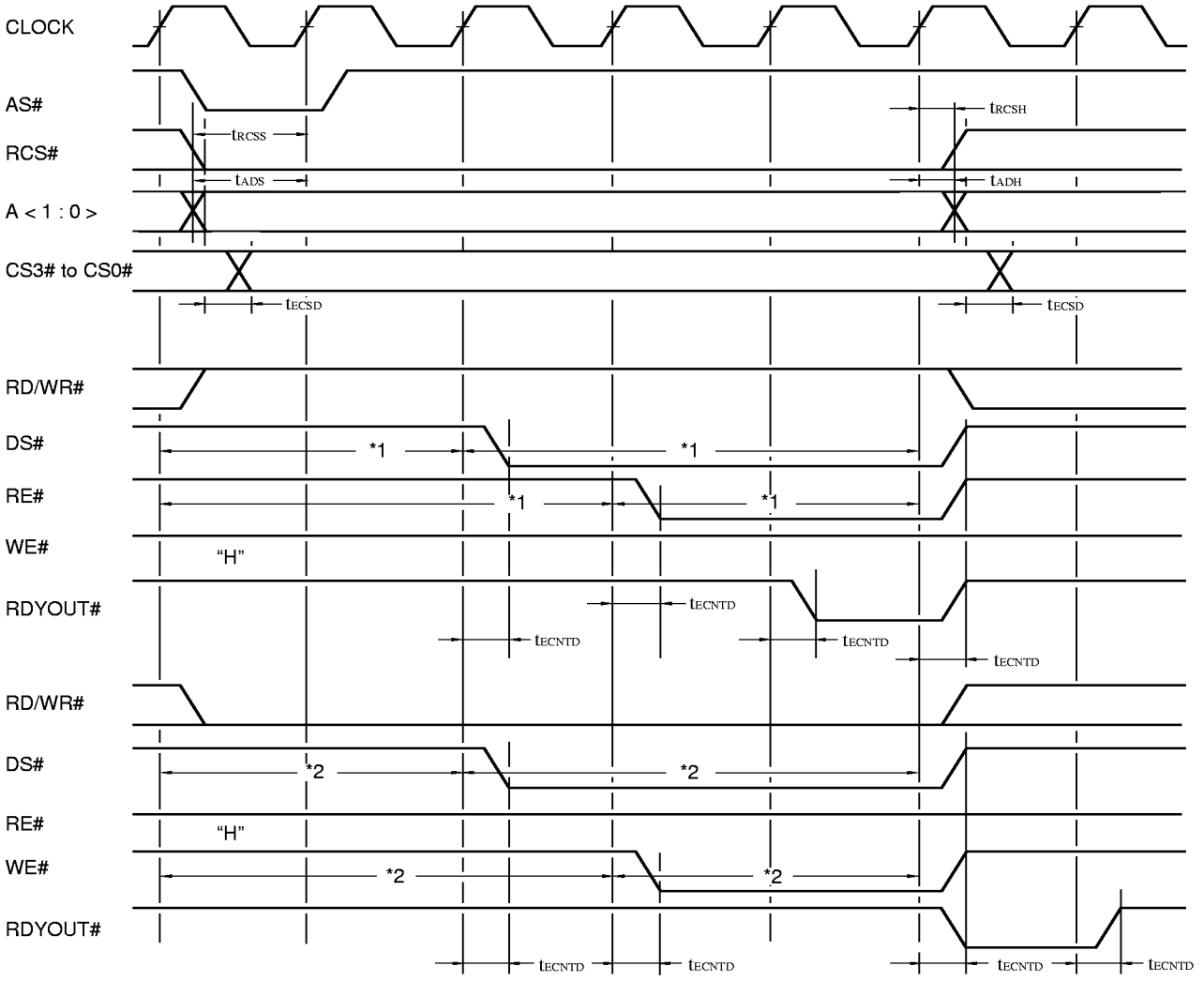
(7) RCSTG

• Control Signal Output Timing

(MB86941: V_{DD} = 5 V ± 5%, T_A = 0 to +70°C)
(MB86942: V_{DD} = 3.3 V ± 0.15 V, T_A = 0 to +70°C)

Parameter	Symbol	MB86941		MB86942		Unit
		Min.	Max.	Min.	Max.	
RCS# setup time	t_{RCSS}	5	—	7	—	ns
RCS# hold time	t_{RCSH}	5	—	2	—	ns
A < 1 : 0 > setup time	t_{ADS}	5	—	7	—	ns
A < 1 : 0 > hold time	t_{ADH}	5	—	2	—	ns
Delay time from RCS#, A1, A0 fix to CS3# to CS0# fix	t_{ECSD}	—	15	—	18	ns
Delay time from CLOCK to RE#, WE#, DS# fix	t_{ECNTD}	—	15	—	18	ns

• Register Read Control Signal Output Timing



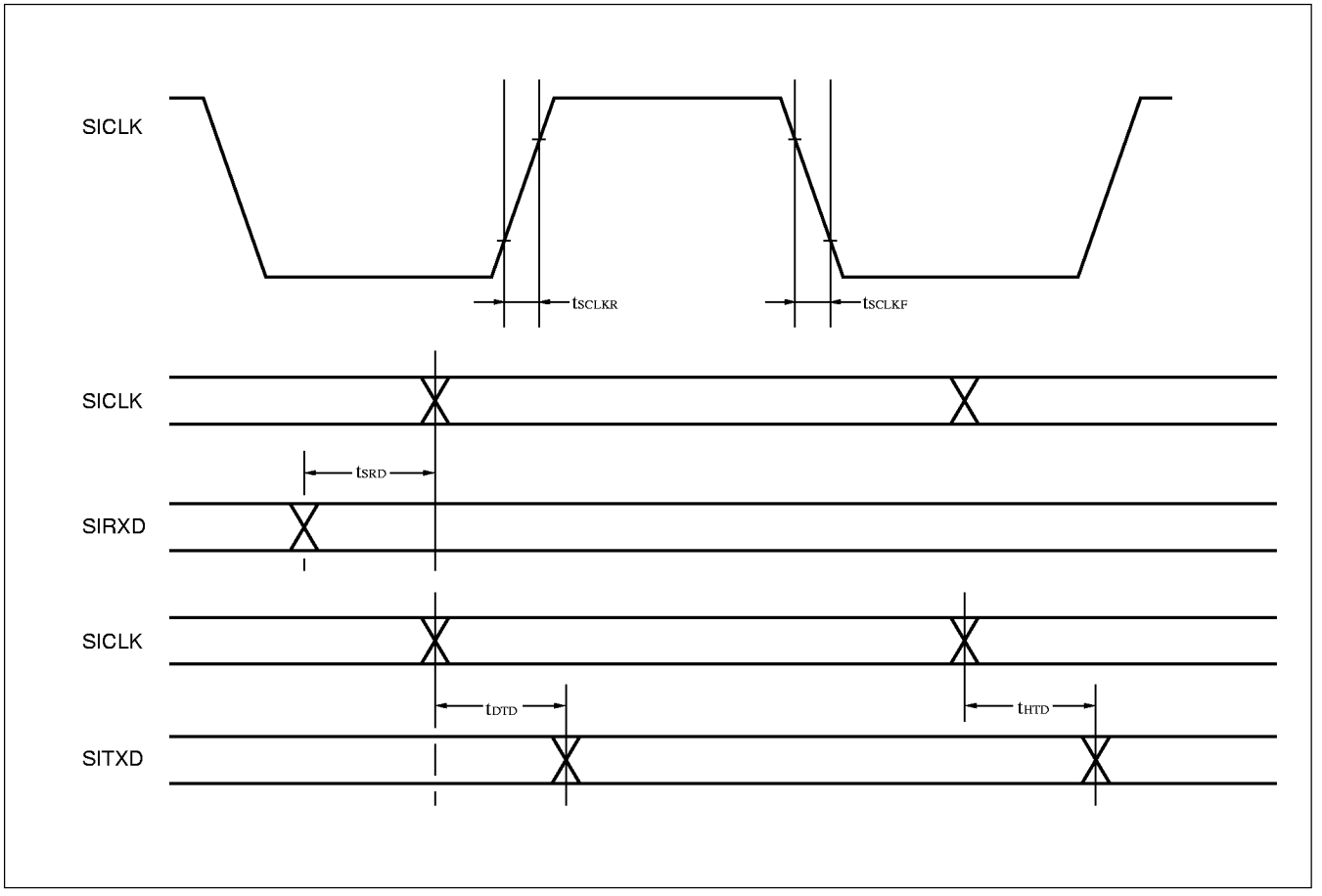
*1: Set register RTR0, RTR1.
*2: Set register WTR0, WTR1.

(8) SIO

• Control Signal Output Timing

(MB86941: V_{DD} = 5 V ± 5%, T_A = 0 to +70°C)
(MB86942: V_{DD} = 3.3 V ± 0.15 V, T_A = 0 to +70°C)

Parameter		Symbol	Value		Unit
			Min.	Max.	
SICLK rise time		t_{SCLKR}	—	3	ns
SICLK fall time		t_{SCLKF}	—	3	ns
Setup time from SICLK rise/fall to valid SIRXD	at receiving	t_{SRD}	80	—	ns
Delay time from SICLK rise/fall to SITXD output	at transmitting	t_{DTD}	—	30	ns
Hold time from SICLK rise/fall to valid SITXD		t_{HTD}	80	—	ns



■ NOTES ON USE

When the prescaler is used in external clock mode, and the prescaler output signal is used as the timer operating clock, use the following settings.

Set the timer operating clock to 'External clock' (TCR bits 10, 9 = "01"), and connect the prescaler output pin PRSCK externally to the timer external clock input pin CLK.

When the prescaler and timer are set to the following modes, the timer output signal OUT will not change at the anticipated time:

Prescaler: External clock mode (PRESCALER REGISTER bit15 = "1").
Timer: Prescaler internal output signal used as operating clock, without using the external input pin (TCR bit 10, 9 = "10").

■ REGISTER MAP

Block name	RS5 to RS0 (HEX)	Register name	bit															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IRC	00H	TM0 (TRIGGER MODE 0)	CH15		CH14		CH13		CH12		CH11		CH10		CH9		CH8	
	01H	TM1 (TRIGGER MODE 1)	CH7		CH6		CH5		CH4		CH3		CH2		CH1		—	—
	02H	RS (REQ SENSE)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	—
	03H	RC (REQ CLEAR)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	—
	04H	MASK (MASK)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	IM
	05H	IRL (IRL Latch/Clear)	—	—	—	—	—	—	—	—	—	—	—	CL	IRL LATCH			
Reserved	06H	Reserved	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	07H		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
SDTR 0	08H	SDR0 (SDTR Data 0)	—	—	—	—	—	—	—	—	TRANSMIT DATA/ RECEIVE DATA							
	09H	SCSR0 (SDTR CM/ST 0)	—	—	—	—	—	—	—	—	CONTROL DATA/STATUS DATA							
Reserved	0AH	Reserved	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	0BH		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
SDTR 1	0CH	SDR1 (SDTR Dsta 1)	—	—	—	—	—	—	—	—	TRANSMIT DATA/ RECEIVE DATA							
	0DH	SCSR1 (SDTR CM/ST 1)	—	—	—	—	—	—	—	—	CONTROL DATA/ STATUS DATA							
Reserved	0EH	Reserved	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	0FH		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
PRESCALER0	10H	PRS0 (PRESCALE 0)	EX	TEST	—	—	—	SELECT			PRESCALE VALUE							

(Continued)

Block name	RS5 to RS0 (HEX)	Register name	bit														
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIMER 0	11H	TCR0 (TIMER CONTROL 0)	OT	IN	—	TEST	CE	CS		OCONT		IV	MODE			EVENT		
	12H	RVR0 (RELOAD VALUE 0)	RELOAD VALUE															
	13H	CVR0 (COUNT VALUE 0)	COUNT VALUE															
PRESCALER1	14H	PRS1 (PRESCALE 1)	EX	TEST	—	—	—	SELECT				PRESCALE VALUE						
TIMER 1	15H	TCR1 (TIMER CONTROL 1)	OT	IN	—	TEST	CE	CS		OCONT		IV	MODE			EVENT		
	16H	RVR1 (RELOAD VALUE 1)	RELOAD VALUE															
	17H	CVR1 (COUNT VALUE 1)	COUNT VALUE															
Reserved	18H	Reserved	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
TIMER 2	19H	TCR2 (TIMER CONTROL 2)	OT	IN	—	TEST	CE	CS		OCONT		IV	MODE			EVENT		
	1AH	RVR2 (RELOAD VALUE 2)	RELOAD VALUE															
	1BH	CVR2 (COUNT VALUE 2)	COUNT VALUE															
Reserved	1CH	Reserved	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
TIMER 3	1DH	TCR3 (TIMER CONTROL 3)	TO	IN	—	TEST	CE	CS		OCONT		IV	MODE			EVENT		
	1EH	RVR3 (RELOAD VALUE 3)	RELOAD VALUE															
	1FH	CVR3 (COUNT VALUE 3)	COUNT VALUE															

(Continued)

(Continued)

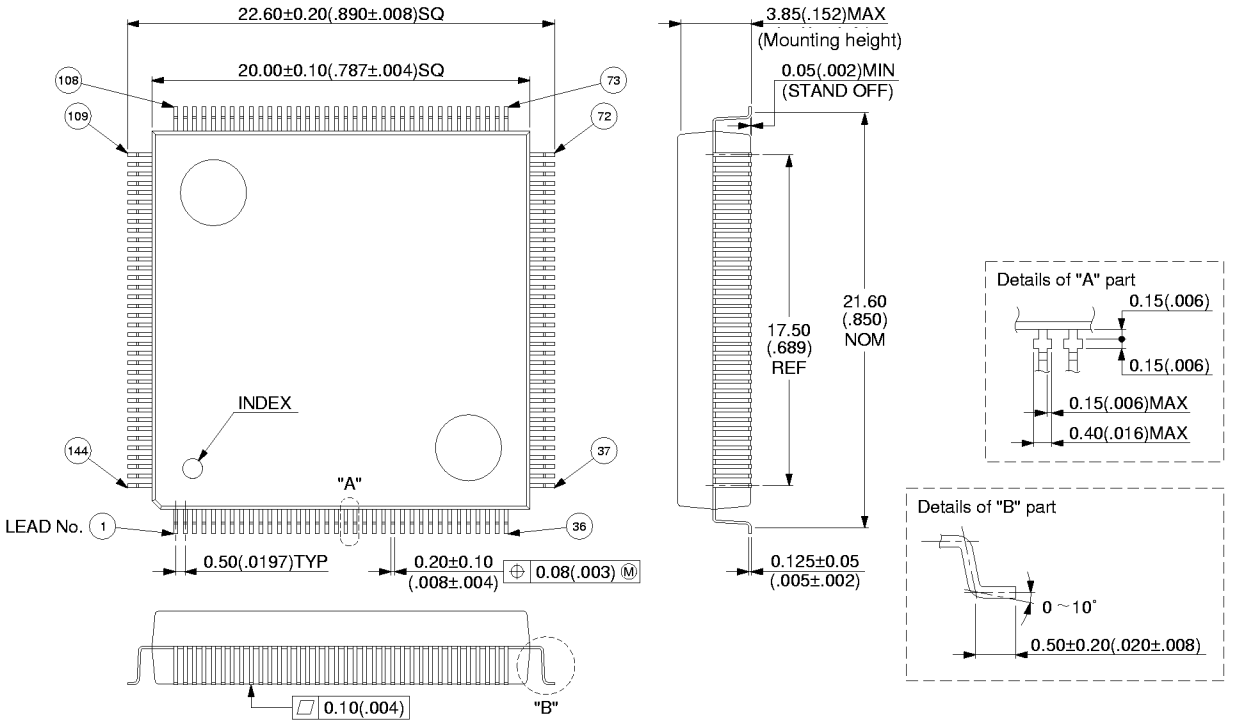
Block name	RS5 to RS0 (HEX)	Register name	bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I/O PORT	20H	PDR (PORT DATA)	PORT DATA															
	21H	DCR (PORT DIRECTION)	PORT DIRECTION															
Reserved	22H	Reserved	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	23H		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
SIO	24H	SCR (SERIAL CONTROL)	—	—	—	—	—	—	—	—	CONTROL							
	25H	STR (SERIAL STATUS)	—	—	—	—	—	—	—	—	—	—	—	—	STATUS			
	26H	RDR (RECEIVE DATA)	—	—	—	—	—	—	—	—	RECEIVE DATA							
	27H	TDR (TRANSMIT DATA)	—	—	—	—	—	—	—	—	TRANSMIT DATA							
	28H	TRR (TRANSFER RATE)	—	—	—	—	—	—	—	—	—	—	—	—	—	RATE SELECT		
Reserved	29H	Reserved	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	2AH		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	2BH		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
TIMING0	2CH	RTR0 (READ TIMING 0)	—	—	—	—	—	—	TREW			TRDSW			TREL		TRDSL	
	2DH	WTR0 (WRITE TIMING 0)	—	—	—	—	—	—	TWEW			TWDSW			TWEL		TWDSL	
TIMING1	2EH	RTR1 (READ TIMING 1)	—	—	—	—	—	—	TREW			TRDSW			TREL		TRDSL	
	2FH	WTR1 (WRITE TIMING 1)	—	—	—	—	—	—	TWEW			TWDSW			TWEL		TWDSL	

■ ORDERING INFORMATION

Part number	Package	Remarks
MB86941PFV	144-pin Plastic QFP (FPT-144P-M03)	
MB86942PFV	144-pin Plastic QFP (FPT-144P-M03)	

■ PACKAGE DIMENSION

144-pin Plastic QFP
(FPT-144P-M03)



Dimensions in mm (inches)