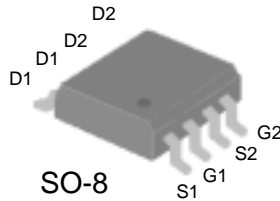


Dual N-channel Enhancement-mode Power MOSFETs

- Simple drive requirement
- Lower gate charge
- Fast switching characteristics

 **Pb-free; RoHS compliant.**

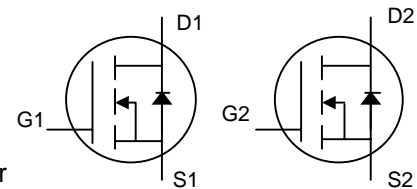


BV_{DSS}	20V
$R_{DS(ON)}$	35m Ω
I_D	6A

DESCRIPTION

Advanced Power MOSFETs from Silicon Standard provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SSM4924GM is in an SO-8 package, which is widely preferred for commercial and industrial surface mount applications. This device is suitable for low voltage applications such as DC/DC converters.



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	20	V
V_{GS}	Gate-Source Voltage	± 8	V
$I_D @ T_A = 25^\circ\text{C}$	Continuous Drain Current ³	6	A
$I_D @ T_A = 70^\circ\text{C}$	Continuous Drain Current ³	4.8	A
I_{DM}	Pulsed Drain Current ^{1,4}	35	A
$P_D @ T_A = 25^\circ\text{C}$	Total Power Dissipation	2	W
	Linear Derating Factor	0.016	W/ $^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{thj-amb}$	Thermal Resistance Junction-ambient	Max. 62.5	$^\circ\text{C}/\text{W}$

ELECTRICAL CHARACTERISTICS @ $T_j = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	20	-	-	V
$\Delta BV_{DSS}/\Delta T_j$	Breakdown Voltage Temperature Coefficient	Reference to 25°C , $I_D=1\text{mA}$	-	0.037	-	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=4.5V, I_D=6A$	-	-	35	$\text{m}\Omega$
		$V_{GS}=2.5V, I_D=5.2A$	-	-	50	$\text{m}\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	0.5	-	1.2	V
g_{fs}	Forward Transconductance	$V_{DS}=10V, I_D=6A$	-	18.5	-	S
I_{DSS}	Drain-Source Leakage Current ($T_j=25^\circ\text{C}$)	$V_{DS}=20V, V_{GS}=0V$	-	-	1	μA
	Drain-Source Leakage Current ($T_j=70^\circ\text{C}$)	$V_{DS}=16V, V_{GS}=0V$	-	-	25	μA
I_{GSS}	Gate-Source Leakage	$V_{GS}=\pm 8V$	-	-	± 100	nA
Q_g	Total Gate Charge ²	$I_D=6A$	-	9	-	nC
Q_{gs}	Gate-Source Charge	$V_{DS}=10V$	-	1.8	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{GS}=4.5V$	-	4.2	-	nC
$t_{d(on)}$	Turn-on Delay Time ²	$V_{DS}=10V$	-	6.5	-	ns
t_r	Rise Time	$I_D=1A$	-	14	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=6\Omega, V_{GS}=4.5V$	-	20	-	ns
t_f	Fall Time	$R_D=10\Omega$	-	15	-	ns
C_{iss}	Input Capacitance	$V_{GS}=0V$	-	300	-	pF
C_{oss}	Output Capacitance	$V_{DS}=8V$	-	255	-	pF
C_{rss}	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	115	-	pF

SOURCE-DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_S	Continuous Source Current (Body Diode)	$V_D=V_G=0V, V_S=1.2V$	-	-	1.7	A
I_{SM}	Pulsed Source Current (Body Diode) ¹		-	-	35	A
V_{SD}	Forward On Voltage ²	$T_j=25^\circ\text{C}, I_S=1.7A, V_{GS}=0V$	-	0.75	1.2	V

Notes:

1. Pulse width limited by maximum junction temperature.
2. Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
3. Surface-mounted on FR4 board, $t_{\leq 10\text{sec}}$.
4. Pulse width $\leq 10\mu s$, duty cycle $\leq 1\%$.

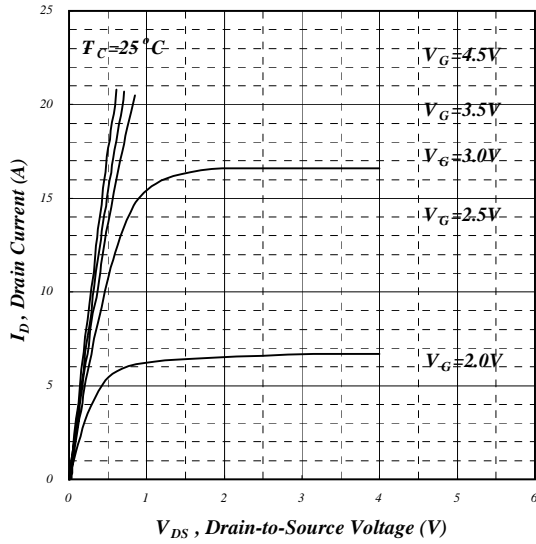


Fig 1. Typical Output Characteristics

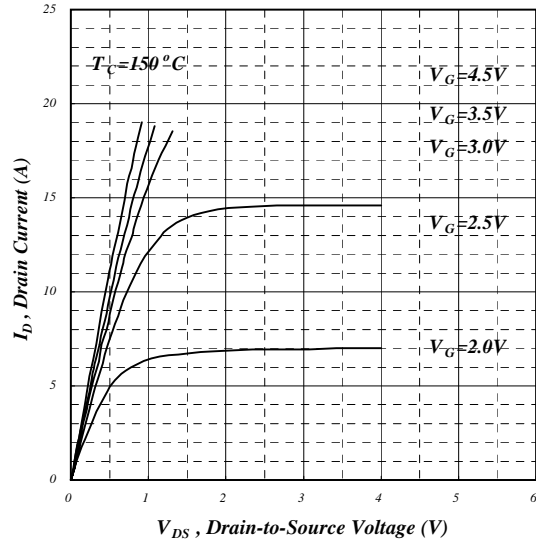


Fig 2. Typical Output Characteristics

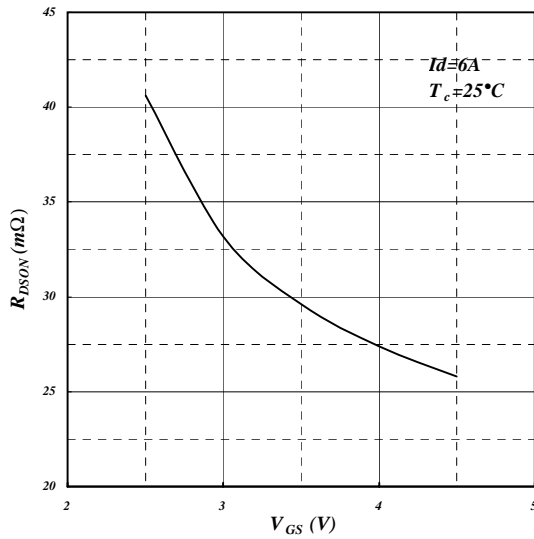


Fig 3. On-Resistance vs. Gate Voltage

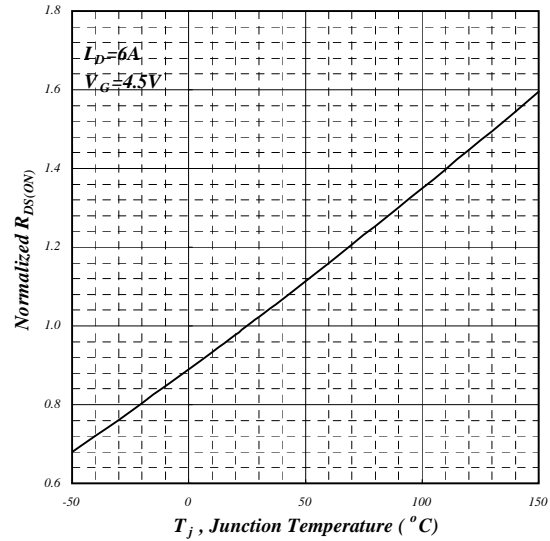


Fig 4. Normalized On-Resistance vs. Junction Temperature

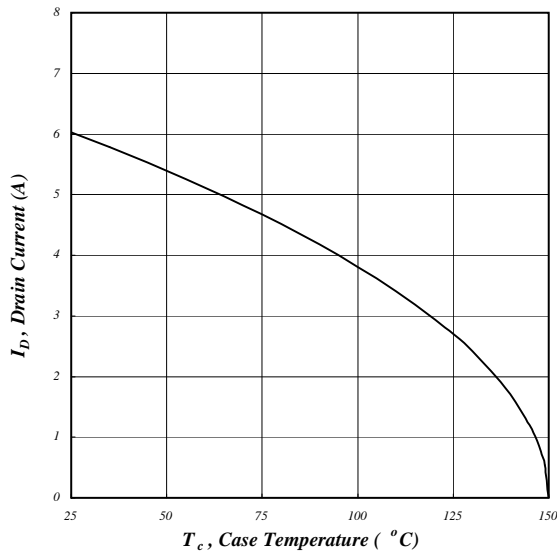


Fig 5. Maximum Drain Current vs. Case Temperature

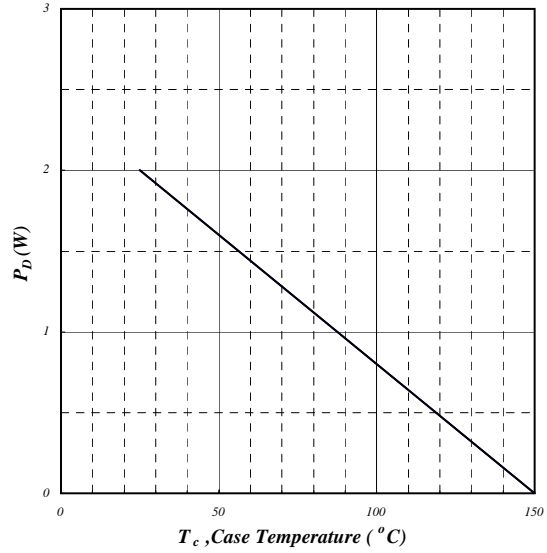


Fig 6. Typical Power Dissipation

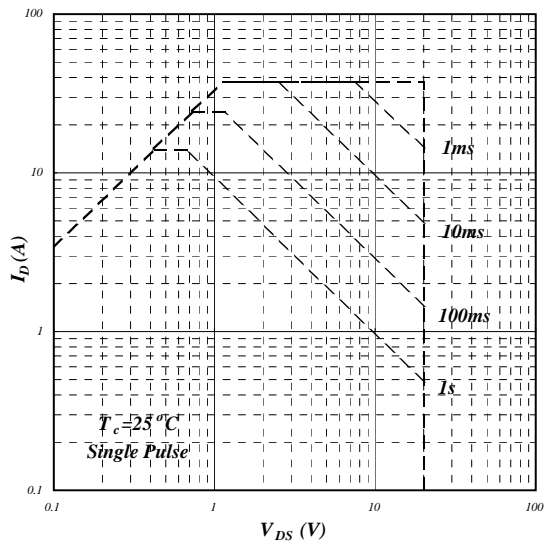


Fig 7. Maximum Safe Operating Area

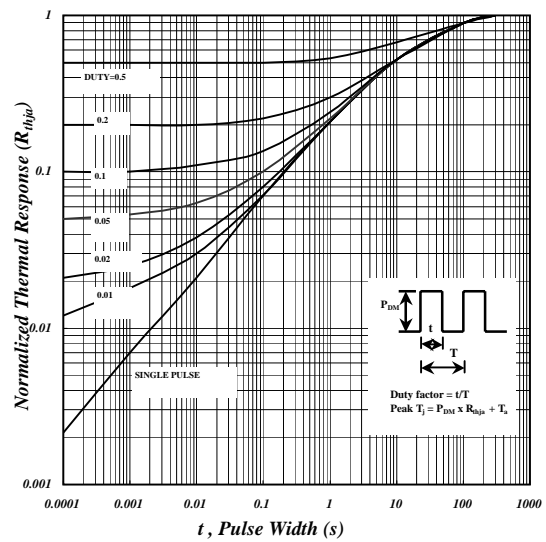


Fig 8. Effective Transient Thermal Impedance

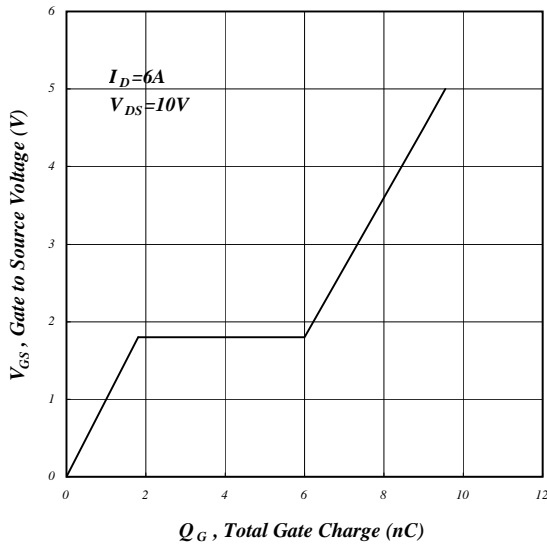


Fig 9. Gate Charge Characteristics

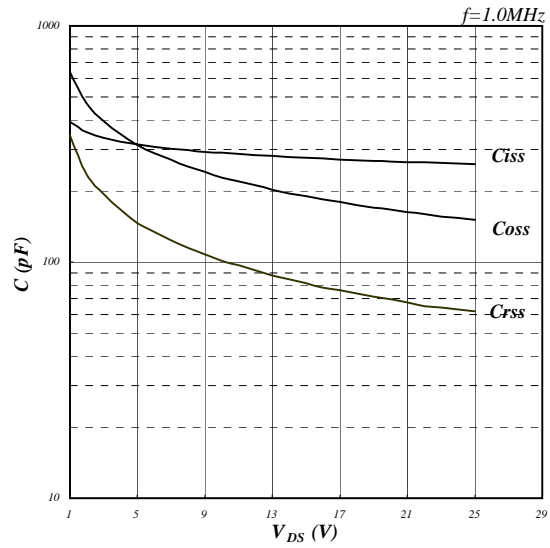


Fig 10. Typical Capacitance Characteristics

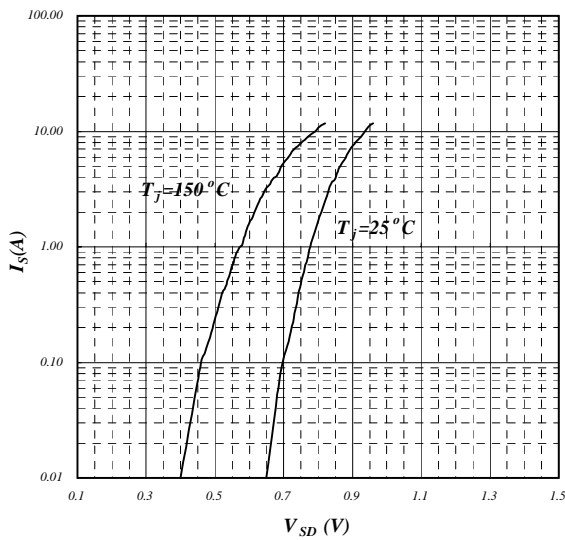


Fig 11. Forward Characteristic of Reverse Diode

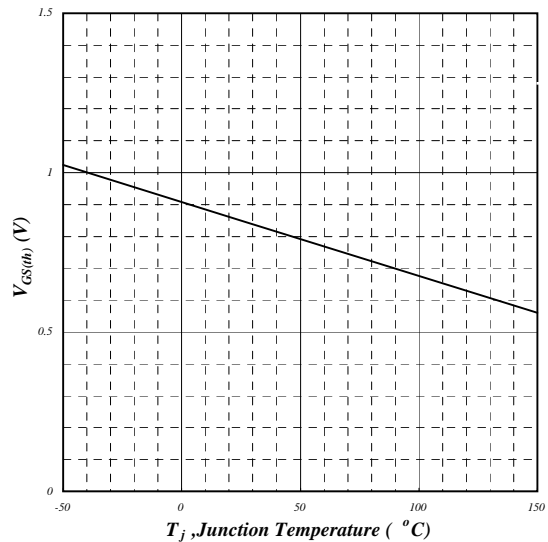


Fig 12. Gate Threshold Voltage vs. Junction Temperature

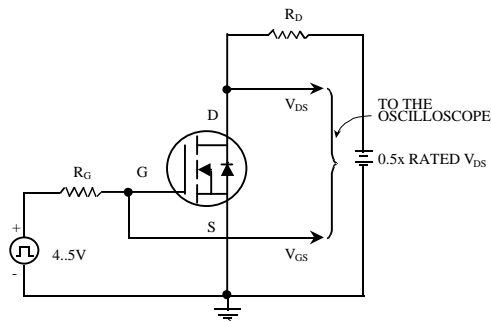


Fig 13. Switching Time Circuit

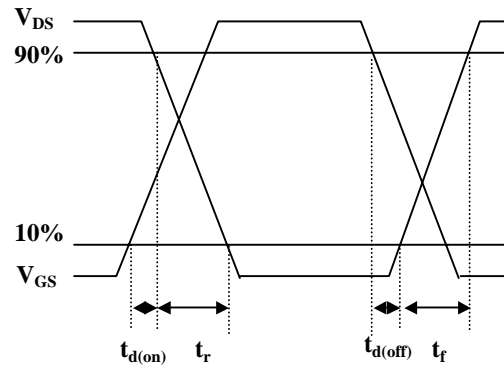


Fig 14. Switching Time Waveform

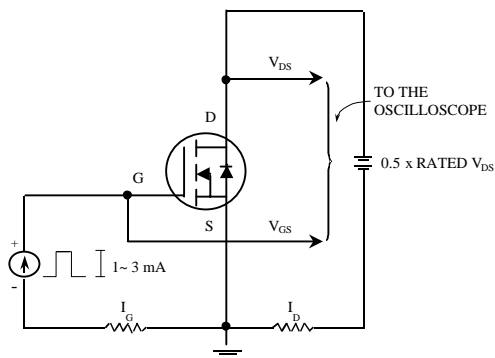


Fig 15. Gate Charge Circuit

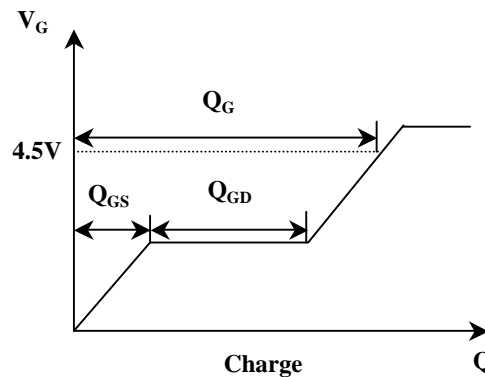


Fig 16. Gate Charge Waveform

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