4 K × 9 CMOS Parallel FIFO Rad Tolerant

Introduction

The M67204E implement a first-in first-out algorithm, featuring asynchronous read/write operations. The FULL and EMPTY flags prevent data overflow and underflow. The Expansion logic allows unlimited expansion in word size and depth with no timing penalties. Twin address pointers automatically generate internal read and write addresses, and no external address information are required for the TEMIC FIFOs. Address pointers are automatically incremented with the write pin and read pin. The 9 bits wide data are used in data communications applications where a parity bit for error checking is necessary. The Retransmit pin resets the Read pointer to zero without affecting the write pointer. This is very useful for retransmitting data when an error is detected in the system.

Using an array of eigh transistors (8 T) memory cell, the M67204E combine an extremely low standby supply current (typ = 1.0 µA) with a fast access time at 40 ns over the full temperature range. All versions offer battery backup data retention capability with a typical power consumption at less than 2 µW.

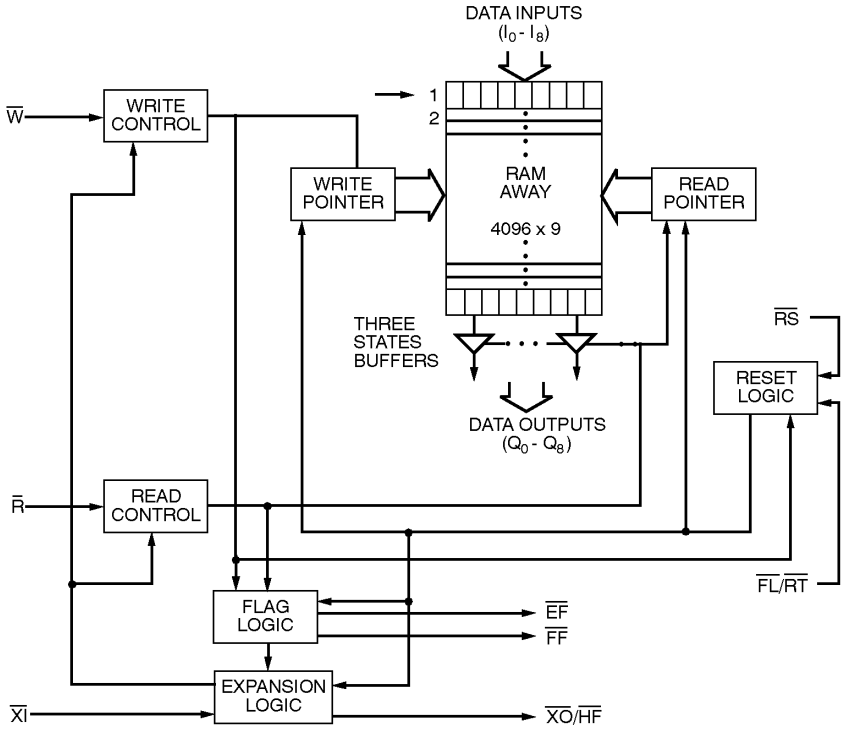
The M67204E is processed according to the methods of the latest revision of the MIL STD 883 (class B or S), ESA SCC 9000 and QML.

Features

- First-in first-out dual port memory
- 4096 × 9 organisation
- Fast access time: 40, 50 ns
- Wide temperature range : – 55 °C to + 125 °C
- Fully expandable by word width or depth
- Asynchronous read/write operations
- Empty, full and half flags in single device mode
- Retransmit capability
- Bi-directional applications
- Battery back-up operation 2 V data retention
- TTL compatible
- Single 5 V ± 10 % power supply
- High performance SCMOS technology

Interface

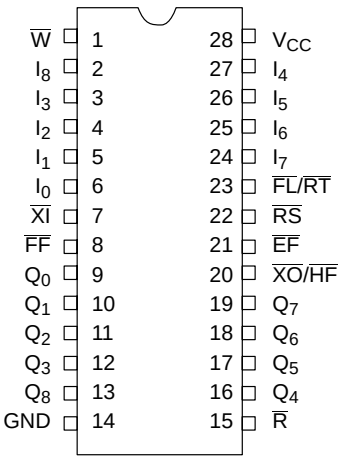
Block Diagram



Pin Configuration

DIL ceramic 28 pin 300 mils
FP 28 pin 400 mils

(top view)



Pin Names

NAMES	DESCRIPTION
I0–8	Inputs
Q0–8	Outputs
$\overline{W}$	Write Enable
$\overline{R}$	Read Enable
$\overline{RS}$	Reset
$\overline{EF}$	Empty Flag

NAMES	DESCRIPTION
$\overline{FF}$	Full Flag
$\overline{XO/HF}$	Expansion Out/Half-Full Flag
$\overline{XI}$	Expansion IN
$\overline{FL/RT}$	First Load/Retransmit
VCC	Power Supply
GND	Ground

Signal Description

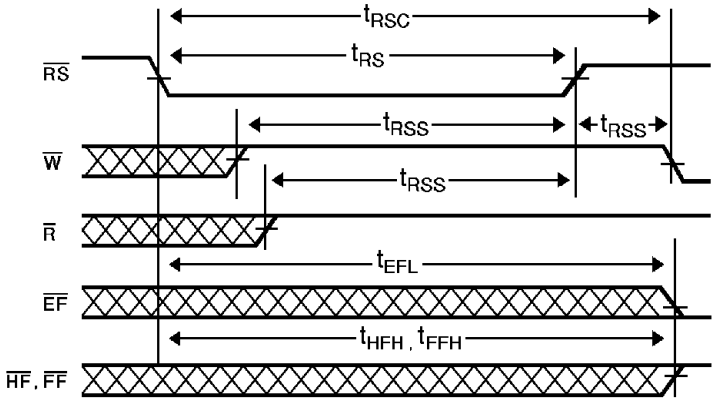
Data In (I0 - I8)

Data inputs for 9-bit data

Reset ($\overline{RS}$)

Reset occurs whenever the Reset ($\overline{RS}$) input is taken to a low state. Reset returns both internal read and write pointers to the first location. A reset is required after power-up before a write operation can be enabled. Both the Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) inputs must be in the high state during the period shown in figure 1 (i.e. t_{RSS} before the rising edge of $\overline{RS}$) and should not change until t_{RSR} after the rising edge of $\overline{RS}$. The Half-Full Flag ($\overline{HF}$) will be reset to high after Reset ($\overline{RS}$).

Figure 1. Reset.



Notes : 1. $\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during reset, but flags will be valid at t_{RSC}.
2. $\overline{W}$ and $\overline{R}$ = V_{IH} around the rising edge of RS.

Write Enable ($\overline{W}$)

A write cycle is initiated on the falling edge of this input if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be maintained in the rise time of the leading edge of the Write Enable ($\overline{W}$). Data is stored sequentially in the Ram array, regardless of any current read operation.

Once half of the memory is filled, and during the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and remain in this state until the difference between the write and read pointers is less than or equal to half of the total available memory in the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go low, inhibiting further write operations. On completion of a valid read operation, the Full Flag ($\overline{FF}$) will go high after TRFF, allowing a valid write to begin. When the FIFO stack is full, the internal write pointer is blocked from $\overline{W}$, so that external changes to $\overline{W}$ will have no effect on the full FIFO stack.

Read Enable ($\overline{R}$)

A read cycle is initiated on the falling edge of the Read Enable ($\overline{R}$) provided that the Empty Flag ($\overline{EF}$) is not set. The data is accessed on a first in/first out basis, not with standing any current write operations. After Read Enable ($\overline{R}$) goes high, the Data Outputs (Q0 – Q8) will return to a high impedance state until the next Read operation. When all the data in the FIFO stack has been read, the Empty Flag ($\overline{EF}$) will go low, allowing the "final" read cycle, but inhibiting further read operations whilst the data outputs remain in a high impedance state. Once a valid write operation has been completed, the Empty Flag ($\overline{EF}$) will go high after tWEF and a valid read may then be initiated. When the FIFO stack is empty, the internal read pointer is blocked from $\overline{R}$, so that external changes to $\overline{R}$ will have no effect on the empty FIFO stack.

First Load/Retransmit ($\overline{FL/RT}$)

This is a dual-purpose input. In the Depth Expansion Mode, this pin is connected to ground to indicate that it is the first loaded (see Operating Modes). In the Single Device Mode, this pin acts as the retransmit input. The Single Device Mode is initiated by connecting the Expansion In ($\overline{XI}$) to ground.

The M67204E can be made to retransmit data when the Retransmit Enable Control ($\overline{RT}$) input is pulsed low. A retransmit operation will set the internal read point to the first location and will not affect the write pointer. Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must be in the high state during retransmit. The retransmit feature is intended for use when a number of writes equals to or less than the depth of the FIFO have occured since the last $\overline{RS}$ cycle. The retransmit feature is not compatible with the Depth Expansion Mode and will affect the Half-Full Flag ($\overline{HF}$), in accordance with the relative locations of the read and write pointers.

Expansion In ($\overline{XI}$)

This input is a dual-purpose pin. Expansion In ($\overline{XI}$)is connected to GND to indicate an operation in the single device mode. Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy Chain modes.

Full Flag ($\overline{FF}$)

The Full Flag ($\overline{FF}$) will go low, inhibiting further write operations when the write pointer is one location less than the read pointer, indicating that the device is full. If the read pointer is not moved after Reset ($\overline{RS}$), the Full Flag ($\overline{FF}$) will go low after 4096 writes.

Empty Flag ($\overline{EF}$)

The Empty Flag ($\overline{EF}$) will go low, inhibiting further read operations when the read pointer is equal to the write pointer, indicating that the device is empty.

Expansion Out/Half-full Flag ($\overline{XO/HF}$)

This is a dual-purpose output. In the single device mode, when Expansion In ($\overline{XI}$) is connected to ground, this output acts as an indication of a half-full memory.

After half the memory is filled and on the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and will remain set until the difference between the write and read pointers is less than or equal to half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

In the Depth Expansion Mode, Expansion In (XI) is connected to Expansion Out ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last memory location.

Data Output ($Q_0 – Q_8$)

DATA output for 9-bit wide data. This data is in a high impedance condition whenever Read (R) is in a high state.

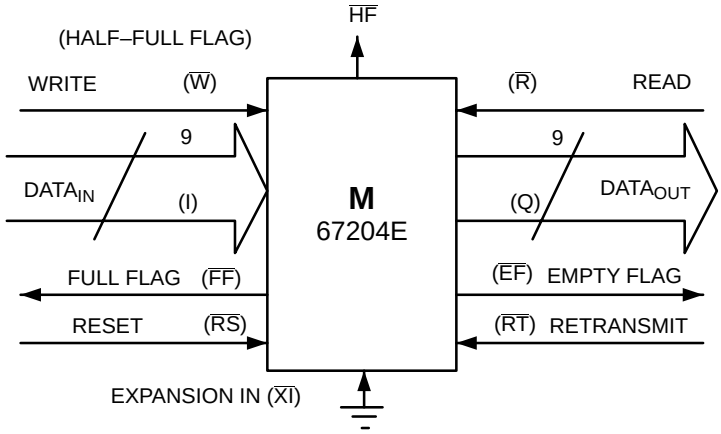
Functional Description

Operating Modes

Single Device Mode

A single M67204E may be used when the application requirements are for 4096 words or less. The M67204E is in a Single Device Configuration when the Expansion In ($\overline{XI}$) control input is grounded (see Figure 2). In this mode the Half-Full Flag ($\overline{HF}$), which is an active low output, is shared with Expansion Out ($\overline{XO}$).

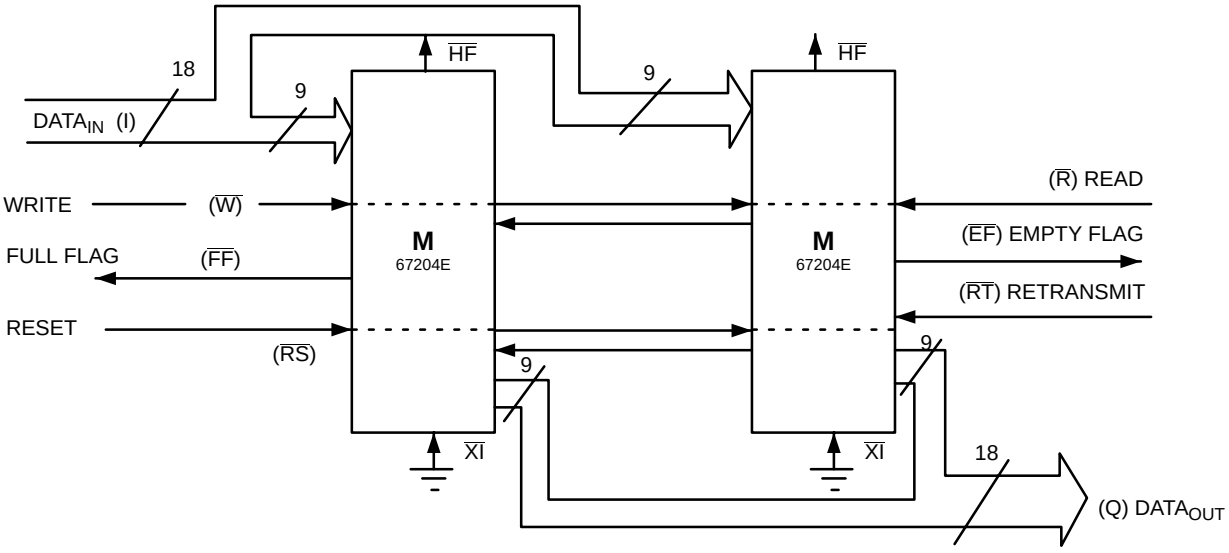
Figure 2. Block Diagram of Single 4K × 9 FIFO.



Width Expansion Mode

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$ and $\overline{HF}$) can be detected from any device. Figure 3 demonstrates an 18-bit word width by using two M67204E. Any word width can be attained by adding additional M67204E.

Figure 3. Block Diagram of 4096 × 18 FIFO Memory Used in Width Expansion Mode.



Note : 3. Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$ and the $\overline{HF}$ signals on either (any) device used in the width expansion configuration. Do not connect any output control signals together.

Table 1 : Reset and retransmit
Single Device Configuration/Width Expansion Mode

MODE	INPUTS			INTERNAL STATUS		OUTPUTS		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment(4)	Increment(4)	X	X	X

Note : 4. Pointer will increment if flag is high.

Table 2 : Reset and First Load Truth Table
Depth Expansion/Compound Expansion Mode

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset First Device	0	0	(5)	Location Zero	Location Zero	0	1
Reset All Other Devices	0	1	(5)	Location Zero	Location Zero	0	1
Read/Write	1	X	(5)	X	X	X	X

Note : 5. $\overline{XI}$ is connected to $\overline{XO}$ of previous device.
See fig. 5.

Depth Expansion (Daisy Chain) Mode

The M67204E can be easily adapted for applications which require more than 4096 words. Figure 4 demonstrates Depth Expansion using three M67204E. Any depth can be achieved by adding additional M67204E.

The M67204E operate in the Depth Expansion configuration if the following conditions are met :

1. The first device must be designated by connecting the First Load ($\overline{FL}$) control input to ground.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be connected to the Expansion In ($\overline{XI}$) pin of the next device. See figure 4.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires that all $\overline{EF}$'s and all $\overline{FF}$s be ØRed (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See figure 4.
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion Mode.

Compound Expansion Module

It is quite simple to apply the two expansion techniques described above together to create large FIFO arrays (see figure 5).

Bidirectional Mode

Applications which require data buffering between two systems (each system being capable of Read and Write operations) can be created by coupling M67204E as shown in figure 6. Care must be taken to ensure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the device on which $\overline{W}$ is in use ; $\overline{EF}$ is monitored on the device on which $\overline{R}$ is in use). Both Depth Expansion and Width Expansion may be used in this mode.

Data Flow - Through Modes

Two types of flow-through modes are permitted : a read flow-through and a write flow-through mode. In the read flow-through mode (figure 17) the FIFO stack allows a

single word to be read after one word has been written to an empty FIFO stack. The data is enabled on the bus at (tWEF + tA) ns after the leading edge of $\overline{W}$ which is known as the first write edge and remains on the bus until the $\overline{R}$ line is raised from low to high, after which the bus will go into a three-state mode after tRHZ ns. The $\overline{EF}$ line will show a pulse indicating temporary reset and then will be set. In the interval in which $\overline{R}$ is low, more words may be written to the FIFO stack (the subsequent writes after the first write edge will reset the Empty Flag) ; however, the same word (written on the first write edge) presented to the output bus as the read pointer will not be incremented if $\overline{R}$ is low. On toggling $\overline{R}$, the remaining words written to the FIFO will appear on the output bus in accordance with the read cycle timings.

In the write flow-through mode (figure 18), the FIFO stack allows a single word of data to be written immediately after a single word of data has been read from a full FIFO stack. The $\overline{R}$ line causes the $\overline{FF}$ to be reset, but the $\overline{W}$ line, being low, causes it to be set again in anticipation of a new data word. The new word is loaded into the FIFO stack on the leading edge of $\overline{W}$. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not set in order to write new data into the FIFO stack and to increment the write pointer.

Figure 4. Block Diagram of 12288 × 9 FIFO Memory (Depth expansion).

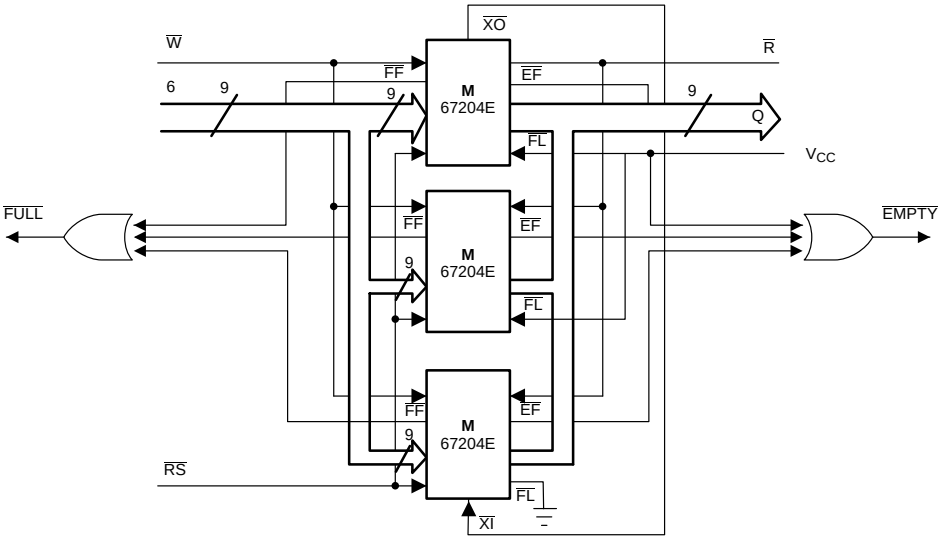
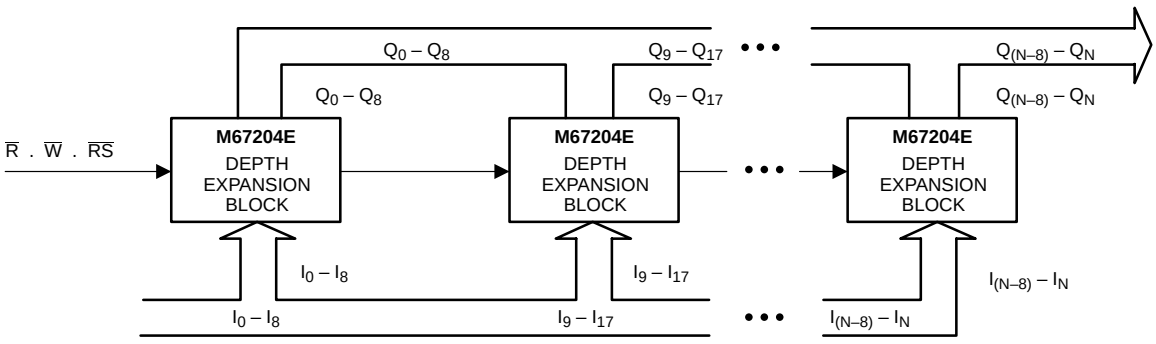
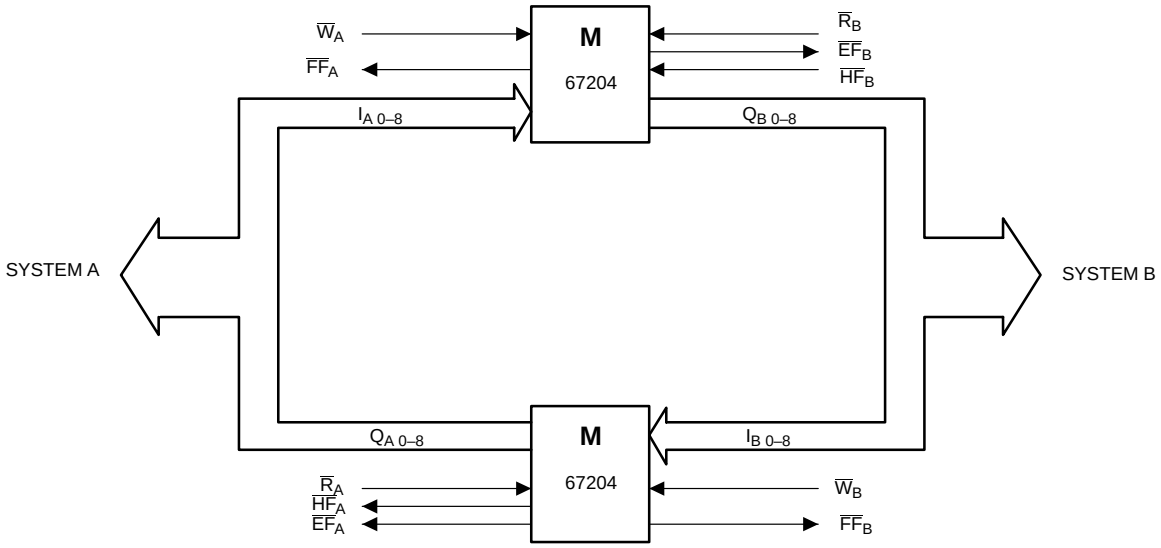


Figure 5. Compound FIFO Expansion.



Notes : 6. For depth expansion block see section on Depth Expansion and Figure 4.
7. For Flag detection see section on Width Expansion and Figure 3.

Figure 6. Bidirectional FIFO Mode.



Electrical Characteristics

Absolute Maximum Ratings

Supply voltage (VCC – GND) . . . . . – 0.3 V to 7.0 V
Input or Output voltage applied : . . . . (GND – 0.3 V) to (Vcc + 0.3 V)
Storage temperature : . . . . . – 65 °C to + 150 °C

OPERATING RANGE	OPERATING SUPPLY VOLTAGE	OPERATING TEMPERATURE
Military	Vcc = 5 V ± 10 %	– 55 °C to + 125 °C

DC Parameters

Parameter	Description	M67204E – 40	M67204E – 50	UNIT	VALUE
$I_{CCOP\ (8)}$	Operating supply current	135	125	mA	Max
$I_{CCSB\ (9)}$	Standby supply current	1.5	1.5	mA	Max
$I_{CCPD\ (10)}$	Power down current	200	200	µA	Max

Notes : 8. Icc measurements are made with outputs open. F = F max
9. $\overline{R} = \overline{W} = \overline{RS} = \overline{FL/RT}$ = VIH.
10. All input = Vcc.

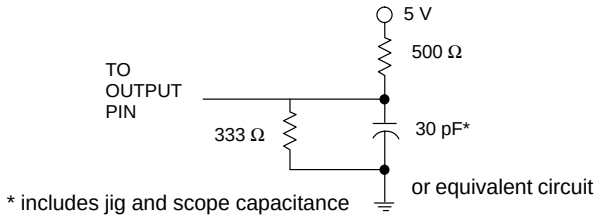
PARAMETER	DESCRIPTION	M67204E	UNIT	VALUE
ILI (11)	Input leakage current	± 1	µA	Max
ILO (12)	Output leakage current	± 1	µA	Max
VIL (13)	Input low voltage	0.8	V	Max
VIH (13)	Input high voltage	2.2	V	Min
VOL (14)	Output low voltage	0.4	V	Max
VOH (14)	Output high voltage	2.4	V	Min
C IN (15)	Input capacitance	8	pF	Max
C OUT (15)	Output capacitance	8	pF	Max

Notes : 11. 0.4 ≤ Vin ≤ Vcc.
12. $\overline{R}$ = VIH, 0.4 ≤ VOUT ≤ VCC.
13. VIH max = Vcc + 0.3 V. VIL min = –0.3 V or –1 V pulse width 50 ns
14. Vcc min, IOL = 8 mA, IOH = –2 mA.
15. Guaranteed but not tested

AC Test Conditions

Input pulse levels : Gnd to 3.0 V
Input rise/Fall times : 5 ns
Input timing reference levels : 1.5 V
Output reference levels : 1.5 V
Output load : See figure 7

Figure 7. Output Load.



SYMBOL (16)	SYMBOL (17)	PARAMETER (18) (22)	M67204E – 40		M67204E – 50		UNIT
			MIN.	MAX.	MIN.	MAX.	
READ CYCLE							
TRLRL	tRC	Read cycle time	50	–	65	–	ns
TRLQV	tA	Access time	–	40	–	50	ns
TRHRL	tRR	Read recovery time	10	–	15	–	ns
TRLRH	tRPW	Read pulse width (19)	40	–	50	–	ns
TRLQX	tRLZ	Read low to data low Z (20)	5	–	10	–	ns
TWHQX	tWLZ	Write low to data low Z (20, 21)	10	–	15	–	ns
TRHQX	tDV	Data valid from read high	5	–	5	–	ns
TRHQZ	tRHZ	Read high to data high Z (20)	–	25	–	30	ns
WRITE CYCLE							
TWLWL	tWC	Write cycle time	50	–	65	–	ns
TWLWH	tWPW	Write pulse width (19)	40	–	50	–	ns
TWHWL	tWR	Write recovery time	10	–	15	–	ns
TDVWH	tDS	Data set-up time	20	–	30	–	ns
TWHDX	tDH	Data hold time	0	–	0	–	ns
RESET CYCLE							
TRSLWL	tRSC	Reset cycle time	50	–	65	–	ns
TRSLRSH	tRS	Reset pulse width (19)	40	–	50	–	ns
TWHRSH	tRSS	Reset set-up time	40	–	50	–	ns
TRSHWL	tRSR	Reset recovery time	10	–	15	–	ns
RETRANSMIT CYCLE							
TRTLWL	tRTC	Retransmit cycle time	50	–	65	–	ns
TRTLRTH	tRT	Retransmit pulse width (19)	40	–	50	–	ns
TWHRTH	tRTS	Retransmit set-up time (20)	40	–	50	–	ns
TRTHWL	tRTR	Retransmit recovery time	10	–	15	–	ns
FLAGS							
TRSLEFL	tEFL	Reset to EF low	–	50	–	60	ns
TRSLFFH	tHFH, tFFH	Reset to HF/FF high	–	50	–	60	ns
TRLEFL	tREF	Read low to EF low	–	35	–	45	ns
TRHFFH	tRFF	Read high to FF high	–	35	–	45	ns
TEFHRH	tRPE	Read width after EF high	40	–	50	–	ns
TWHEFH	tWEF	Write high to EF high	–	35	–	45	ns
TWLFFL	tWFF	Write low to FF low	–	35	–	45	ns
TWLHFL	tWHF	Write low to HF low	–	50	–	60	ns
TRHHFH	tRHF	Read high to HF high	–	50	–	60	ns
TFFHWH	tWPF	Write width after FF high	40	–	50	–	ns

SYMBOL (16)	SYMBOL (17)	PARAMETER (18) (22)	M67204E – 40		M67204E – 50		UNIT
			MIN.	MAX.	MIN.	MAX.	
EXPANSION			PREVIEW				
TWLXOL	tXOL	Read/Write to XO low	–	40	–	50	ns
TWHXOH	tXOH	Read/Write to XO high	–	40	–	50	ns
TXILXIH	tXI	XI pulse width	40	–	50	–	ns
TXIHXIL	tXIR	XI recovery time	10	–	10	–	ns
TXILRL	tXIS	XI set-up time	10	–	15	–	ns

Notes : 16. STD symbol.
17. ALT symbol.
18. Timings referenced as in ac test conditions.
19. Pulse widths less than minimam value are not allowed.
20. Values guaranteed by design, not currently tested.
21. Only applies to read data flow-through mode.
22. All parameters tested only.

Figure 8. Asynchronous Write and Read Operation.

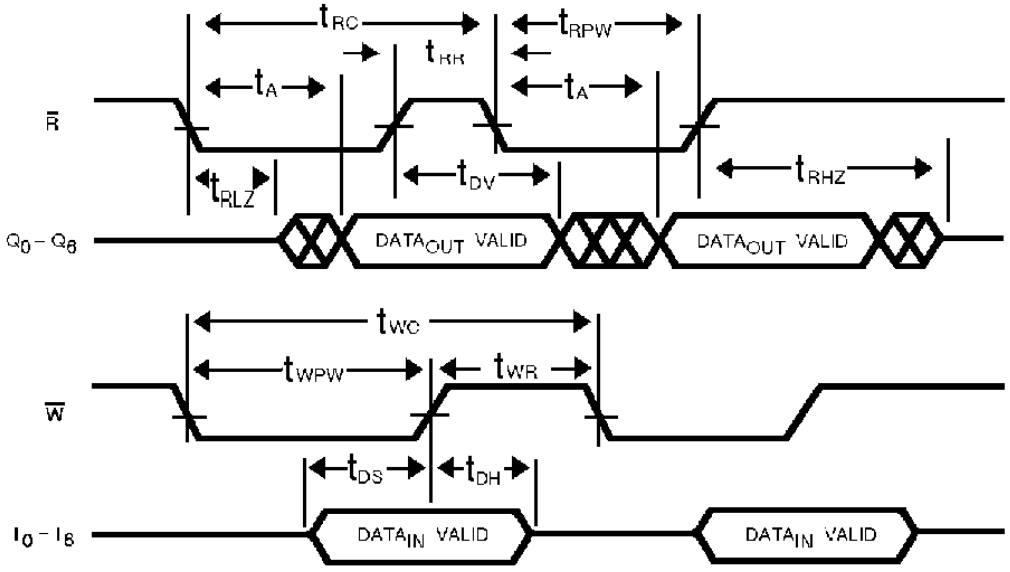


Figure 9. Full Flag from Last Write to First Read.

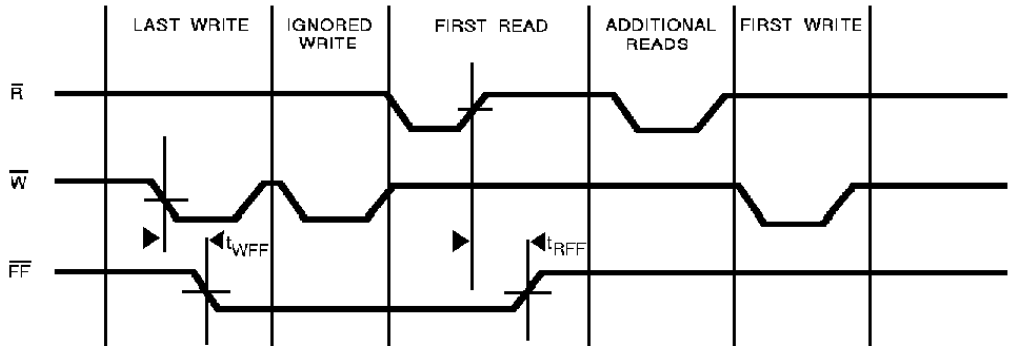


Figure 10. Empty Flag from Last Read to First Write.

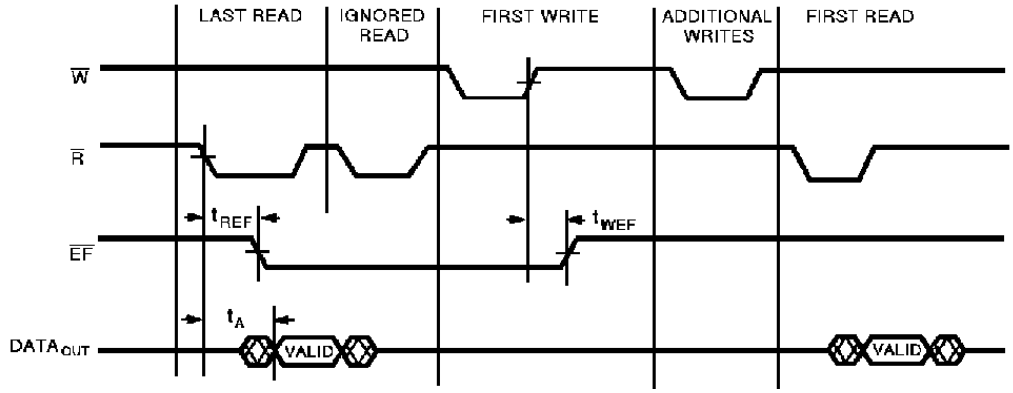
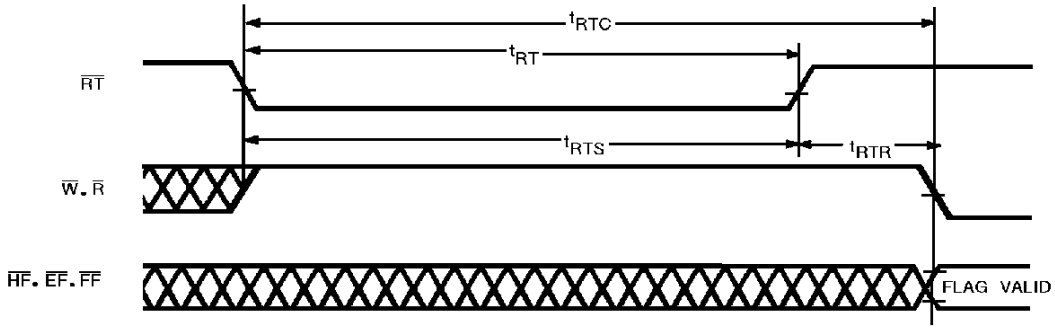


Figure 11. Retransmit.



Notes : 23. $\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during Retransmit, but flags will be valid at t_{RTC}.

Figure 12. Empty Flag Timing

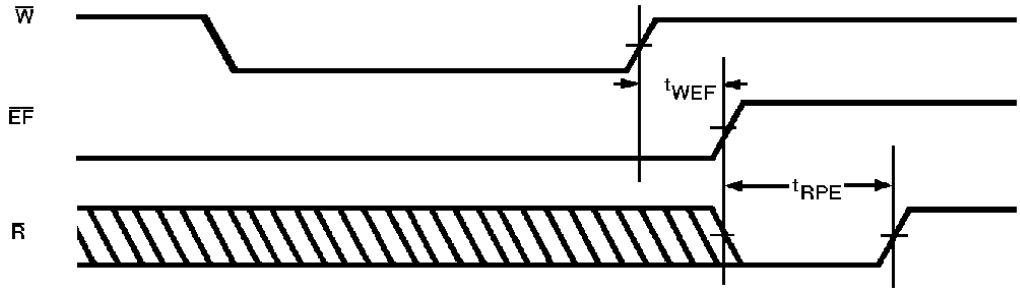


Figure 13. Full Flag Timing

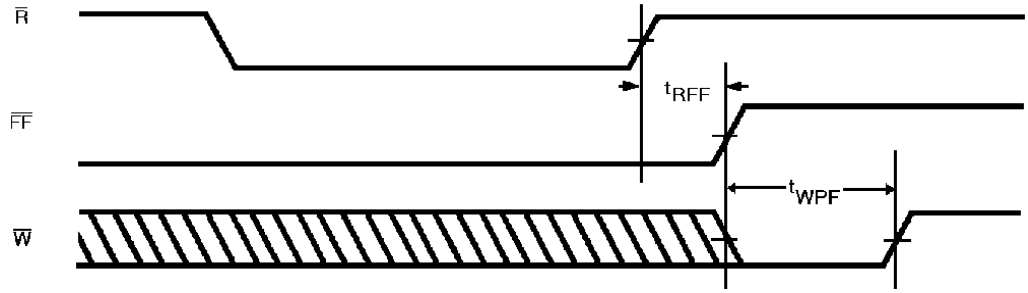


Figure 14. Half-Full Flag Timing.

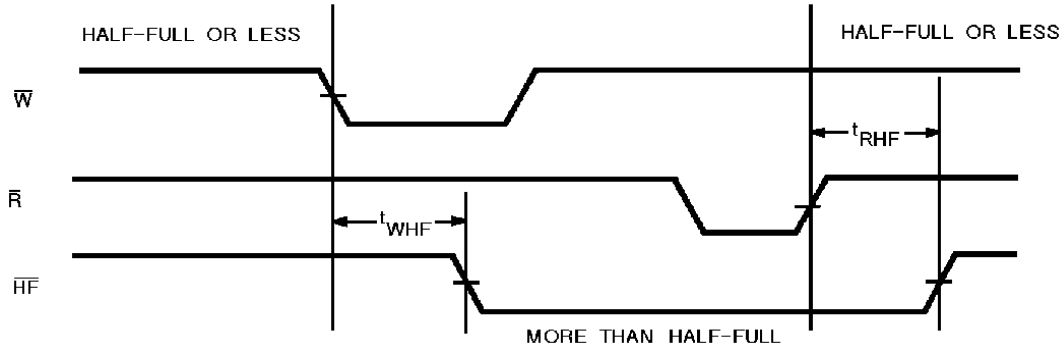


Figure 15. Expansion Out.

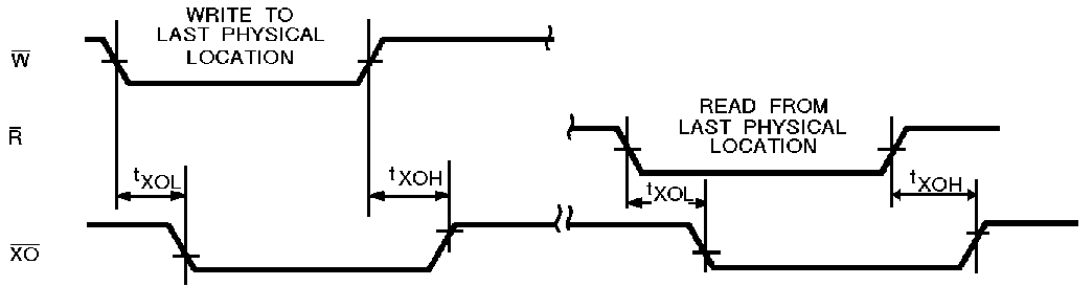


Figure 16. Expansion In.

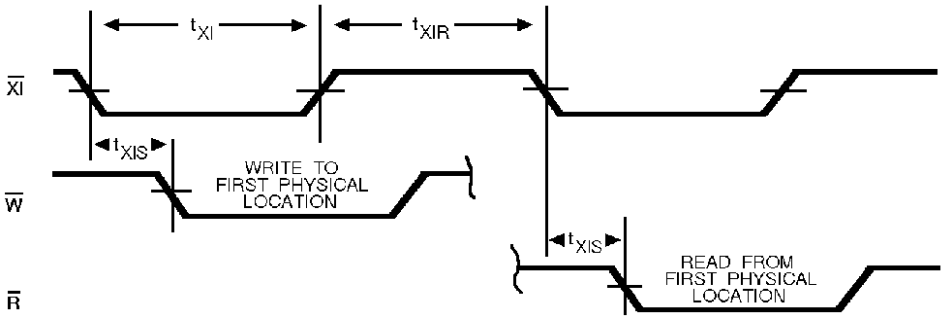


Figure 17. Read Data Flow – Through Mode.

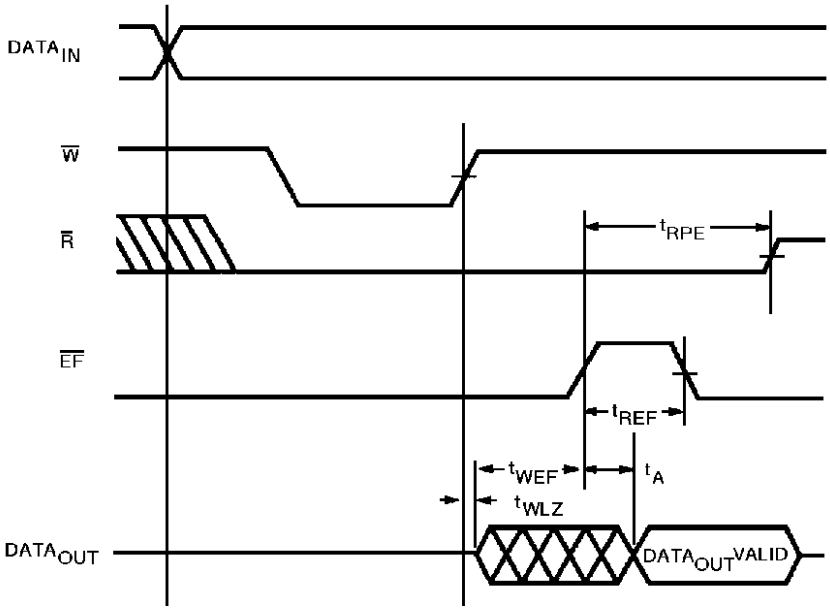
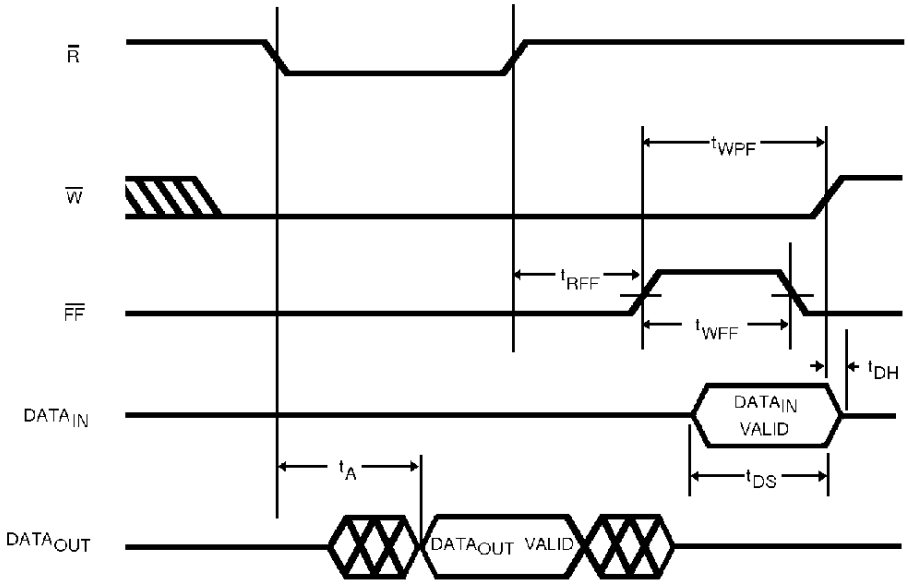


Figure 18. Write Data Flow – Through Mode.



Ordering Information

TEMPERATURE RANGE	PACKAGE	DEVICE	SPEED	FLOW*
M	M	DP	67204EV	40	/883

M = 5 V version

DP = 28 pin FP 400 mils
CP = Side brazed 28 pins 300 mils
0 = Dice form

40 ns
50 ns

blank	=	MHS standards
/883	=	MIL STD 883 Class B or S
SB/SC	=	SCC 9000 level B/C

M = Military
S = Space

–55° to +125°C
–55° to +125°C

67204E = 4096 × 9 FIFO
EV = Very low power Rad Tolerant

* For ordering in QML quality level, use the QML PIN according to SMD nº 5962–89568.