Data Sheet | January 3, 2006 | FN9162.1

Multiphase Core Regulator for IMVP-6 Mobile CPUs

The ISL6260 and ISL6260B provide microprocessor core voltage regulation by driving up to 3 channels in parallel. The multiphase buck converter architecture uses interleaved channels to multiply the output voltage ripple frequency and reduce output channel currents. The reduction in ripple results in fewer components, lower component cost, reduced power dissipation, and smaller implementation area. The ISL6260, ISL6260B multiphase controller together with the ISL6208 gate drivers form the basis for a portable power supply solution to power Intel's next generation mobile microprocessors. The modulator at the heart of this power system is derived from Intersil's Robust Ripple Regulator technology, (R^3) Compared with the traditional multiphase buck regulator, the R^3 technology multiphase converter has faster transient response. This is due to the R^3 modulator commanding variable switching frequency during load transients.

Intel Mobile Voltage Positioning is a smart voltage regulation technology, which effectively reduces power dissipation in Intel Pentium processors. The ISL6260 and ISL6260B support the IMVP-6 mobile processor voltage regulation specifications. ISL6260 and ISL6260B are pin-to-pin compatible. ISL6260B responds to PSI# signal by adding or dropping PWM2 and adjusting overcurrent protection accordingly. To improve audible noise, the DPRSLPVR signal can be used to reduce slew rates entering and exiting Deeper Sleep.

The ISL6260 and ISL6260B have several other key features. Current sensing can be done using either DCR sensing or discrete precision resistor sensing. A single NTC thermistor thermally compensates both the gain and time constant of the DCR variation. A unity gain, differential amplifier is provided for remote CPU die sensing. This allows the voltage on the CPU die to be accurately measured and regulated per Intel IMVP-6 specifications.

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-FREE)	PKG. DWG. #
ISL6260CRZ	ISL6260CRZ	-10 to 100	40 Ld 6x6 QFN	L40.6x6
ISL6260CRZ-T	ISL6260CRZ	-10 to 100	40 Ld 6x6 QFN	L40.6x6
ISL6260BCRZ	ISL6260BCRZ	-10 to 100	40 Ld 6x6 QFN	L40.6x6
ISL6260BCRZ-T	ISL6260BCRZ	-10 to 100	40 Ld 6x6 QFN	L40.6x6

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

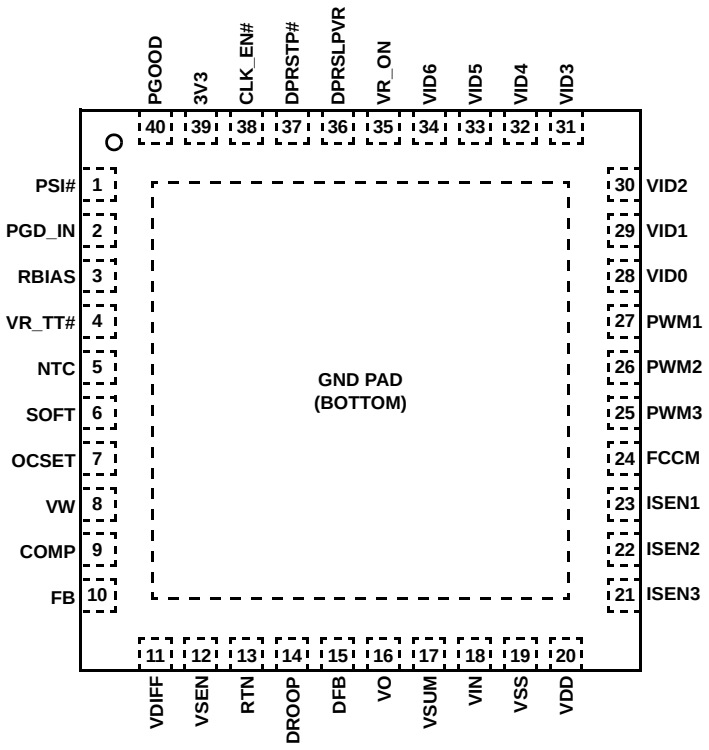
- Precision Multiphase Core Voltage Regulation
  - 0.5% System Accuracy Over Temperature
  - Enhanced Load Line Accuracy
- Microprocessor Voltage Identification Input
  - 7-Bit VID Input
  - 0.300V to 1.500V in 12.5mV Steps
  - Supports VID Changes On-The-Fly
- Multiple Current Sensing Approaches Supported
  - Lossless DCR Current Sensing
  - Precision Resistive Current Sensing
- Supports PSI# and Narrow VDC for Enhanced Battery Life (EBL) Initiatives
- Superior Noise Immunity and Transient Response
- Thermal Monitor
- Differential Remote Voltage Sensing
- High Efficiency Across Entire Load Range
- Programmable 1, 2 or 3 Power Channels
- Balanced Channel Loading Including Transients
- Small Footprint QFN 40 Lead 6x6 Package
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

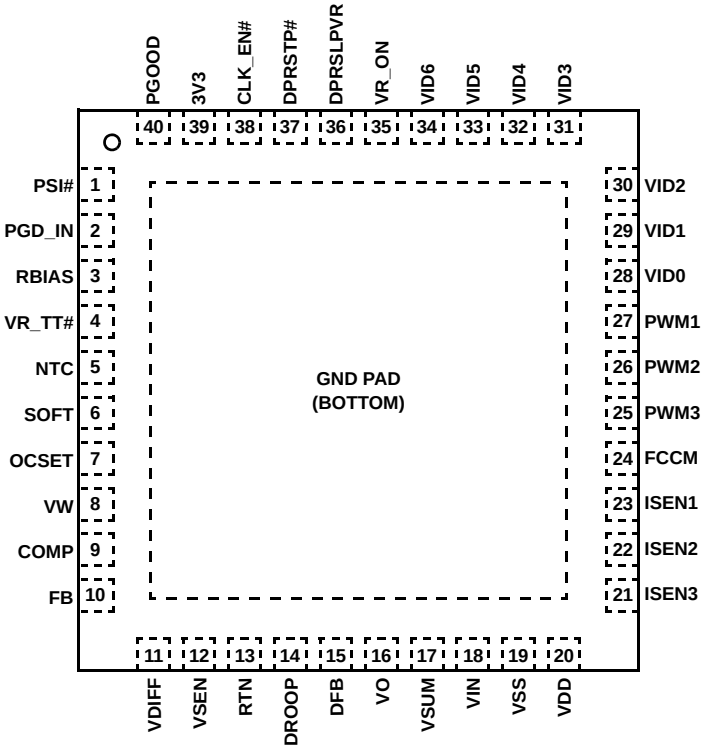
- Mobile laptop computers

Pinout

ISL6260CRZ, ISL6260BCRZ (QFN)
TOP VIEW



Functional Pin Description



PSI#

Low load current indicator input. When asserted low, indicates a reduced load-current condition. For ISL6260B, when PSI# is asserted low, PWM2 will be disabled.

PGD_IN

Digital Input. When asserted high, indicates VCCP and VCC_MCH voltages are within regulation. PGD_IN signal high is needed for the CLK_EN# to be low and PGOOD to be high.

RBIAS

147K Resistor to VSS sets internal current reference.

VR_TT#

Thermal overload output indicator.

NTC

Thermistor input to VRTT# circuit.

SOFT

A capacitor from this pin to Vss sets the maximum slew rate of the output voltage. Soft pin is the non-inverting input of the error amplifier.

OCSET

Overcurrent set input. A resistor from this pin to VO sets DROOP voltage limit for OC trip. A 10µA current source is connected internally to this pin.

VW

A resistor from this pin to COMP programs the switching frequency. (7kΩ gives approximately 300kHz). VW pin sources current.

COMP

This pin is the output of the error amplifier.

FB

This pin is the inverting input of error amplifier.

VDIFF

This pin is the output of the differential amplifier.

VSEN

Remote core voltage sense input. Connect to micro-processor die.

RTN

Remote voltage sensing return. Connect to ground at micro-processor die.

DROOP

Output of droop amplifier. Output = VO + DROOP.

DFB

Inverting input to droop amplifier.

VO

An input to the IC that reports the local output voltage.

VSUM

This pin is connected to the current summation junction.

VIN

Battery supply voltage, used for feed forward.

VSS

Signal ground; Connect to local controller ground.

VDD

5V bias power.

ISEN3

Individual current sensing for channel 3.

ISEN2

Individual current sensing for channel 2.

ISEN1

Individual current sensing for channel 1.

FCCM

Forced Continuous Conduction Mode (FCCM) enable pin to MOSFET drivers. It will disable diode emulation.

PWM3

PWM output for channel 3.

PWM2

PWM output for channel 2. For ISL6260B, PSI# low will make this output tri-state.

PWM1

PWM output for channel 1.

VID0, VID1, VID2, VID3, VID4, VID5, VID6

VID input with VID0 = LSB.

CLK_EN#

Digital output to enable System PLL Clock; Goes active 10µs after PG_IN is active and Vcore is within 10% of Boot Voltage.

PGOOD

Power Good open-drain output. Will be pulled up externally by a 680Ω resistor to VCCP or 1.9kΩ to 3.3V.

3V3

3.3V supply voltage for CLK_EN# logic, such an implementation will improve power consumption from 3.3V compared to open drain circuit other wise.

VR_ON

Voltage Regulator enable input. A high level logic signal on this pin enables the regulator.

DPRSLPVR

Deeper Sleep Enable signal. A high level logic signal on this pin indicates that the micro-processor is in Deeper Sleep Mode and indicates that slow entry and exit from C4 should occur. DPRSLPVR low indicates large charging or discharging soft pin current, and therefore fast output voltage transitions.

DPRSTP#

Deeper Sleep Enable signal. A low level logic signal on this pin indicates that the micro-processor is in Deeper Sleep Mode.

Absolute Maximum Ratings

Supply Voltage, VDD . . . . . -0.3 - +7V
Battery Voltage, VIN. . . . . +25V
Open Drain Outputs, PGOOD, VR_TT# . . . . . -0.3 - +7V
ALL OTHER PINS . . . . . -0.3V to (VDD + 0.3V)

Operating Conditions

Temperature Range . . . . . -10°C to 100°C
Supply Voltage Range (Typical). . . . . +5V ±5%

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package (Notes 1, 2)	30	5.5

Maximum Junction Temperature . . . . . 150°C
Storage Temperature . . . . . -65°C to +150°C
Maximum Lead Temperature (Soldering, 10s). . . . . +300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Operating Conditions: VDD = 5V, T_A = -10°C to +100°C, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT POWER SUPPLY						
+5V Supply Current	I_{VDD}	VR_ON = 3.3V		2.9	3.5	mA
		VR_ON = 0V			1	µA
+3.3V Supply Current	I_{3V3}	No load on CLK_EN#			1	µA
Battery Supply Current	I_{VIN}	VR_ON = 0V			1	µA
VIN Input Resistance	R_{VIN}	VR_ON = 3.3V		900		kΩ
Power-On-Reset Threshold	POR_r	V_{DD} rising		4.35	4.5	V
	POR_f	V_{DD} falling	4.00	4.15		V
SYSTEM AND REFERENCES						
System Accuracy	%Error (V_{CC_CORE})	No load; closed loop, active mode range VID = 0.75V - 1.50V	-0.5		+0.5	%
		VID = 0.5V - 0.7375V	-8		+8	mV
		VID = 0.3 - 0.4875V	-15		+15	mV
V_{BOOT}			1.176	1.200	1.224	V
Maximum Output Voltage	$V_{CC\_CORE(max)}$	VID = [0000000]		1.500		V
Minimum Output Voltage	$V_{CC\_CORE(min)}$	VID = [1100000]		0.300		V
VID Off State		VID = [1111111]		0.0		V
R_{BIAS} Voltage		R_{BIAS} = 147kΩ	1.45	1.47	1.49	V
CHANNEL FREQUENCY						
Nominal Channel Frequency	$f_{SW(nom)}$	Rfset = 7kΩ, 3 channel operation, Vcomp = 2V	285	300	315	kHz
Adjustment Range		See Equation 4 Rfset selection	200		500	kHz
AMPLIFIERS						
Droop Amplifier Offset			-0.3		+0.3	mV
Error Amp DC Gain	A_{V0}			90		dB
Error Amp Gain-Bandwidth Product	GBW	C_L= 20pF		18		MHz
FB Input Current	$I_{IN(FB)}$			10	150	nA

Electrical Specifications Operating Conditions: VDD = 5V, T_A = -10°C to +100°C, unless otherwise noted. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ISEN						
Imbalance Voltage		Maximum of ISENs - Minimum of ISENs			2	mV
Input Bias Current				20		nA
SOFT CURRENT						
Soft-start current	I_{SS}		-46	-41	-36	µA
SOFT Geyserville Current	I_{GV}	|SOFT-V_{DAC}| >100mV	±175	±200	±225	µA
SOFT Deeper Sleep Entry Current	I_{C4}	DPRSLPVR = 3.3V	-46	-41	-36	µA
SOFT Deeper Sleep Exit Current	I_{C4EA}	DPRSLPVR = 3.3V	36	41	46	µA
SOFT Deeper Sleep Exit Current	I_{C4EB}	DPRSLPVR = 0V	175	200	225	µA
POWER GOOD AND PROTECTION MONITORS						
PGOOD Low Voltage	V_{OL}	I_{PGOOD}= 4mA		0.26	0.4	V
PGOOD Leakage Current	I_{OH}	PGOOD = 3.3V	-1		1	µA
PGOOD Delay	tpgd	CLK_ENABLE# LOW to PGOOD HIGH	5.5	6.8	8.1	ms
Overvoltage Threshold	OV_H	VO rising above setpoint for >1ms	160	200	240	mV
Severe Overvoltage Threshold	OV_{HS}	VO rising for >2µs	1.675	1.7	1.725	V
OCSET Reference Current		I(Rbias) = 10µA	9.8	10	10.2	µA
OC Threshold Offset		DROOP rising above OCSET for >150µs	-2		4	mV
Current Imbalance Threshold		One ISEN above another ISEN for >1.2ms		9		mV
Undervoltage Threshold (VDIFF/SOFT)	UV_f	VO falling below setpoint for >1.2ms	-355	-295	-235	mV
LOGIC THRESHOLDS						
VR_ON, DPRSLPVR and PGD_IN Input Low	$V_{IL(3.3V)}$				1.0	V
VR_ON, DPRSLPVR and PGD_IN Input High	$V_{IH(3.3V)}$		2.3			V
VID0-VID6, PSI#, DPRSTP# Input Low	$V_{IL(1.0V)}$				0.3	V
VID0-VID6, PSI#, DPRSTP# Input High	$V_{IH(1.0V)}$		0.7			V
PWM						
PWM (PWM1-PWM3) Output Low	$V_{OL(5.0V)}$	Sinking 5mA			1.0	V
FCCM Output Low	V_{OL_FCCM}	Sinking 3mA			1.0	V
PWM (PWM1-PWM3) and FCCM Output High	$V_{OH(5.0V)}$	Sourcing 5mA	3.5			V
PWM Tri-State Leakage		PWM = 2.5V	-1		1	µA
THERMAL MONITOR						
NTC Source Current		NTC = 1.3V	53	60	67	µA
Over-Temperature Threshold		V (NTC) falling	1.165	1.18	1.2	V
VR_TT# Low Output Resistance	R_{TT}	I = 20mA		6.5	9	Ω
CLK_EN# OUTPUT LEVELS						
CLK_EN# High Output Voltage	V_{OH}	3V3 = 3.3V, I = -4mA	2.9	3.1		V
CLK_EN# Low Output Voltage	V_{OL}	I = 4mA		0.26	0.4	V

Typical Operating Performance 3 Phase, DCR Sense, (1) 7821, (2) 7832 per phase, 300kHz, 0.5µH

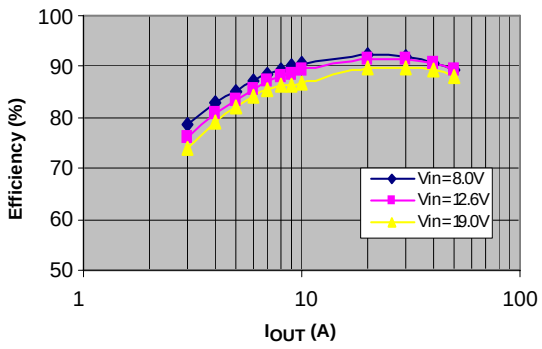


FIGURE 1. ACTIVE MODE EFFICIENCY, 3 PHASE, CCM, PSI# = HIGH, VID = 1.4375V

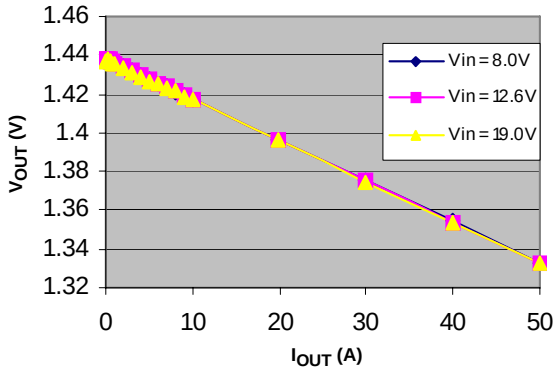


FIGURE 2. ACTIVE MODE LOAD LINE, 3 PHASE, CCM, PSI# = HIGH VID= 1.435V

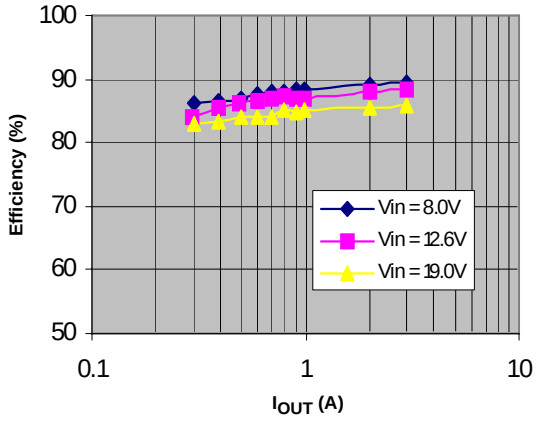


FIGURE 3. DEEPER SLEEP MODE EFFICIENCY, 3 PHASE, DCM OPERATION, PSI# = LOW, VID = 1.4375V

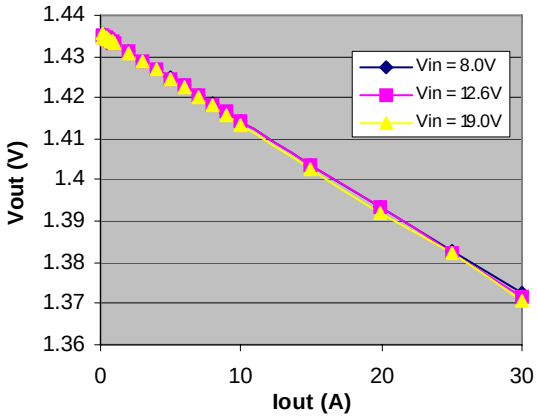


FIGURE 4. DEEPER SLEEP MODE LOAD LINE, 3 PHASE, CCM, PSI# = LOW VID= 1.435V

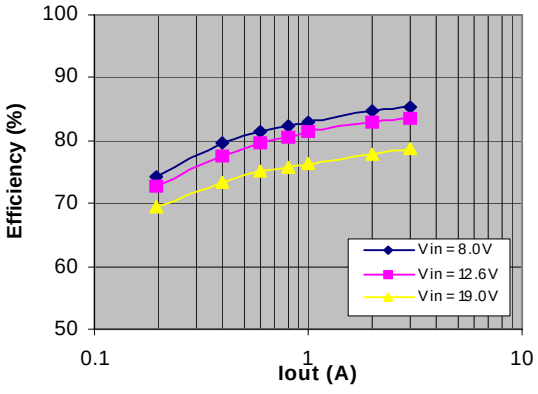


FIGURE 5. DEEPER SLEEP MODE EFFICIENCY, 3 PHASE, DCM OPERATION, PSI# = LOW, VID = 0.75V

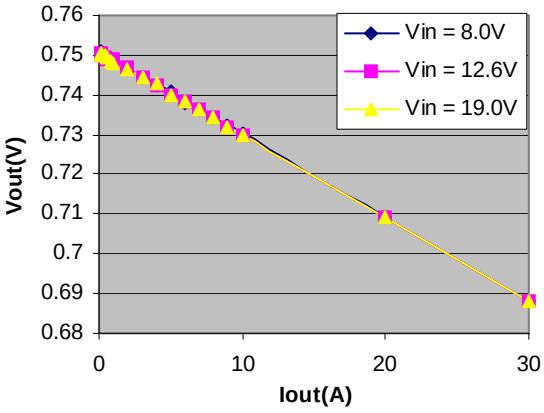


FIGURE 6. DEEPER SLEEP MODE LOAD LINE, 3 PHASE, DCM OPERATION, PSI# = LOW, VID = 0.75V

Typical Operating Performance 3 Phase, DCR Sense, (1) 7821, (2) 7832 per phase, 300kHz, 0.5µH (Continued)

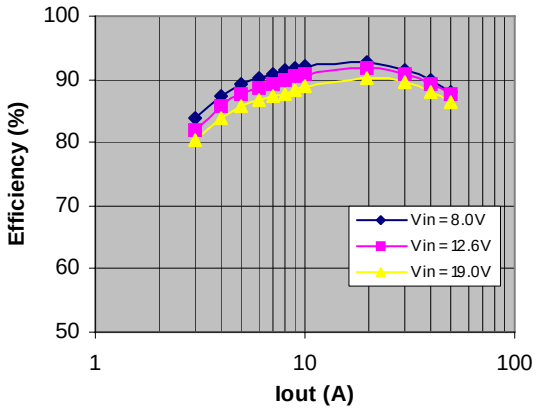


FIGURE 7. ACTIVE MODE EFFICIENCY, 2 PHASE, CCM, PSI# = HIGH, VID = 1.4375V

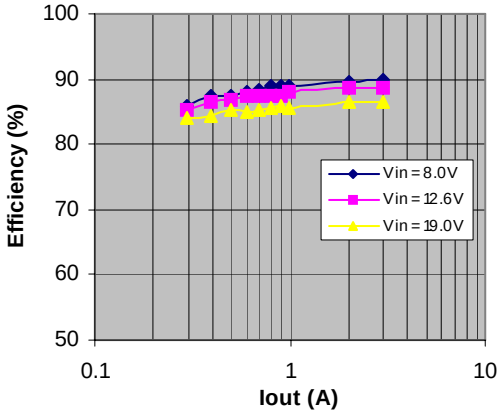


FIGURE 8. DEEPER SLEEP MODE EFFICIENCY, 2 PHASE, DCM OPERATION, PSI# = LOW, VID = 1.4375V

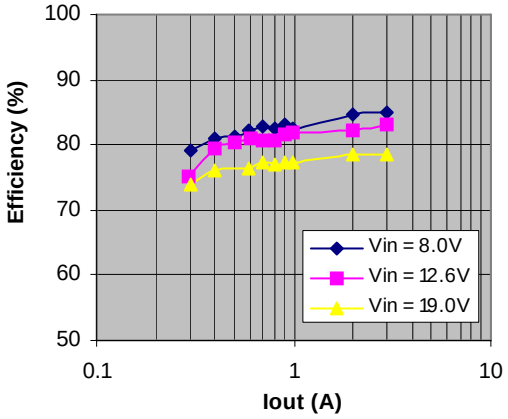


FIGURE 9. DEEPER SLEEP MODE EFFICIENCY, 2 PHASE, DCM OPERATION, PSI# = LOW, VID = 0.75V

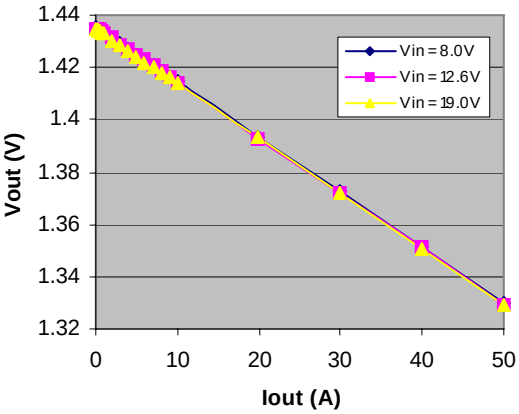


FIGURE 10. ACTIVE MODE LOAD LINE, 2 PHASE, CCM, PSI# = HIGH, VID = 1.435V

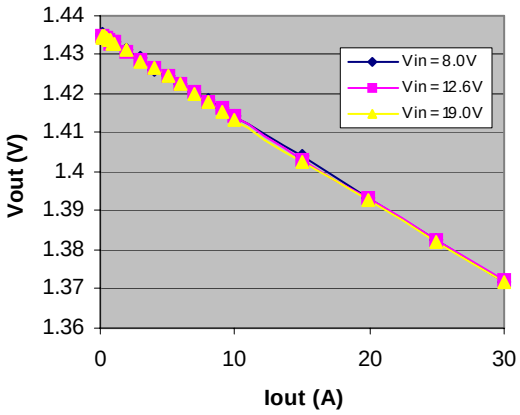


FIGURE 11. DEEPER SLEEP MODE LOAD LINE, 2 PHASE, DCM OPERATION, PSI# = LOW, VID = 1.4375V

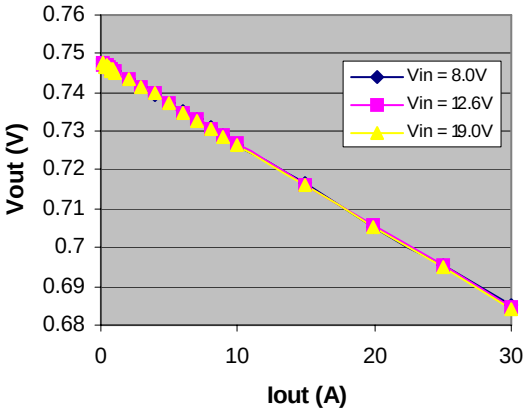


FIGURE 12. DEEPER SLEEP MODE LOAD LINE, 2 PHASE, DCM OPERATION, PSI# = LOW, VID = 0.75V

Typical Operating Performance

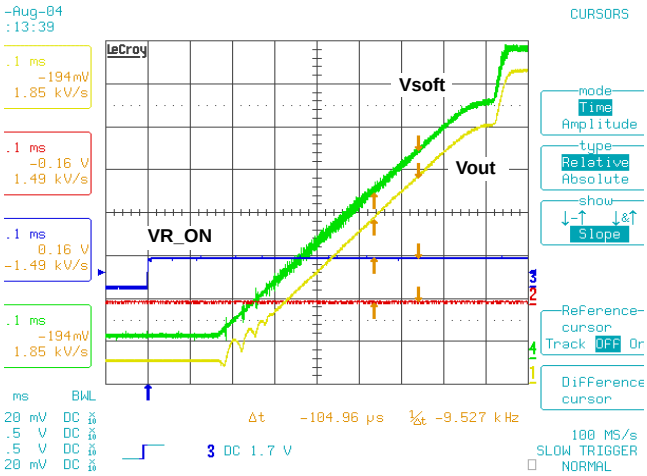


FIGURE 13. SOFT-START WAVEFORM SHOWING SLEW RATE OF 2mV/µs, 0V TO 1.2V (BOOT VOLTAGE)

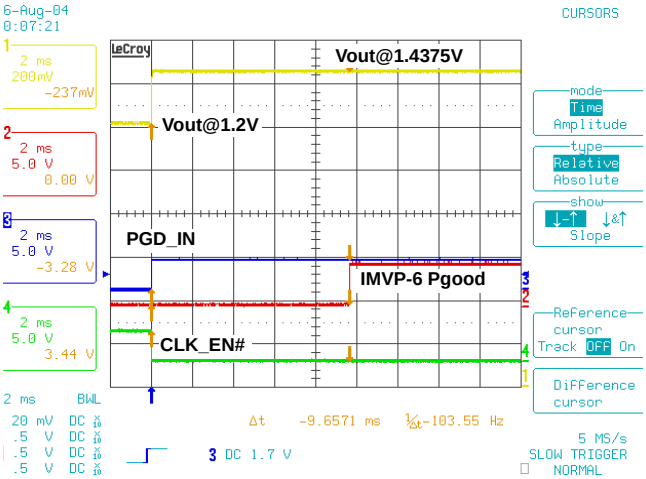


FIGURE 14. SOFT-START WAVEFORM SHOWING CLK_EN# AND IMVP-6 PGOOD

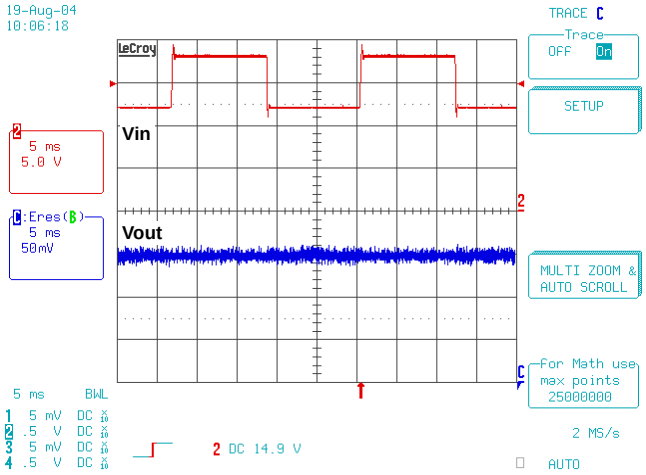


FIGURE 15. 12V-18V INPUT LINE TRANSIENT RESPONSE

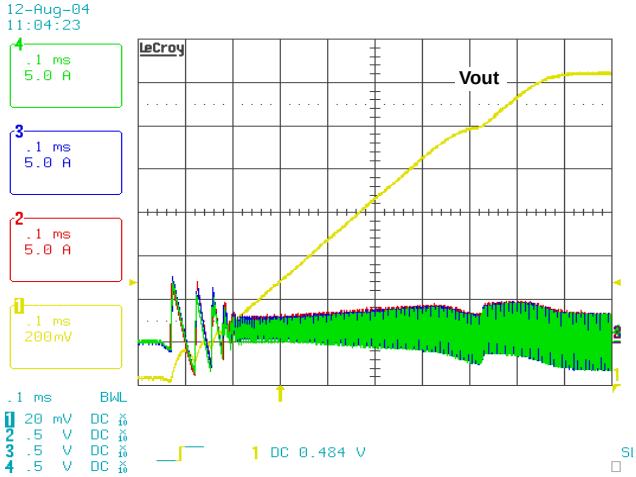


FIGURE 16. SOFT-START INRUSH CURRENT, V_{IN} = 8V

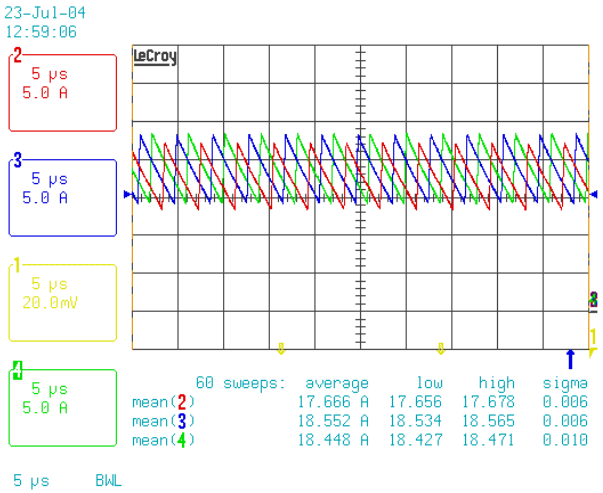


FIGURE 17. 3 PHASE CURRENT BALANCE, FULL LOAD = 50A

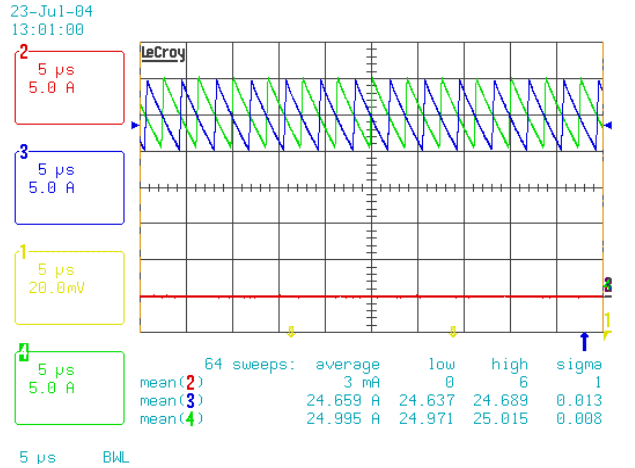


FIGURE 18. 2 PHASE CURRENT BALANCE, FULL LOAD = 50A

Typical Operating Performance (Continued)

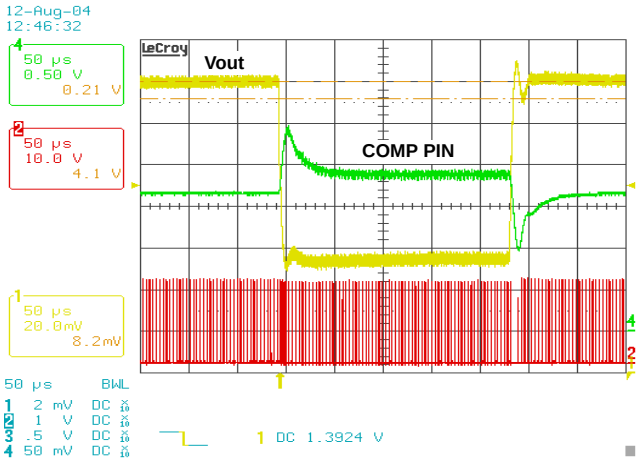


FIGURE 19. TRANSIENT LOAD RESPONSE, 40A LOAD STEP @ 200A/µs, 3 PHASE

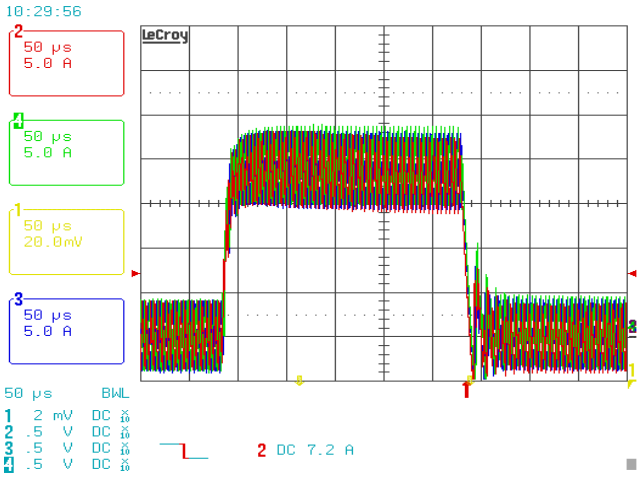


FIGURE 20. TRANSIENT LOAD 3 PHASE OPERATION - CURRENT BALANCE

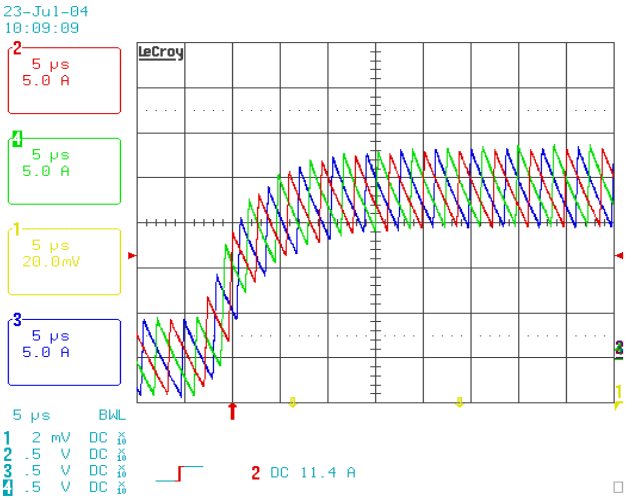


FIGURE 21. TRANSIENT LOAD 3 PHASE OPERATION, ZOOM OF RISING EDGE CURRENT BALANCE

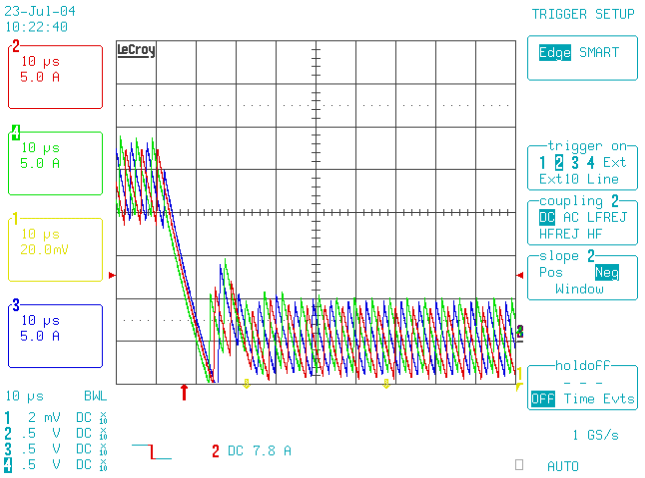


FIGURE 22. TRANSIENT LOAD 3 PHASE OPERATION, ZOOM OF FALLING EDGE CURRENT BALANCE

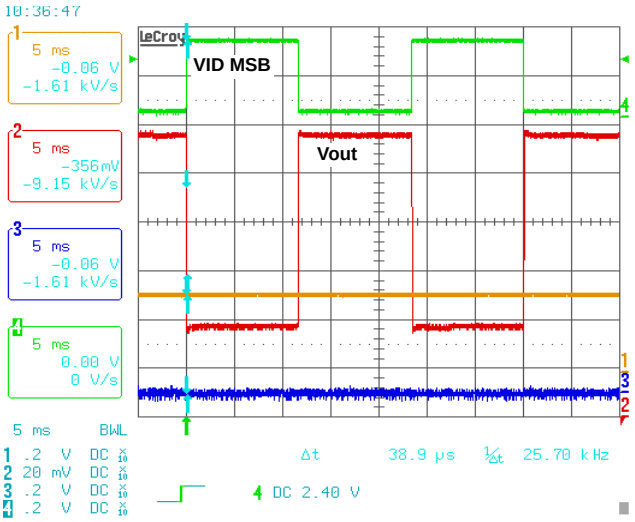


FIGURE 23. ISL6260, VID MSB BIT CHANGE FROM 1.4375V TO 0.65V SHOWING 9mV/µs SLEW RATE, DPRSLPVR = 0, DPRSTP# = 1

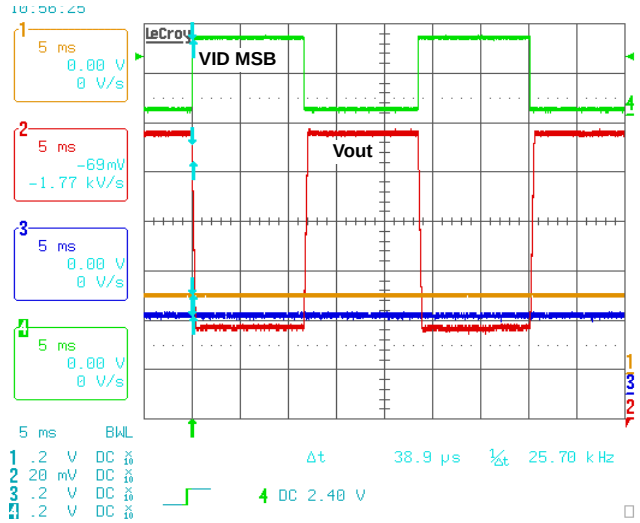


FIGURE 24. SLEW RATE ENTERING C4, VID MSB BIT CHANGE FROM 1.4375V TO 0.65V SHOWING 2mV/µs SLEW RATE, DPRSLPVR = 1, DPRSTP# = 0

Typical Operating Performance (Continued)

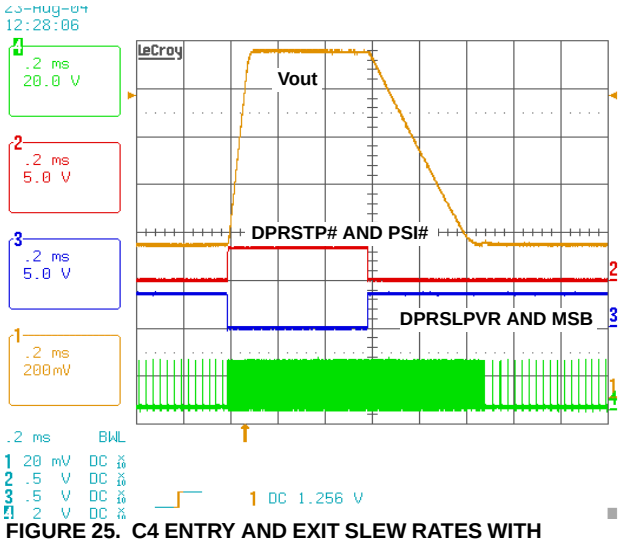


FIGURE 25. C4 ENTRY AND EXIT SLEW RATES WITH DPRSLPVR AND DPRSTP# (ISL6260)

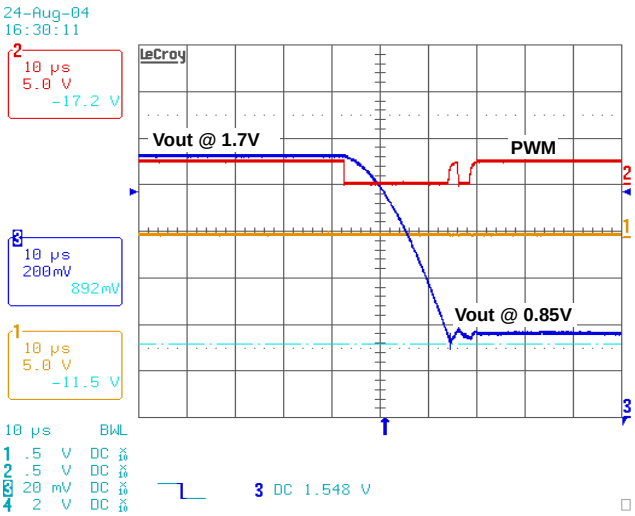


FIGURE 26. 1.7V OVP SHOWING OUTPUT PULLED LOW TO 0.85V AND PWM TRI_STATE

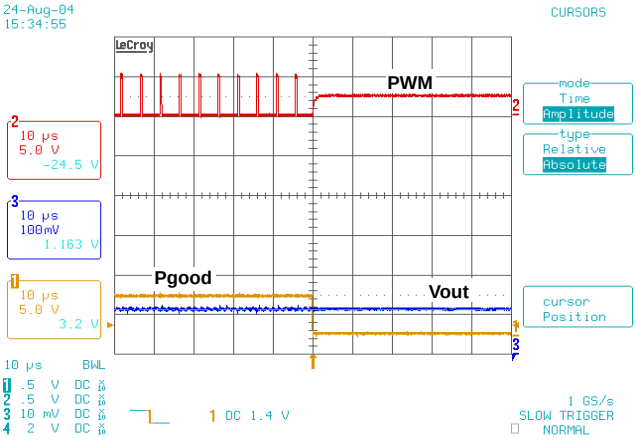


FIGURE 27. UNDERVOLTAGE RESPONSE SHOWING PWM TRI-STATE, VOUT < VID - 300mV

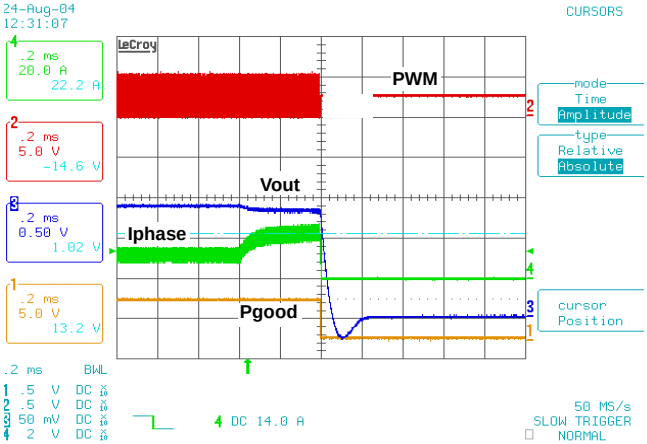


FIGURE 28. OCP - RESPONSE

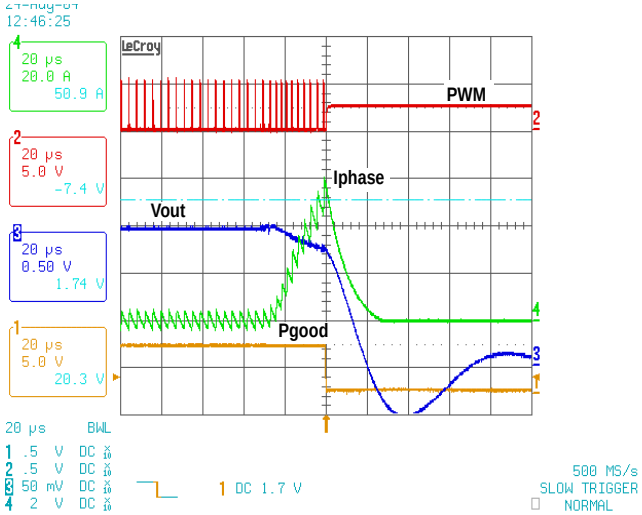


FIGURE 29. OCP - SHORT CIRCUIT PROTECTION

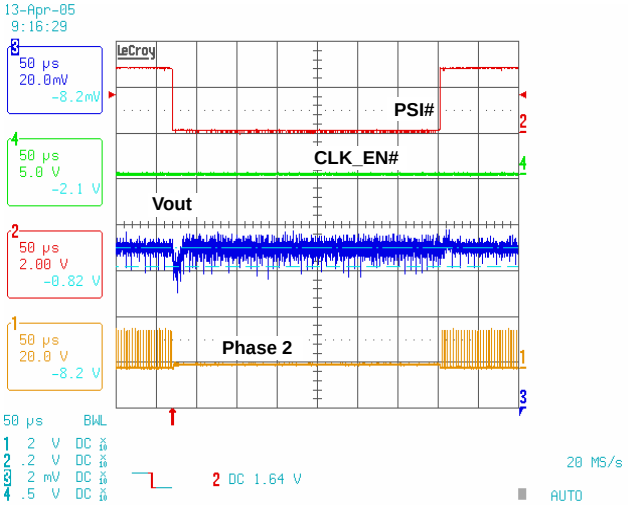


FIGURE 30. ISL6260B, PHASE ADDING AND DROPPING IN ACTIVE MODE, LOAD CURRENT = 15A

Typical Operating Performance (Continued)

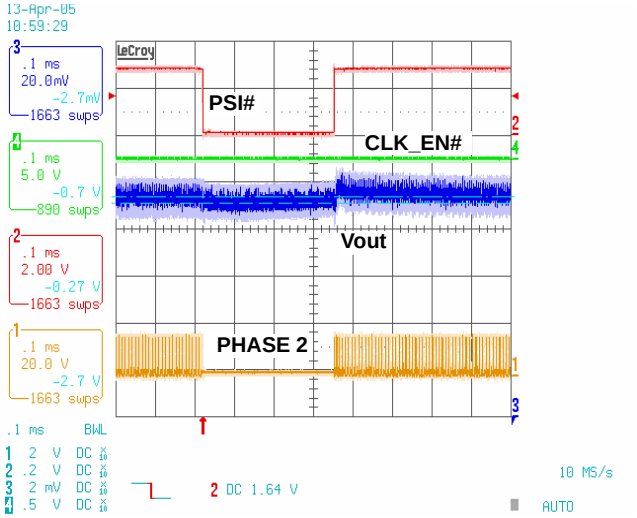


FIGURE 31. ISL6260B PHASE ADDING AND DROPPING IN DEEPER SLEEP MODE, LOAD CURRENT = 4.35A

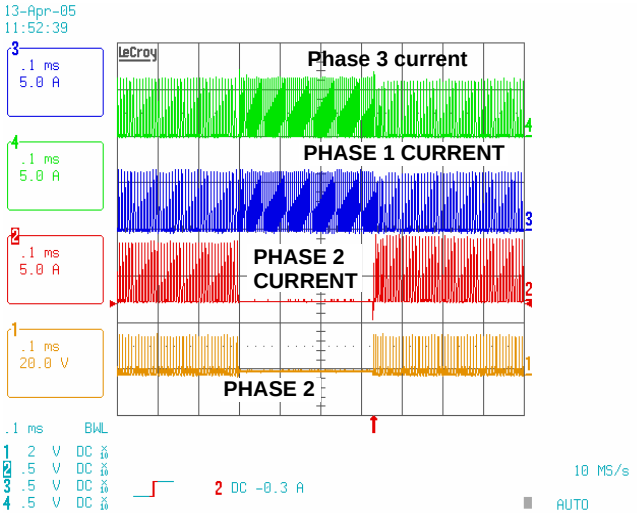


FIGURE 32. ISL6260B, INDUCTOR CURRENT WAVEFORM WITH PHASE ADDING AND DROPPING IN DCM OR DEEPER SLEEP MODE

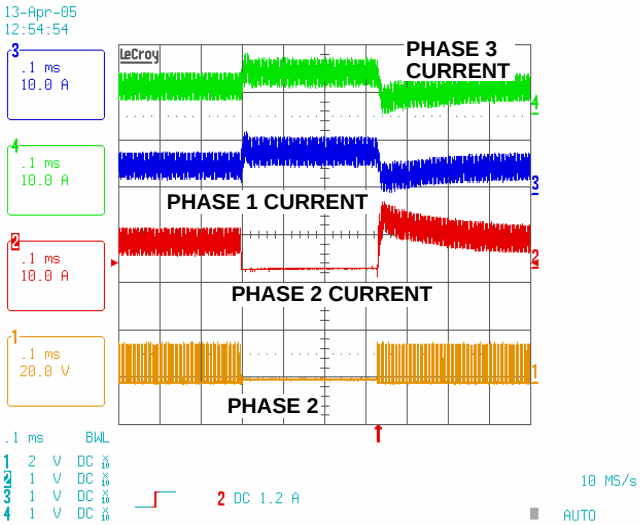


FIGURE 33. ISL6260B, INDUCTOR CURRENT WAVEFORM WITH PHASE ADDING AND DROPPING IN CCM OR ACTIVE MODE

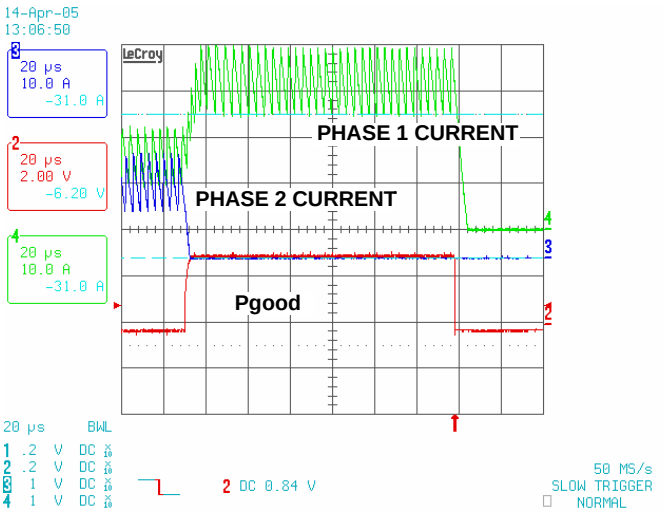


FIGURE 34. ISL6260B, OVERCURRENT DUE TO PHASE DROPPING

Simplified Application Circuit for DCR Current Sensing

Figure 35 shows a simplified application circuit for the ISL6260 or ISL6260B converter. Both the MOSFET driver IC and main control IC are shown. The driver has a force-continuous-conduction-mode (FCCM) input, that when disabled, allows the regulator to operate in Diode Emulation for improved light load efficiency.

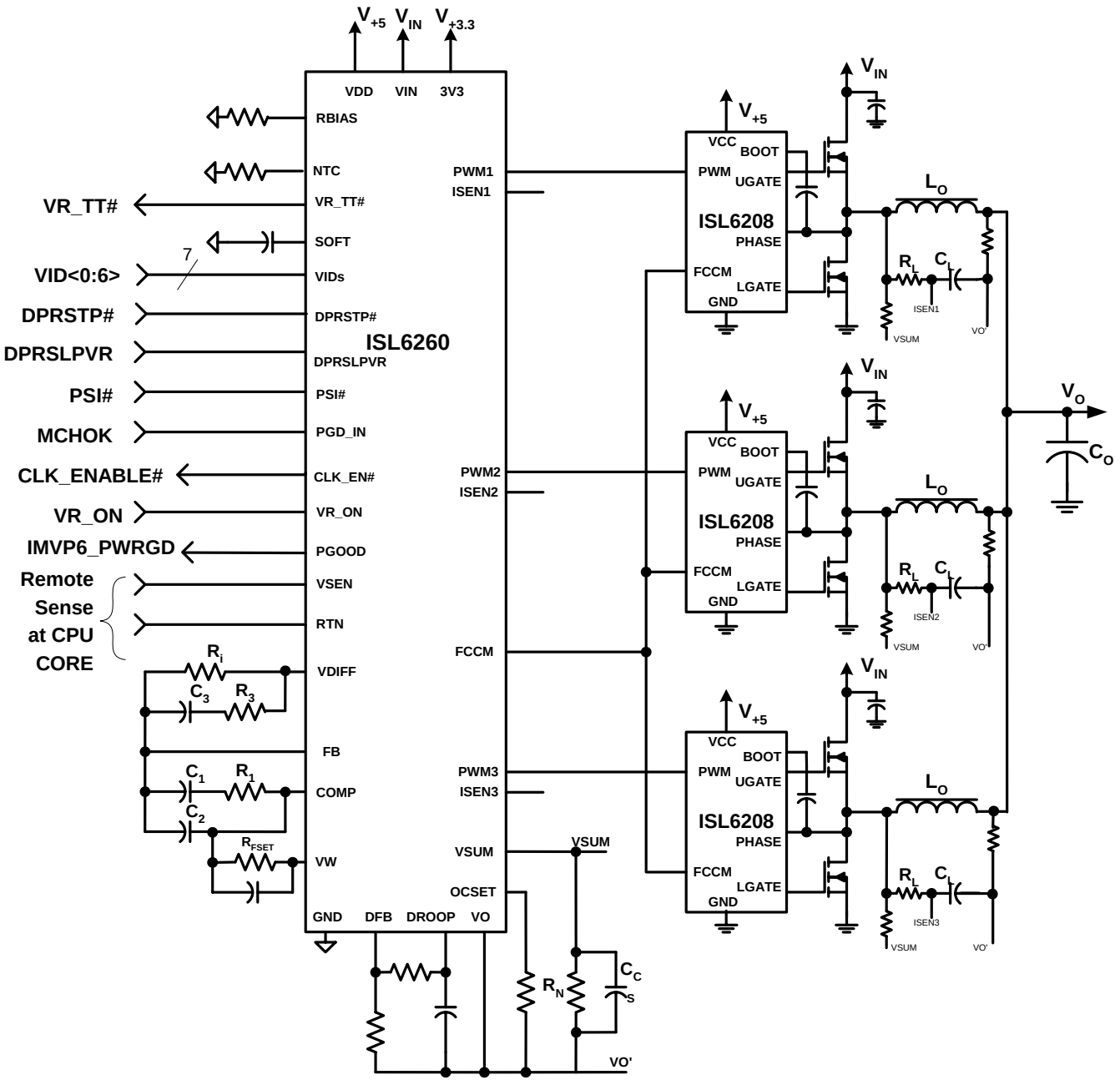


FIGURE 35. TYPICAL APPLICATION CIRCUIT FOR DCR SENSING

Simplified Application Circuit for Resistive Current Sensing

Figure 36 shows a simplified application circuit for the ISL6260 or ISL6260B converter. Both the MOSFET drivers and main control IC are shown. The driver has a force continuous-conduction-mode (FCCM) input, that when disabled, allows the regulator to operate in Diode Emulation for improved light load efficiency.

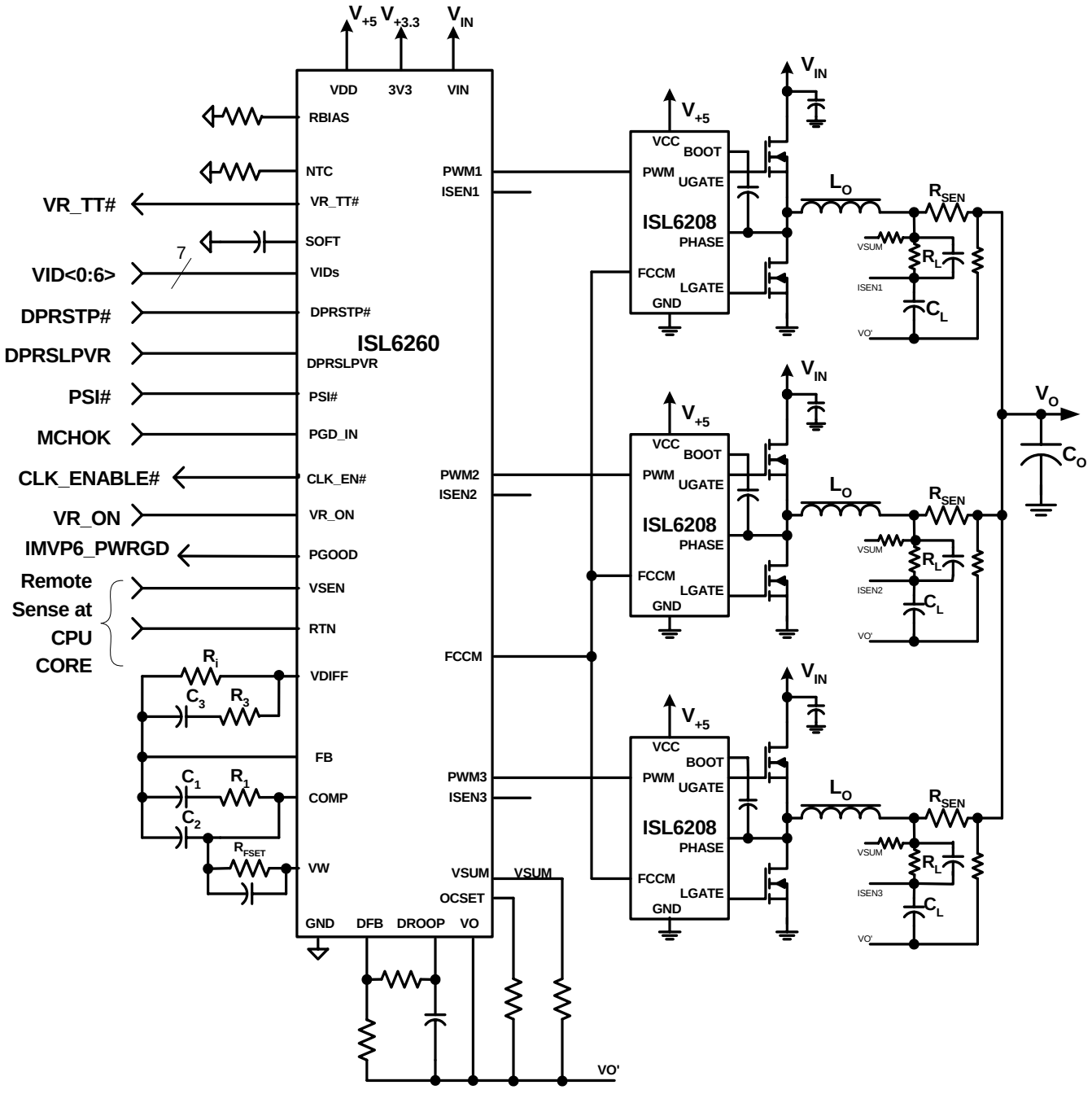


FIGURE 36. TYPICAL APPLICATION CIRCUIT FOR DISCRETE RESISTOR CURRENT SENSING

Functional Block Diagram

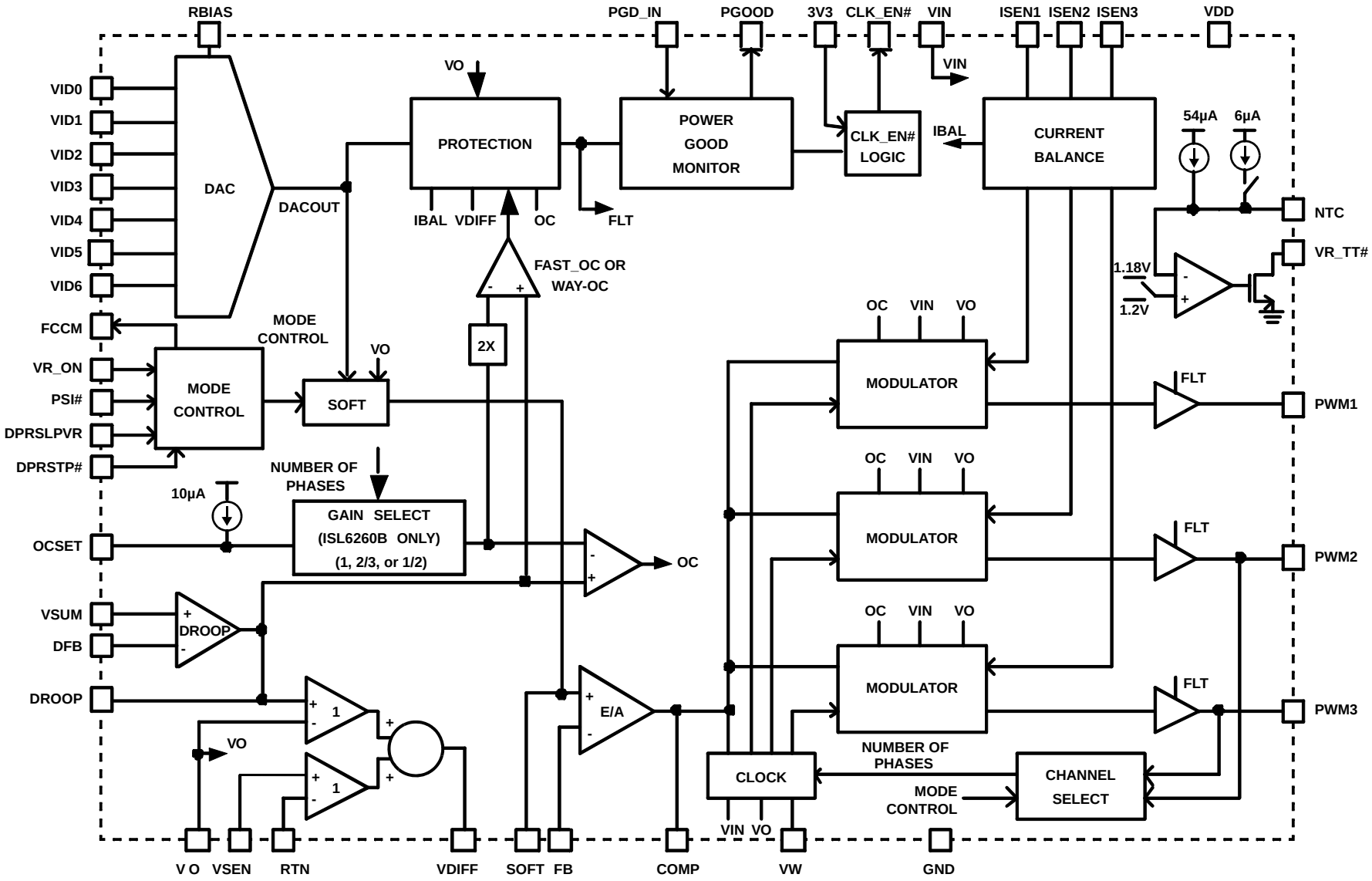


FIGURE 37. SIMPLIFIED BLOCK DIAGRAM

Theory of Operation

Operational Description

The ISL6260 and ISL6260B are multiphase regulators implementing Intel® IMVP-6 protocol. They can be programmed for one-, two- or three-channel operation for microprocessor core applications up to 70A. With their mating gate driver, the ISL6208, the SL6260 and ISL6260B give optimum steady-state and transient performance.

At the heart of the ISL6260 and ISL6260B is the patented R^3 (Robust Ripple Regulator®) modulator. The R^3® modulator combines the best features of fixed frequency PWM and hysteretic PWM while eliminating many of their shortcomings. The ISL6260 and ISL6260B modulator internally synthesize an analog of the inductor ripple currents and use hysteretic comparators on those signals to determine PWM pulse widths. Operating on these large-amplitude, noise-free synthesized signals allows the ISL6260 and ISL6260B to achieve lower output ripple and lower phase jitter than conventional hysteretic and fixed PWM controllers. Unlike conventional hysteretic converters, the ISL6260 and ISL6260B have an error amplifier that allows the controller to maintain a 0.5% voltage tolerance.

The hysteresis window voltage rides on the error amplifier output such that a load current transient results in an increase in switching frequency to give the R^3 regulator a faster response than conventional fixed frequency PWM controllers. The sharing of the hysteretic window voltage also inherently shares the transient load current between the phases. The individual average phase voltages are monitored and controlled to equally share the static current among the phases.

ISL6260B disables PWM2 when PSI# is asserted low. ISL6260 does not drop phase with PSI# signal.

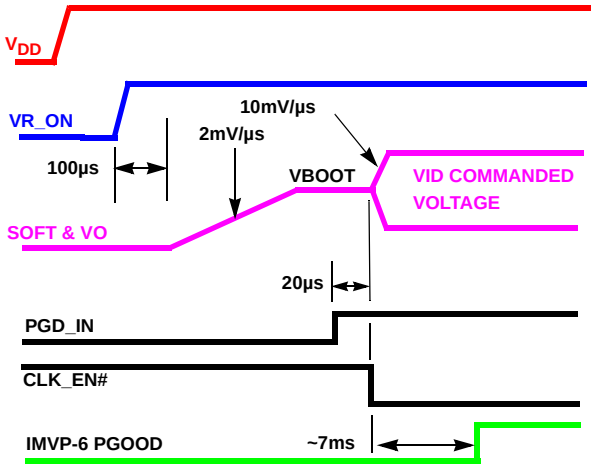


FIGURE 38. SOFT-START WAVEFORMS USING A 20nF SOFT CAPACITOR

Start-up Timing

With the controller's +5V VDD voltage above the POR threshold, the start-up sequence begins when VR_ON exceeds the 3.3V logic HIGH threshold. Approximately 100µs later SOFT and VOUT start ramping up to the boot voltage of 1.2V. During this interval, the SOFT capacitor is charged with approximately 40µA. Therefore, if the SOFT capacitor is selected to be 20nF, the SOFT ramp will be at about 2mV/µs for a soft-start time of 600µs. Once VOUT is within 10% of the boot voltage and PGD_IN is HIGH for six PWM cycles (20µs for frequency = 300kHz), then CLK_EN# is pulled LOW and the SOFT capacitor is charged up with approximately 200µA. Therefore, VOUT slews at +10mV/µs to the voltage set by the VID pins. Approximately seven milliseconds later, PGOOD is asserted HIGH. A typical start-up timing is shown in Figure 38. Similar results occur if VR_ON or PGD_IN or both are tied to VDD, with the soft-start sequence starting 120µs after VDD crosses the POR threshold.

PGD_IN - LATCH

It should be noted that PGD_IN going low will cause the converter to latch off. This state will be cleared when VR_ON is toggled. This feature allows the converter to respond to other system voltage outages immediately. For ISL6260B only, PGD_IN de-assertion (0) during normal operation will make CLK_EN# go high.

Static Operation

After the start sequence, the output voltage will be regulated to the value set by the VID inputs per Table 1. This Table is presented in its entirety in the Intel IMVP-6™ specification. The ISL6260, ISL6260B will control the no-load output voltage to an accuracy of ±0.5% over the range of 0.75V to 1.5V.

TABLE 1. TRUNCATED VID TABLE FOR INTEL IMVP-6™ SPECIFICATION

VID6	VID5	VID4	VID3	VID2	VID1	VID0	VOUT
0	0	0	0	0	0	0	1.500V
0	0	0	0	0	0	1	1.4875
0	0	0	0	1	0	1	1.4375
0	0	0	0	1	1	1	1.4125
0	0	0	1	0	0	0	1.4000
0	0	1	0	0	0	1	1.2875
0	0	1	1	0	0	0	1.2000
0	0	1	1	1	0	0	1.1500
0	1	0	1	0	0	0	1.0000
0	1	0	1	0	1	1	0.9625
0	1	1	1	1	0	0	0.7500
1	0	0	0	1	0	0	0.6500
1	0	1	0	0	0	0	0.5000
1	1	0	0	0	0	0	0.300
1	1	0	0	0	0	1	Off
1	1	0	0	0	1	0	Off
...							Off
1	1	1	1	1	1	0	Off
1	1	1	1	1	1	1	Off

A fully-differential amplifier allows CPU die voltage sensing for precise voltage control at the microprocessor die. The inputs to the amplifier are the VSEN and RTN pins.

As the load current increases from zero, the output voltage will droop from the VID table value by an amount proportional to current to achieve the IMVP-6 load line. The ISL6260 and ISL6260B provide for current to be measured using resistors in series with the channel inductors as shown in the application circuit of Figure 36 or using the intrinsic series resistance of the inductors as shown in the application circuit of Figure 35. In both cases, signals representing the inductor currents are summed at VSUM which is the non-inverting input to the DROOP amplifier shown in the block diagram of Figure 37. The voltage at the DROOP pin minus the output voltage, VO´ is thus a high-bandwidth analog of the total inductor current. This value is used as an input to the differential amplifier to achieve the IMVP-6 load line as well as the input to the overcurrent circuit.

When using inductor DCR current sensing, a single NTC element is used to compensate the positive temperature coefficient of the copper winding thus sustaining the load-line accuracy. Procedures to follow in determining component values are covered in the “Component Selection and Application” section of the datasheet.

In addition to the total current which is used for DROOP and OC, the individual channel average currents are also monitored and are used for balancing the load between the channels. The IBAL circuit will adjust the channel pulse-widths up or down relative to the other channels to cause the voltages presented to the ISEN pins to be equal.

The ISL6260 and ISL6260B controller can be configured for three-, two- or single-channel operation. To disable channel two and/or channel three, its PWM output pin should be tied to +5V VDD and the ISEN pins should be grounded. If the ISL6208 gate driver is populated in an unused channel, its PWM input pin should be opened in order to turn off its output. In three-channel operation, the three channel PWM's are 120 degrees apart, and in two-channel operation they are 180 degrees apart. The channel PWM frequency is determined by the value of RFSET as shown in the “Component Selection and Application” section of this document.

If the controller is kept in continuous conduction mode (CCM), the switching frequency may not be constant but it can maintain the switching ripple within spec. However, it will be very close to the set value at high input voltage and heavy load conditions. Selected by setting DPRSLPVR high, DPRSTP# low, together with PSI# signal (see Table 2), discontinuous conduction mode (DCM) is allowed. In DCM, the ISL6260, ISL6260B commands the ISL6208 to turn off the lower FET after its channel current decays to zero. As load is further reduced, channel switching frequency will drop, providing optimized efficiency even at light loading.

Dynamic Operation

Refer to Figure 39. The ISL6260 and ISL6260B respond to changes in VID command voltage by slewing to new voltages with a dV/dt set by the SOFT capacitor and by the state of DPRSLPVR. With CSOFT = 20nF and DPRSLPVR HIGH, the output voltage will move at ±2mV/µs for large changes in voltage. For DPRSLPVR LOW, the large signal dV/dt will be ±10mV/µs. As the output approaches the VID command voltage, the dV/dt rate moderates to prevent overshoot. During Geyserville III transitions where there is one LSB VID step each 5µs, the controller will follow the VID command with its dV/dt rate of ±2.5mV/µs.

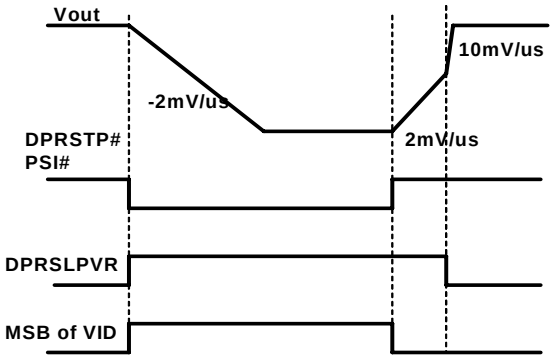


FIGURE 39. DEEPER SLEEP TRANSITION SHOWING DPRSLPVR's EFFECT ON EXIT SLEW RATE

Keeping DPRSLPVR HIGH during VID transitions will result in reduced dV/dt output voltage changes with resulting minimized audio noise. For fastest recovery from Deeper Sleep to Active mode, DPRSLPVR LOW achieves maximum dV/dt. Therefore, the ISL6260 and ISL6260B are IMVP-6 compliant for DPRSTP# and DPRSLPVR logic.

Intersil's R^3 intrinsically has voltage-feed-forward. High-speed input voltage steps result in insignificant output voltage perturbations. Refer to Figure 15 in the "Typical Operating Performance" section of this document for Input Transient Performance.

In response to load current step increases, the ISL6260 and ISL6260B will transiently raise the switching frequency so that response time is decreased and current is shared by all the channels.

Modes of Operation Programmed by Logic Signals

The operational modes of ISL6260 and ISL6260B are related to the control signals of DPRSLPVR, DPRSTP#, and PSI#. ISL6260B responds PSI# signal by adding or dropping PWM2 and adjusting the overcurrent protection level accordingly. ISL6260 does not drop phases while in operation. For example, if the ISL6260B is initially used as three phase, the PSI# signal will add or drop PWM2 and leave PWM1 and PWM3 always in operation. Meanwhile, after PWM2 is dropped, the phase shift between the PWM1 and PWM3 is adjusted from 120 degree to 180 degree and the overcurrent and the way-overcurrent protection level will be adjusted to 2/3 of the initial value. If the ISL6260B is initially used as two phase operation, it is suggested that PWM1 and PWM2 pair, not PWM1 and PWM3 pair, should be used such that PSI# signal will enable or disable PWM2 with PWM1 in operation always. The overcurrent and way-overcurrent protection level in two-to-one phase mode operation will be adjusted as two to one as well. For ISL6260B, the DCM mode is independent of PSI#, it just responds to the DPRSLPVR and DPRSTP#. The following table shows the operation modes of ISL6260 and ISL6260B with combinations of control logic.

When PSI# is de-asserted low, ISEN2 pin is connected to the ISEN pins of the operational phases internally to keep proper current balance and less current overshoot and undershoot when the disabled phase is enabled again.

TABLE 2. ISL6260 ISL6260B MODE OF OPERATIONS

	DPRS LPVR	DPR STP#	PSI#	ISL6260	ISL6260B	CPU MODE
IMVP-6 Logic	0	1	1	N phase CCM	N phase CCM	Active
	0	1	0	N phase CCM	N-1 phase CCM	Active
	1	0	1	N phase CCM	N phase DCM	Deeper sleep
	1	0	0	N phase DCM	N-1 phase DCM	Deeper sleep
Other Logic	0	0	1	N phase CCM	N phase CCM	
	0	0	0	N phase CCM	N-1 phase CCM	
	1	1	1	N phase CCM	N phase CCM	
	1	1	0	N phase CCM	N-1phase CCM	

Protection

The ISL6260 and ISL6260B provide overcurrent, overvoltage, and undervoltage protection. Overcurrent protection is tied to the voltage droop which is determined by the resistors selected as described in the "Component Selection and Application" section. After the load-line is set, the OCSET resistor can be selected to detect overcurrent at any level of droop voltage. For overcurrent less that twice the OCSET level, the overload condition must exist for 120µs in order to trip the OC fault latch. This is shown in Figure 28.

For overload exceeding twice the set level, the PWM outputs will immediately shut off and PGOOD will go low to maximize protection due to hard shorts. This protection was referred to as way-overcurrent.

In addition, excessive phase unbalance due to gate driver failure will be detected and will shut down the controller after 1ms. The phase unbalance is detected by the voltage on the ISEN pins if the difference is greater than 9mV.

Undervoltage protection is independent of the overcurrent limit. If the output voltage is less than the VID set value by 300mV or more, a fault will latch after 1ms in that condition. The PWM outputs will turn off and PGOOD will go low. This is shown in Figure 27. Note that most practical core regulators will have the overcurrent set to trip before the -300mV undervoltage limit.

There are two levels of overvoltage protection and response. For output voltage exceeding the set value by +200mV for 1ms, a fault is declared. All of the above faults have the same action taken: PGOOD is latched low and the upper and lower power FETs are turned off so that inductor current will decay through the FET body diodes. This condition can be reset by bringing VR_ON low or by bringing VDD below POR threshold. When these inputs are returned to their high operating levels, a soft-start will occur.

TABLE 3. SUMMARY OF THE FAULT PROTECTION AND RESET OPERATIONS OF ISL6260, ISL6260B

	FAULT DURATION PRIOR TO PROTECTION	PROTECTION ACTIONS	FAULT RESET
Overcurrent	120µs	PWMs tri-state, Pgood latched low	VR_ON toggle or VDD toggle
Way-Overcurrent	<2µs	PWMs tri-state, Pgood latched low	VR_ON toggle or VDD toggle
Overvoltage 1.7V	Immediately	Low side MOSFET on until Vcore <0.85V, then PWM tri-state, Pgood latched low.	VDD toggle
Overvoltage +200mV	1ms	PWMs tri-state, Pgood latched low	VR_ON toggle or VDD toggle
Undervoltage -300mV	1ms	PWMs tri-state, Pgood latched low	VR_ON toggle or VDD toggle
Phase Current Unbalance	1ms	PWMs tri-state, Pgood latched low	VR_ON toggle or VDD toggle
Over Temperature	Immediately	VR_TT# goes low	N/A

Refer to Figure 26. The second level of overvoltage protection behaves differently. If the output exceeds 1.7V, an OV fault is immediately declared, PGOOD is latched low and the low-side FETs are turned on. The low-side FETs will remain on until the output voltage is pulled down below 0.85V at which time all FETs are turned off. If the output again rises above 1.7V, the process is repeated. This affords the maximum amount of protection against a shorted high-side FET while preventing output ringing below ground. The 1.7V OV is not reset with VR_ON, but requires that VDD be lowered to reset. The 1.7V OC detector is active at all times that the controller is enabled including after one of the other faults occurs so that the processor is protected against high-side FET leakage while the FETs are commanded off.

The ISL6260 and ISL6260B have a thermal throttling feature. If the voltage on the NTC pin goes below the 1.18V OT threshold, the VR_TT# pin is pulled low indicating the need for thermal throttling to the system oversight processor. No other action is taken within the ISL6260 and ISL6260B in response to NTC pin voltage.

Fault protection is summarized in Table 3.

Component Selection and Application

Soft-Start and Mode Change Slew Rates

The ISL6260 and ISL6260B use 2 slew rates for various modes of operation. The first is a slow slew rate, used to reduce inrush current on start-up. It is also used to reduce audible noise when entering or exiting Deeper Sleep Mode. A faster slew rate is used to exit out of Deeper Sleep and to increase system performance by achieving active mode regulation more quickly. Note that the SOFT cap current is bidirectional and is flowing into the SOFT capacitor when the output voltage is commanded to rise, and out of the SOFT capacitor when the output voltage is commanded to fall.

The two slew rates are determined by commanding 1 of 2 currents onto the SOFT pin. As can be seen in Figure 40, the SOFT pin has a capacitance to ground. Also, the SOFT pin is the input to the error amplifier and is, therefore, the commanded system voltage. Depending on the state of the system, i.e. Start-Up or Active mode, and the state of the DPRSLPVR pin, one of the two currents shown in Figure 40 will be used to charge or discharge this capacitor, thereby controlling the slew rate of the commanded voltage. These currents can be found under the Soft Current section of the Electrical Specification Table.

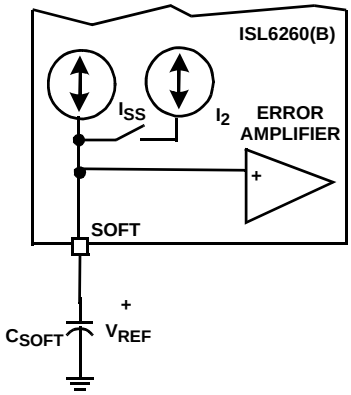


FIGURE 40. SOFT PIN CURRENT SOURCES FOR FAST AND SLOW SLEW RATES

The first current, labeled I_{SS}, is given in the Specification Table as 41µA. This current is used during Soft-Start. The second current, I_2 sums with I_{SS} to get the larger of the two currents, labeled I_{GV} in the Electrical Specification Table. This total current is typically 200µA with a minimum of 175µA.

The IMVP-6™ specification reveals the critical timing associated with regulating the output voltage. The symbol, Slewrate, as given in the IMVP-6™ specification, will determine the choice of the SOFT capacitor, C_{SOFT}, by the following equation:

$$C_{SOFT} = \frac{I_{GV}}{SLEWRATE}$$

Using a SLEWRATE of 10mV/µs, and the typical I_{GV} value, given in the Electrical Specification Table of 200µA, C_{SOFT} is

$$C_{SOFT} = \frac{200\mu A}{\frac{10mV}{1\mu s}} = 0.020\mu F \quad \text{(EQ. 2)}$$

A choice of 0.015µF would guarantee a SLEWRATE of 10mV/µs is met for minimum I_{GV} value, given in the Electrical Specification Table.

Now this choice of C_{SOFT} will then control the start-up slewrate as well. One should expect the output voltage to slew to the Boot value of 1.2V at a rate given by the following equation:

$$\frac{dV}{dt} = \frac{I_{SS}}{C_{SOFT}} = \frac{41\mu A}{0.015\mu F} = 2.73\frac{mV}{\mu s} \quad \text{(EQ. 3)}$$

Generally, when output voltage is approaching its steady state, its dv/dt will slow down to prevent overshoot. In order to compensate the slow-down effect, faster initial dv/dt slew rates can be used with small soft capacitors such as 10nF to achieve the desired overall dv/dt in the allocated time interval.

Selecting R_{BIAS}

To properly bias the ISL6260 and ISL6260B, a reference current is established by placing a 147kΩ, 1% tolerance resistor from the R_{BIAS} pin to ground. This will provide a highly accurate, 10µA current source from which OCSET reference current can be derived.

Care should be taken in layout that the resistor is placed very close to the R_{BIAS} pin and that a good quality signal ground is connected to the opposite side of the R_{BIAS} resistor. Do not connect any other components to this pin as this would negatively impact performance. Capacitance on this pin would create instabilities and is to be avoided.

Start-up Operation - CLK_EN# and PGOOD

The ISL6260 and ISL6260B provide a 3.3V logic output pin for CLK_EN#. The 3V3 pin allows for a system 3.3V source to be connected to separated circuitry inside the ISL6260 and ISL6260B, solely devoted to the CLK_EN# function. The output is a 3.3V CMOS signal with 4mA of source and sinking capability. This implementation removes the need for an external pull-up resistor on this pin, and due to the normal level of this signal being a low, removes the leakage path from the 3.3V supply to ground through the pull-up resistor. This reduces 3.3V supply current, that would occur under normal operation with a pull-up resistor, and prolongs battery life. The 3.3V supply should be decoupled to digital ground, not to analog ground for noise immunity.

As mentioned in the “Theory of Operation” section of this datasheet, CLK_EN# is logic level high at start-up until 20µs after the system Vccp and Vcc_mch supplies are within regulation, and the Vcc-core is in regulation at the Boot level. Approximately 20µs after these voltages are within regulation, as indicated by PGD_IN going high, CLK_EN# goes low, triggering an internal timer for the IMVP6_PWRGD signal. This timer allows IMVP6_PWRGD to go high approximately 7ms after CLK_EN# goes low.

Static Mode of Operation - Processor Die Sensing

Die sensing is the ability of the controller to regulate the Core output voltage at a remotely sensed point. This allows the Voltage Regulator to compensate for various resistive drops in the power path and insure that the voltage seen at the CPU die is the correct level independent of load current.

The VSEN and RTN pins of the ISL6260 and ISL6260B are connected to Kelvin sense leads at the die of the processor through the processor socket. These signal names are Vcc_sense and Vss_sense respectively. This allows the Voltage Regulator to tightly control the processor voltage at the die, independent of layout inconsistencies and drops. This Kelvin sense technique provides for extremely tight load line regulation.

These traces should be laid out as noise sensitive traces. For optimum load line regulation performance, the traces connecting these two pins to the Kelvin sense leads of the processor must be laid out away from rapidly rising voltage nodes (switching nodes) and other noisy traces. To achieve optimum performance, place common mode and differential mode RC filters to analog ground on VSEN and RTN as shown in Figure 42. The filter resistors should be in order of 10Ω so that they do not interact with the 50kΩ input resistance of the differential amplifier.

Due to the fact that the voltage feedback to the switching regulator is sensed at the processor die, there exists the potential of an overvoltage due to an open circuited feedback signal, should the regulator be operated without the processor installed. Due to this fact, we recommend the use of the Ropn1 and Ropn2 connected to Vout and ground as shown in Figure 42. These resistors will provide voltage feedback in the event that the system is powered up without a processor installed. These resistors are typically 100Ω.

Setting the Switching Frequency - FSET

The R_3 modulator scheme is not a fixed frequency PWM architecture. The switching frequency can increase during the application of a load to improve transient performance. However, it also varies slightly due changes in input and output voltage and output current, but this variation is normally less than 10% in continuous conduction mode.

Refer to Figure 35. A resistor connected between the VW and COMP pins of the ISL6260 and ISL6260B adjusts the switching window, and therefore adjusts the switching frequency. The Rfset resistor that sets up the switching frequency of the converter operating in CCM can be

determined using the following relationship, where Rfset is in kΩ and the switching period is in μs.

$$Rfset(k\Omega) = (Period(\mu s) - 0.29) \times 2.33 \quad \text{(EQ. 4)}$$

In discontinuous conduction mode, (DCM), the ISL6260, ISL6260B runs in period stretching mode. It should be noted that the switching frequency in the Electric Table is tested with the error amplifier output or Comp pin voltage at 2V. When Comp pin voltage is lower, the switching frequency will not be at the tested value.

Voltage Regulator Thermal Throttling

Intel® IMVP-6® technology supports thermal throttling of the processor to prevent catastrophic thermal damage to the voltage regulator. The ISL6260 and ISL6260B feature a thermal monitor which senses the voltage change across an externally placed negative temperature coefficient (NTC) thermistor, see Figure 41. Proper selection and placement of the NTC thermistor allows for detection of a designated temperature rise by the system.

Figure 41 shows the thermal throttling feature with hysteresis. At low temperature, SW1 is on and SW2 connects to the 1.18V side. The total current going from NTC pin is 60μA. The voltage on NTC pin is higher than threshold voltage of 1.18V and the comparator output is low. VR_TT# is pulling up high by the external resistor.

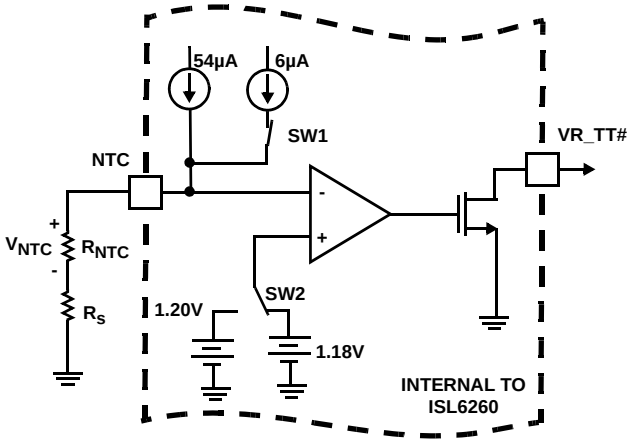


FIGURE 41. CIRCUITRY ASSOCIATED WITH THE THERMAL THROTTLING FEATURE OF THE ISL6260

When temperature increases, the NTC resistor on NTC pin decreases. The voltage on NTC pin decreases to a level lower than 1.18V. The comparator changes polarity and turns SW1 off and throws SW2 to 1.20V. This pulls VR_TT# low and sends the signal to start thermal throttle. There is a 6μA current reduction on NTC pin and 20mV voltage increase on threshold voltage of the comparator in this state. The VR_TT# signal will be used to change the CPU operation and decrease the power consumption. When the temperature goes down, the NTC thermistor voltage will eventually go up. If NTC voltage increases to 1.20V, the comparator will then be able to flip back. The external resistance difference in these two conditions is:

$$\frac{1.2\ V}{54\ \mu A} - \frac{1.18\ V}{60\ \mu A} = 2.56\ K$$

Therefore, proper NTC thermistor has to be chosen such that 2.56K resistor change will be corresponding to required temperature hysteresis. Regular external resistor may need to be in series with NTC resistors to meet the threshold voltage values.

The following is an example.

For Panasonic NTC with B = 4700, its resistance will drop to 0.03322 of its nominal at 105°C, and drop to 0.03956 of its nominal at 100 C°. If the requirement for the temperature hysteresis is (105-100) C°, the required resistance of NTC will be:

$$\frac{2.56\ K\Omega}{(0.03956 - 0.03322)} = 404\ K\ \Omega$$

Therefore a larger value thermistor, such as 470 K NTC should be used.

At 105°C, 470K NTC resistance becomes (0.03322*470K) = 15.6K. With 60μA on NTC pin, the voltage is only (15.6K*60μA) = 0.937V. This value is much lower than the threshold voltage of 1.18V. Therefore, a resistor is needed to be in series with the NTC. The required resistance can be calculated by:

$$\frac{1.18\ V}{60\ uA} - 15.6\ K\Omega = 4.06\ K\Omega$$

4.02K is a standard resistor value. Therefore, the NTC branch should have a 470K NTC and 4.02K resistor in series. The part number for the NTC thermistor is ERTJ0EV474J. It is a 0402 package. NTC thermistor will be placed in the hot spot of the board. A thermistor in an 0402 package costs less than in an 0603 package.

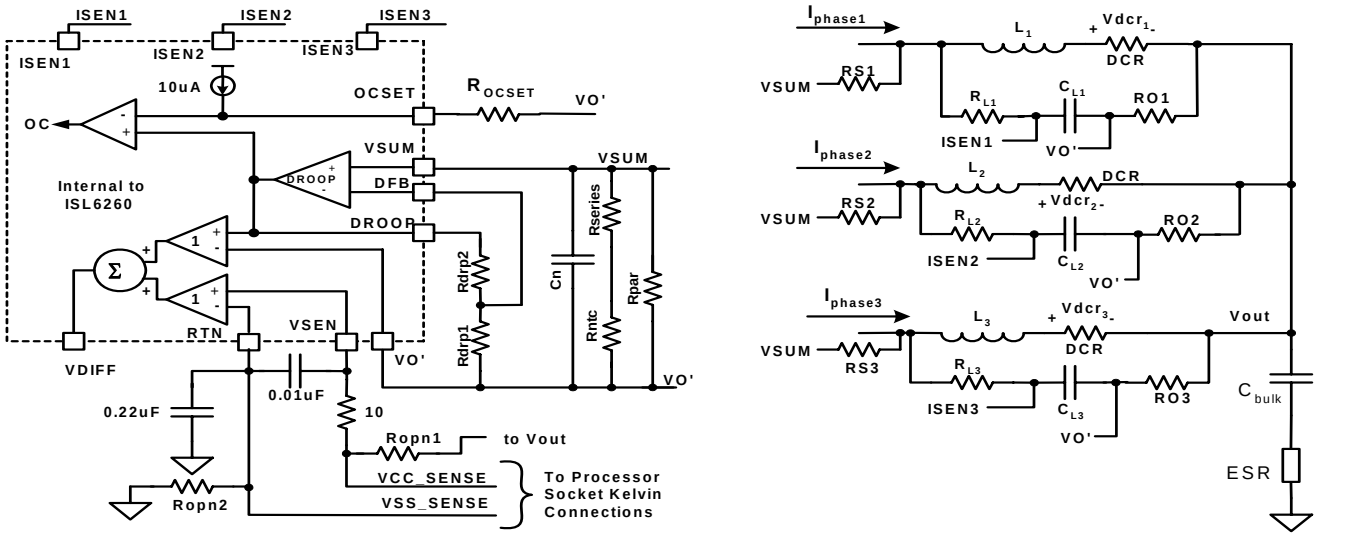


FIGURE 42. EQUIVALENT MODEL FOR DROOP AND DIE SENSING USING DCR SENSING

Static Mode of Operation - Static Droop using DCR Sensing

As previously mentioned, the ISL6260 and ISL6260B have an internal differential amplifier which provides for extremely accurate voltage regulation at the die of the processor. The load line regulation is also very accurate, and the process of selecting the components for the appropriate load line droop is explained here.

For DCR sensing, the process of compensation for DCR resistance variation to achieve the desired load line droop has several steps and is somewhat iterative. Refer to Figure 42.

In Figure 42 we show a 3 phase solution using DCR sensing. There are two resistors around the inductor of each phase. These are labeled RS and RO. These resistors are used to arrive at the DC voltage drop across each inductor. Each inductor will have a certain level of DC current flowing through it, this current when multiplied by the DCR of the inductor creates a small DC level of voltage. When this voltage is summed with the other channels DC voltages, the total DC load current can be derived.

RO is typically 5 to 10Ω. This resistor is used to tie the outputs of all channels together and thus create a summed average of the local CORE voltage output. RS is determined through an understanding of both the DC and transient load currents. This value will be covered in the next section.

However, it is important to keep in mind that the output of each of these RS resistors are tied together to create the VSUM voltage node. With both the outputs of RO and RS tied together, the simplified model for the droop circuit can be derived. This is presented in Figure 43.

Figure 43 shows the simplified model of the droop circuitry. Essentially one resistor can replace the RO resistors of each phase and one RS resistor can replace the RS resistors of each phase. The total DCR drop due to load current can be replaced by a DC source, the value of which is given by Equation 5.

$$Vdcr_{EQV} = \frac{Iout \times DCR}{N} \quad \text{(EQ. 5)}$$

where N is the number of channels designed for Active operation. N = 3 for this example. Another simplification can be done by reducing the NTC network comprised of Rntc, Rseries and Rparallel, given in Figure 43, to a single resistor given as Rn.

The first step in droop load line compensation is to adjust Rn, RO_{EQV} and RS_{EQV} such that sufficient droop voltage exists even at light loads between the VSUM and VO' nodes. We recognize that these components form a voltage divider. As a rule of thumb we start with the voltage drop across the Rn network, VN, to be 0.57 x Vdcr. This ratio provides for a fairly reasonable amount of light load signal from which to arrive at droop.

First we calculate the equivalent NTC network resistance, Rn. Typical values that provide good performance are, Rseries = 3.57K_1%, Rpar = 4.53K_1% and Rntc = 10kΩ NTC, ERT-J1VR103J from Panasonic. Rn is then given by Equation 6.

$$Rn = \frac{(Rseries + Rntc) \times Rpar}{Rseries + Rntc + Rpar} = 3.4k\Omega \quad \text{(EQ. 6)}$$

In our second step we calculate the series resistance from each phase to the Vsum node, labeled RS1, RS2 and RS3 in Figure 42.

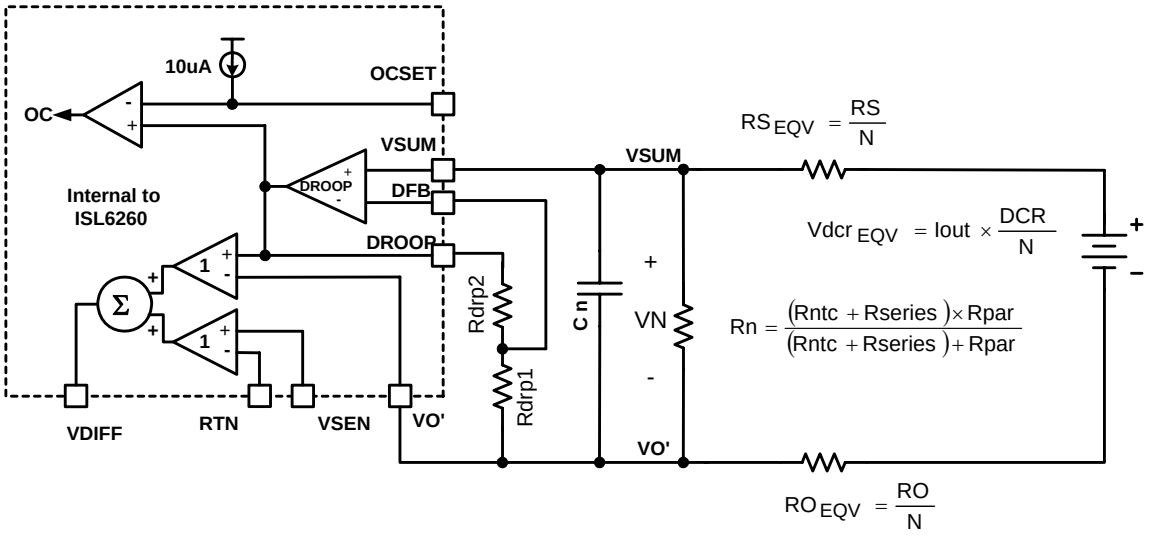


FIGURE 43. EQUIVALENT MODEL FOR DROOP AND DIE SENSING USING DCR SENSING

We do this using the assumption that we desire approximately a 0.57 gain from the DCR voltage, Vdcr, to the Rn network. We call this gain, G1.

$$G1 = 0.57 \quad \text{(EQ. 7)}$$

After simplification, then RS_{EQV} is given by the following equation:

$$RS_{EQV} = \left(\frac{1}{G1} - 1\right) Rn = 2.56k\Omega \quad \text{(EQ. 8)}$$

The individual resistors from each phase to the VSUM node, labeled RS1, RS2 and RS3 in Figure 42, are then given by Equation 9, where N is 3, for the number of channels in active operation.

$$RS = N \times RS_{EQV} = 7.69k\Omega \quad \text{(EQ. 9)}$$

Choosing RS = 7.68k_1% is a good choice. Once we know the attenuation of the RS and RN network, we can then determine the Droop amplifier Gain required to achieve the load line. Setting Rdrp1 = 1k_1%, then Rdrp2 is can be found using Equation 10.

$$Rdrp2 = \left(\frac{N \times Rdroop}{DCR \times G1} - 1\right) \times Rdrp1 \quad \text{(EQ. 10)}$$

Setting N = 3 for 3 channel operation, Droop Impedance (Rdroop) = 0.0021 (V/A) as per the Intel IMVP-6 specification, DCR = 0.0012Ω typical, Rdrp1 = 1kΩ and the attenuation gain (G1) = 0.57, Rdrp2 is then

$$Rdrp2 = \left(\frac{3 \times 0.0021}{0.0012 \times 0.57} - 1\right) \times 1K = 8.21k\Omega \quad \text{(EQ. 11)}$$

Rdrp2 is selected to be a 8.25k_1% resistor. Note, we choose to ignore the RO resistors because they do not add significant error.

These values are extremely sensitive to layout and coupling factor of the NTC to the inductor. As only one NTC is required in this application, this NTC should be placed as close to the Channel 1 inductor as possible and PCB traces sensing the inductor voltage should be go directly to the inductor pads.

Once the board has been laid out, some adjustments may be required to adjust the full load droop voltage. This is fairly easy and can be accomplished by allowing the system to achieve thermal equilibrium at full load, and then adjusting Rdrp2 to obtain the appropriate load line slope.

To see whether the NTC has compensated the temperature change of the DCR, the user can apply full load current and wait for the thermal steady state and see how much the output voltage will deviate from the initial voltage reading. A good compensation can limit the drift to 2mV. If the output voltage is decreasing with temperature increase, that ratio between the NTC thermistor value and the rest of the resistor divider network has to be increased. The user should follow the component values and layout of NTC on evaluation board as much as possible to minimize engineering time.

The 2.1mV/A load line should be adjusted by Rdrp2 based on maximum current steps, not based on small current steps like 10A, as the droop gain might vary slightly between each 10A steps. Basically, if the max current is 40A, the required droop voltage is 84mV. The user should have 40A load current on the converter and look for 84mV droop. If the droop voltage is

less than 84mV, for example, 80mV. The new value will be calculated by:

$$Rdrp\ \ 2\ \_\ new\ \ = \frac{84\ mV}{80\ mV}(Rdrp\ \ 1 + Rdrp\ \ 2) - Rdrp\ \ 1$$

For the best accuracy, the effective resistance on the DFB and VSUM pins should be identical so that the bias current of the droop amplifier does not cause an offset voltage. In the example above, the resistance on the DFB pin is Rdrp1 in parallel with Rdrop2, that is, 1K in parallel with 8.21K or 890Ω. The resistance on the VSUM pin is Rn in parallel with RSeqv or 3.4K in parallel with 2.56K or 1460Ω. The mismatch in the effective resistances is 1460-890 = 570Ω. Do not let the mismatch get larger than 600Ω. To reduce the mismatch, multiply both Rdrp1 and Rdrp2 by the appropriate factor. The appropriate factor in the example is 1460/890 = 1.64.

Dynamic Mode of Operation - Dynamic Droop using DCR Sensing

Droop is very important for load transient performance. If the system is not compensated correctly, the output voltage could sag excessively upon load application and potentially create a system failure. The output voltage could also take a long period of time to settle to its final value. This could be problematic if a load dump were to occur during this time. This situation would cause the output voltage to rise above the no load setpoint of the converter and could potentially damage the CPU.

The L/DCR time constant of the inductor must be matched to the Rn*Cn time constant as shown in the following equation:

$$\frac{L}{DCR} = \left(\frac{Rn \times RS_{EQV}}{Rn + RS_{EQV}}\right) \times Cn \qquad \text{(EQ. 12)}$$

Solving for Cn we now have the following equation:

$$Cn = \frac{\frac{L}{DCR}}{\left(\frac{Rn \times RS_{EQV}}{Rn + RS_{EQV}}\right)} \qquad \text{(EQ. 13)}$$

Note, RO was neglected. As long as the inductor time constant matches the Cn, Rn and Rs time constants as given above, the transient performance will be optimum. As in the Static Droop Case, this process may require a slight adjustment to correct for layout inconsistencies. For the example of L = 0.5µH, Cn is calculated below.

$$Cn = \frac{\frac{0.5\mu H}{0.0012}}{\left(\frac{3.4k\Omega \times 2.56k\Omega}{3.4k\Omega + 2.56k\Omega}\right)} = 28.5nF \qquad \text{(EQ. 14)}$$

The value of this capacitor is selected to be 27nF. As the inductors tend to have 20% to 30% tolerances, this cap generally will be tuned on the board by examining the transient voltage. If the output voltage transient has an initial dip, lower than the voltage required by the load line, and slowly increases back to the steady state, the cap is too small and vice versa. It is better to have the cap value a little bigger to cover the tolerance of the inductor to prevent the output voltage from going lower than the spec. This cap needs to be a high grade cap like X7R with low tolerance. There is another consideration in order to achieve better time constant match mentioned above. The NPO/COG (class-I) capacitors have only 5% tolerance and a very good thermal characteristics. But those caps are only available in small capacitance values. In order to use such capacitors, the resistors and thermistors surrounding the droop voltage sensing and droop amplifier has to be resized up to 10X to reduce the capacitance by 10X. But attention has to be paid in balancing the impedance of droop amplifier in this case.

Dynamic Mode of Operation - Compensation Parameters

Considering the voltage regulator as a black box with a voltage source controlled by VID and a series impedance, in order to achieve the 2.1mV/A load line, the impedance needs to be 2.1mΩ. The compensation design has to ensure the output impedance of the converter be lower than 2.1mΩ. There is a mathematical calculation file available to the user. The power stage parameters such as L and Cs are needed as the input to calculate the compensation component values. Attention has be paid to the input resistor to the FB pin. Too high of a resistor will cause an error to the output voltage regulation because of bias current flowing in the FB pin. It is better to keep this resistor below 3K when using this file.

Static Mode of Operation - Current Balance using DCR or Discrete Resistor Current Sensing

Current Balance is achieved in the ISL6260 and ISL6260B through the matching of the voltages present on the ISEN pins. The ISL6260 and ISL6260B adjust the duty cycles of each phase to maintain equal potentials on the ISEN pins. RL and CL around each inductor, or around each discrete current resistor, are used to create a rather large time constant such that the ISEN voltages have minimal ripple voltage and represent the DC current flowing through each channel's inductor. For optimum performance, RL is chosen to be 10kΩ and CL is selected to be 0.22µF. When discrete resistor sensing is used, a capacitor of 10nF should be placed in parallel with RL to properly compensate the current balance circuit.

ISL6260 and ISL6260B uses RC filter to sense the average voltage on phase node and forces the average voltage on the phase node to be equal for current balance. Even though the ISL6260, ISL6260B forces the ISEN voltages to be almost equal, the inductor currents will not be exactly equal. Take DCR current sensing as example, two errors have to be added to find the total current imbalance. 1) Mismatch of DCR: If the DCR has a 5% tolerance then the resistors could mismatch by 10% worst case. If each phase is carrying 20A then the phase currents mismatch by 20A*10% = 2A. 2) Mismatch of phase voltages/offset voltage of ISEN pins. The

phase voltages are within 2mV of each other by current balance circuit. The error current that results is given by 2mV/DCR. If DCR = 1mΩ then the error is 2A.

In the above example, the two errors add to 4A. For a two phase DC/DC, the currents would be 22A in one phase and 18A in the other phase. In the above analysis, the current balance can be calculated with 2A/20A = 10%. This is the worst case calculation, for example, the actual tolerance of two 10% DCRs is 10%*sqrt(2) = 7%.

There are provisions to correct the current imbalance due to layout or to purposely divert current to certain phase for better thermal management. Customer can put a resistor in parallel with the current sensing capacitor on the phase of interest in order to purposely increase the current in that phase. But it is highly recommended for symmetrical layout.

In the case the PC board trace resistance from the inductor to the microprocessor are not the same on all three phases, the current will not be balanced. On the phases that have too much trace resistance a resistor can be added in parallel with the ISEN capacitor that will correct for the poor layout. But it is highly recommended for symmetrical layout.

An estimate of the value of the resistor is:

Rtweak = Risen* [2*Rdcr - (Rtrace - Rmin)]/[2(Rtrace - Rmin)]

where Risen is the resistance from the phase node to the ISEN pin; usually 10kΩ. Rdcr is the DCR resistance of the inductor. Rtrace is the trace resistance from the inductor to the microprocessor on the phase that needs to be tweaked. It should be measured with a good microΩ meter. Rmin is the trace resistance from the inductor to the microproccessor on the phase with the least resistance.

For example, if the PC board trace on one phase is 0.5mΩ and on another trace is 0.3mΩ; and if the DCR is 1.2mΩ; then the tweaking resistor is Rtweak = 10kΩ * [1.2*2 - (0.5-0.3)]/[2*(0.5-0.3)] = 55kΩ.

Droop using Discrete Resistor Sensing - Static/ Dynamic Mode of Operation

When choosing current sense resistor, not only the tolerance of the resistance is important, but also the TCR. And its combined tolerance at a wide temperature range should be calculated.

Figure 44 shows the equivalent circuit of a discrete current sense approach. Figure 36 shows a more detailed schematic of this approach. Droop is solved the same way as the DCR sensing approach with a few slight modifications.

First, there is no NTC required for thermal compensation, therefore, the Rn resistor network in the previous section is not required. Secondly, there is no time constant matching required, therefore, the Cn component is not matched to the L/DCR time constant, but this component does indeed provide noise immunity, especially due to the ESL of the current sensing resistors, and therefore is populated with a 47pF capacitor.

The Rs values in the previous section, Rs = 7.68k_1% are sufficient for this approach.

Now, the input to the Droop amplifier is the Vrsense voltage. This voltage is given by the following equation:

$$Vrsense = \frac{Rsense}{N} \times Iout \quad \text{(EQ. 15)}$$

The gain of the Droop amplifier, G2, must be adjusted for the ratio of the Rsense to Droop impedance, Rdroop. We use the following equation:

$$G2 = \frac{Rdroop}{Rsense} \times N \quad \text{(EQ. 16)}$$

Assuming N = 3, Rdroop = 0.0021(V/A) as per the Intel IMVP-6 specification, Rsense = 0.001Ω, we obtain G2 = 6.3.

The values of Rdrp1 and Rdrp2 are selected to satisfy two requirements. First, the ratio of Rdrp2 and Rdrp1 determine the gain G2 = (Rdrp2/Rdrp1)+1. Second, the parallel combination of Rdrp1 and Rdrp2 should equal the parallel combination of the Rs resistors. Combining these requirements gives:

Rdrp1 = G2/(G2-1) * Rs/N

Rdrp2 = (G2-1) * Rdrp1

In the example above, Rs = 7.68K, N = 3, and G2 = 6.3 so Rdrp 3K and Rdrp2 is 15.8kΩ.

These values are extremely sensitive to layout. Once the board has been laid out, some tweaking may be required to adjust the full load Droop. This is fairly easy and can be accomplished by allowing the system to achieve thermal equilibrium at full load, and then adjusting Rdrp2 to obtain the desired Droop value.

Fault Protection - Overcurrent Fault Setting

As previously described, the overcurrent protection of the ISL6260, ISL6260B is related to the Droop voltage. Previously we have calculated that the Droop Voltage = ILoad * Rdroop, where Rdroop is the load line slope specified as 0.0021 (V/A) in the Intel IMVP-6 specification. Knowing this relationship, the overcurrent protection threshold can be set up as a voltage Droop level. Knowing this voltage droop level, one can program in the appropriate drop across the Roc resistor. This voltage drop will be referred to as Voc. Once the droop voltage is greater than Voc, the PWM drives will turn off and PGOOD will go low.

The selection of Roc is given below in Equation 17. Assuming we desire an overcurrent trip level, Ioc, of 55A, and knowing from the Intel Specification that the load line

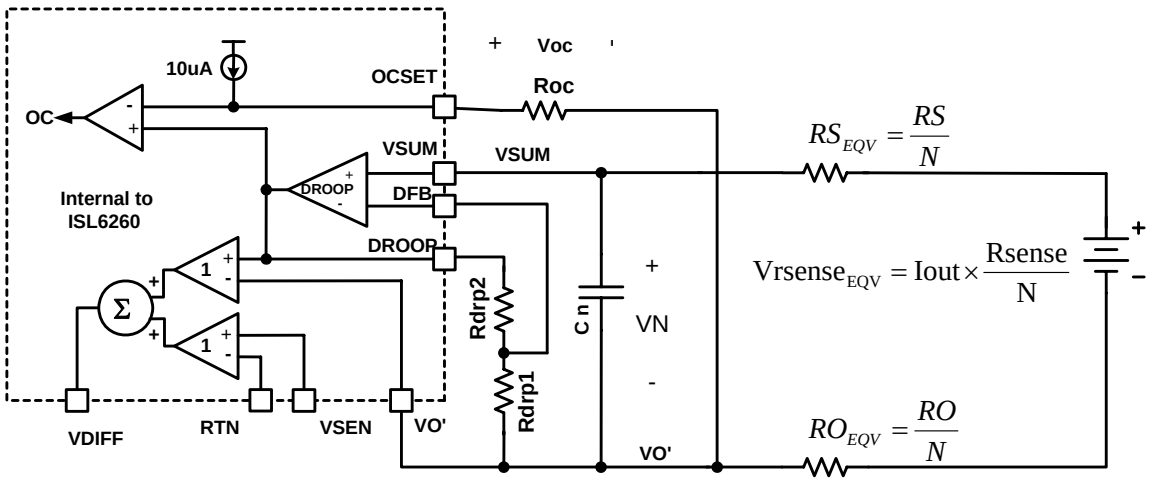


FIGURE 44. EQUIVALENT MODEL FOR DROOP AND DIE SENSING USING DISCRETE RESISTOR SENSING

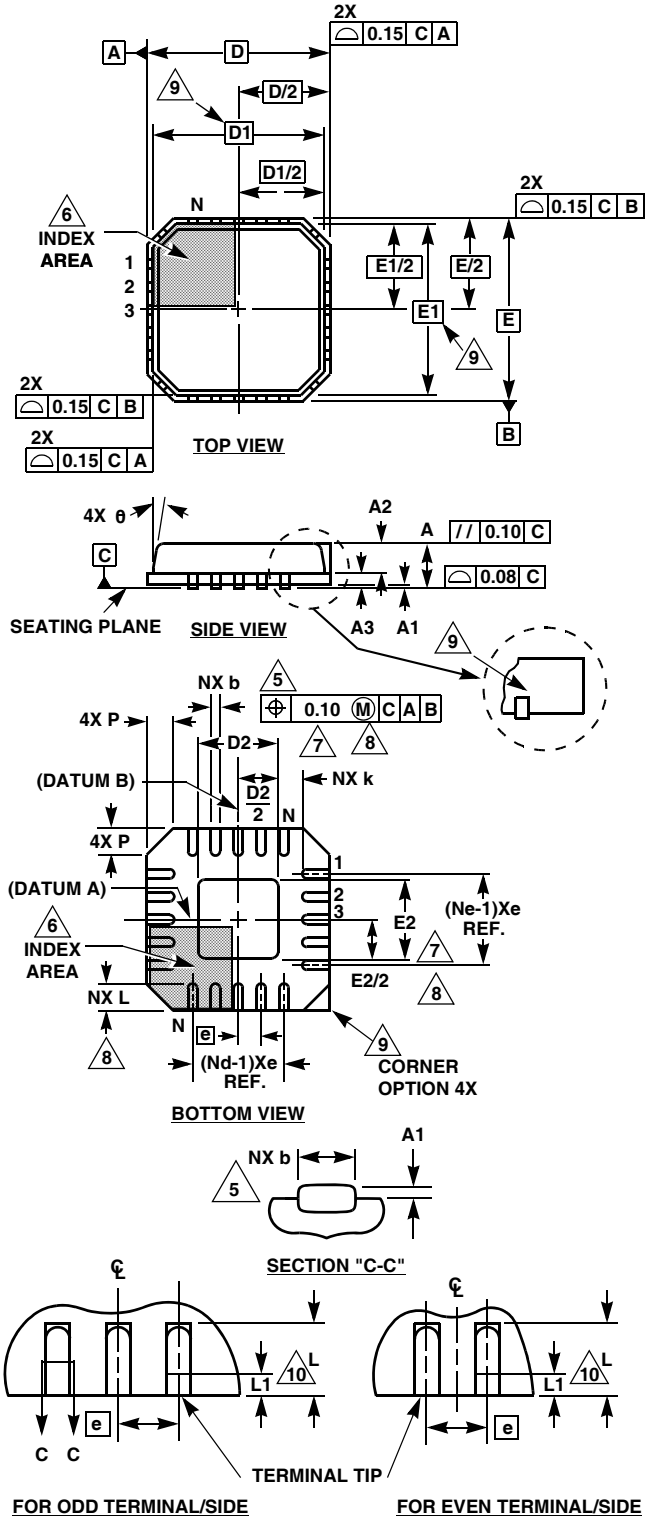
slope, Rdroop is 0.0021 (V/A), we can then calculate for Roc as shown in Equation 17.

$$Roc = \frac{Ioc \times Rdroop}{10\mu A} = \frac{55 \times 0.0021}{10x10^{-6}} = 11.5K\Omega \qquad \text{(EQ. 17)}$$

Note, if the droop load line slope is not -0.0021 (V/A) in the application, the overcurrent setpoint will differ from predicted.

A capacitor may be added in parallel with Roc to improve noise rejection but the Roc*capacitor time constant cannot exceed 20µs. Do not remove Roc if overcurrent protection is not desired. The maximum Roc is 30K.

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L40.6x6

40 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VJJD-2 ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.18	0.23	0.30	5, 8
D		6.00 BSC		-
D1		5.75 BSC		9
D2	3.95	4.10	4.25	7, 8
E		6.00 BSC		-
E1		5.75 BSC		9
E2	3.95	4.10	4.25	7, 8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.30	0.40	0.50	8
L1	-	-	0.15	10
N		40		2
Nd		10		3
Ne		10		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 1 10/02

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.