

## FEATURES

- ◆ Avalanche Rugged Technology
- ◆ Rugged Gate Oxide Technology
- ◆ Lower Input Capacitance
- ◆ Improved Gate Charge
- ◆ Extended Safe Operating Area
- ◆ Lower Leakage Current: 10µA (Max.) @  $V_{DS} = 100V$
- ◆ Lower  $R_{DS(ON)}$ : 0.336Ω (Typ.)

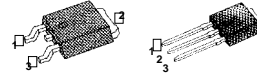
$$BV_{DSS} = 100 V$$

$$R_{DS(on)} = 0.44\Omega$$

$$I_D = 4.7 A$$

**D-PAK**

**I-PAK**



1. Gate 2. Drain 3. Source

## Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
$V_{DSS}$	Drain-to-Source Voltage	100	V
$I_D$	Continuous Drain Current ( $T_C=25^\circ C$ )	4.7	A
	Continuous Drain Current ( $T_C=100^\circ C$ )	3	
$I_{DM}$	Drain Current-Pulsed (1)	16	A
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulsed Avalanche Energy (2)	58	mJ
$I_{AR}$	Avalanche Current (1)	4.7	A
$E_{AR}$	Repetitive Avalanche Energy (1)	2.2	mJ
dv/dt	Peak Diode Recovery dv/dt (3)	6.5	V/ns
$P_D$	Total Power Dissipation ( $T_A=25^\circ C$ ) *	2.5	W
	Total Power Dissipation ( $T_C=25^\circ C$ )	22	W
	Linear Derating Factor	0.18	W/ $^\circ C$
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	- 55 to +150	$^\circ C$
$T_L$	Maximum Lead Temp. for Soldering Purposes, 1/8. from case for 5-seconds	300	

## Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	5.6	$^\circ C/W$
$R_{\theta JA}$	Junction-to-Ambient *	--	50	
$R_{\theta JA}$	Junction-to-Ambient	--	110	

\* When mounted on the minimum pad size recommended (PCB Mount).

Rev. B

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### Electrical Characteristics (T<sub>C</sub>=25°C unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	100	--	--	V	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA
ΔBV/ΔT <sub>J</sub>	Breakdown Voltage Temp. Coeff.	--	0.1	--	V/°C	I <sub>D</sub> =250μA <b>See Fig 7</b>
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.0	--	2.0	V	V <sub>DS</sub> =5V, I <sub>D</sub> =250μA
I <sub>GSS</sub>	Gate-Source Leakage, Forward	--	--	100	nA	V <sub>GS</sub> =20V
	Gate-Source Leakage, Reverse	--	--	-100		V <sub>GS</sub> =-20V
I <sub>DSS</sub>	Drain-to-Source Leakage Current	--	--	10	μA	V <sub>DS</sub> =100V
		--	--	100		V <sub>DS</sub> =80V, T <sub>C</sub> =125°C
R <sub>DS(on)</sub>	Static Drain-Source On-State Resistance	--	--	0.44	Ω	V <sub>GS</sub> =5V, I <sub>D</sub> =2.35A (4)
g <sub>fs</sub>	Forward Transconductance	--	3.2	--	Ū	V <sub>DS</sub> =40V, I <sub>D</sub> =2.35A (4)
C <sub>iss</sub>	Input Capacitance	--	180	235	pF	V <sub>GS</sub> =0V, V <sub>DS</sub> =25V, f=1MHz <b>See Fig 5</b>
C <sub>oss</sub>	Output Capacitance	--	50	65		
C <sub>rss</sub>	Reverse Transfer Capacitance	--	20	25		
t <sub>d(on)</sub>	Turn-On Delay Time	--	8	25	ns	V <sub>DD</sub> =50V, I <sub>D</sub> =5.6A, R <sub>G</sub> =12Ω <b>See Fig 13</b> (4) (5)
t <sub>r</sub>	Rise Time	--	10	30		
t <sub>d(off)</sub>	Turn-Off Delay Time	--	17	45		
t <sub>f</sub>	Fall Time	--	8	25		
Q <sub>g</sub>	Total Gate Charge	--	5.5	8	nC	V <sub>DS</sub> =80V, V <sub>GS</sub> =5V, I <sub>D</sub> =5.6A <b>See Fig 6 &amp; Fig 12</b> (4) (5)
Q <sub>gs</sub>	Gate-Source Charge	--	0.9	--		
Q <sub>gd</sub>	Gate-Drain (. Miller. ) Charge	--	3.5	--		

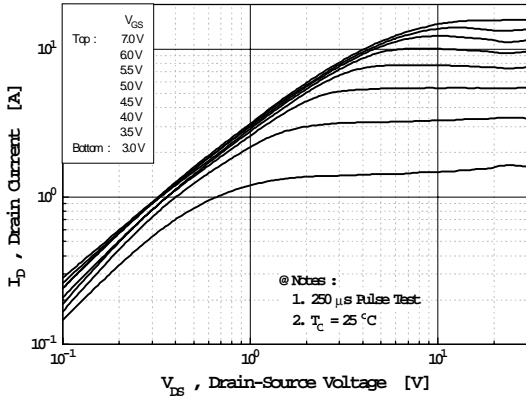
### Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
I <sub>S</sub>	Continuous Source Current	--	--	4.7	A	Integral reverse pn-diode in the MOSFET
I <sub>SM</sub>	Pulsed-Source Current (1)	--	--	16		
V <sub>SD</sub>	Diode Forward Voltage (4)	--	--	1.5	V	T <sub>J</sub> =25°C, I <sub>S</sub> =4.7A, V <sub>GS</sub> =0V
t <sub>rr</sub>	Reverse Recovery Time	--	85	--	ns	T <sub>J</sub> =25°C, I <sub>F</sub> =5.6A
Q <sub>rr</sub>	Reverse Recovery Charge	--	0.23	--	μC	di <sub>F</sub> /dt=100A/μs (4)

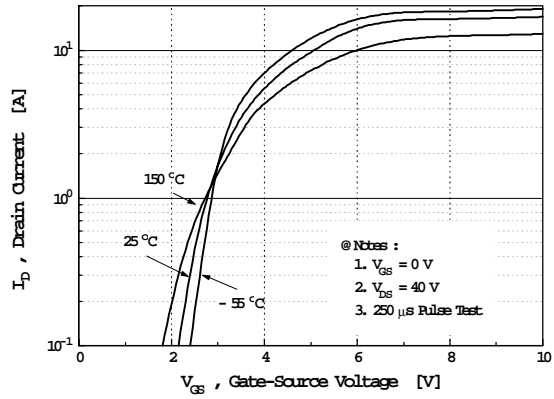
#### Notes;

- (1) Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
- (2) L=4mH, I<sub>AS</sub>=4.7A, V<sub>DD</sub>=25V, R<sub>G</sub>=27Ω, Starting T<sub>J</sub>=25°C
- (3) I<sub>SD</sub> ≤ 5.6A, di/dt ≤ 250A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, Starting T<sub>J</sub>=25°C
- (4) Pulse Test: Pulse Width = 250μs, Duty Cycle ≤ 2%
- (5) Essentially Independent of Operating Temperature

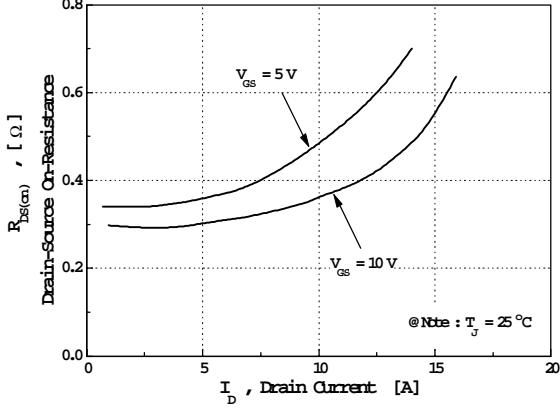
**Fig 1. Output Characteristics**



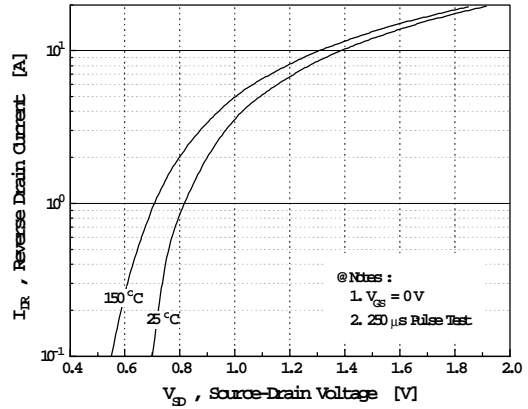
**Fig 2. Transfer Characteristics**



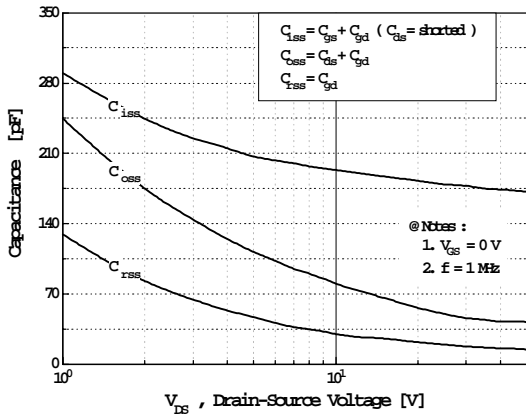
**Fig 3. On-Resistance vs. Drain Current**



**Fig 4. Source-Drain Diode Forward Voltage**



**Fig 5. Capacitance vs. Drain-Source Voltage**



**Fig 6. Gate Charge vs. Gate-Source Voltage**

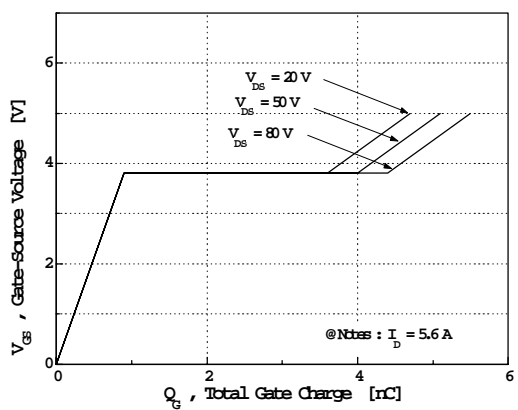


Fig 7. Breakdown Voltage vs. Temperature

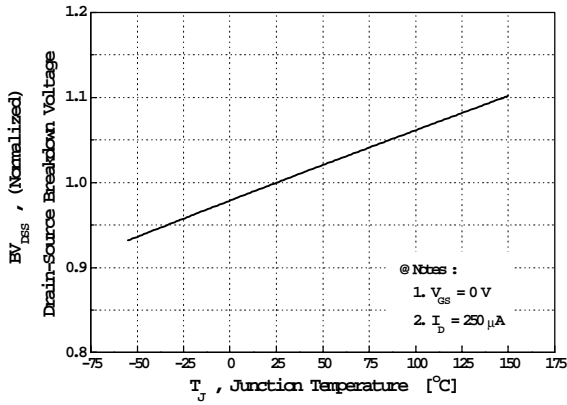


Fig 8. On-Resistance vs. Temperature

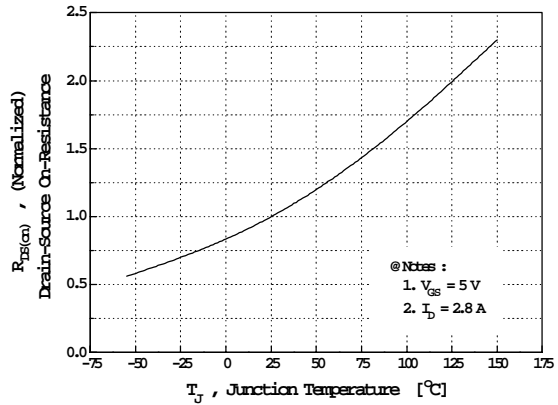


Fig 9. Max. Safe Operating Area

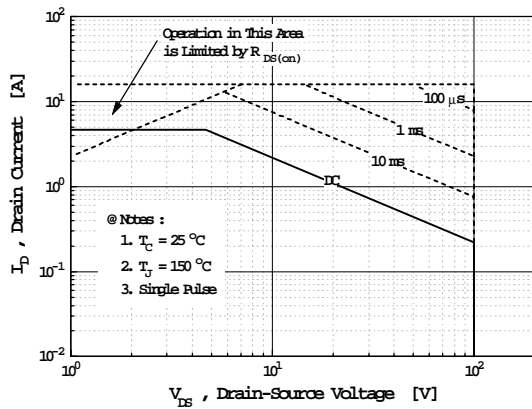


Fig 10. Max. Drain Current vs. Case Temperature

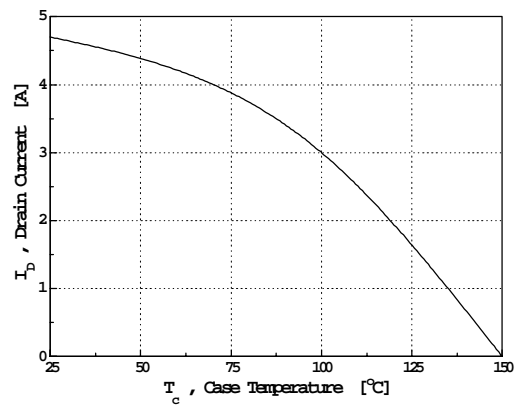
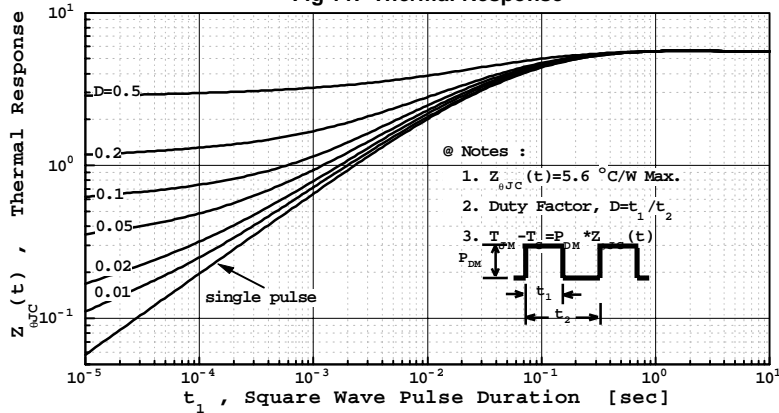
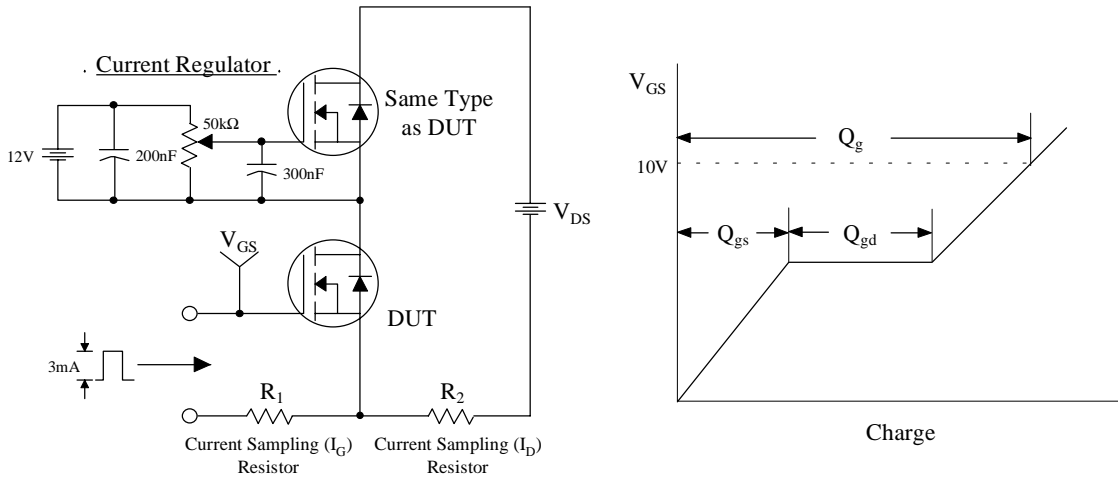


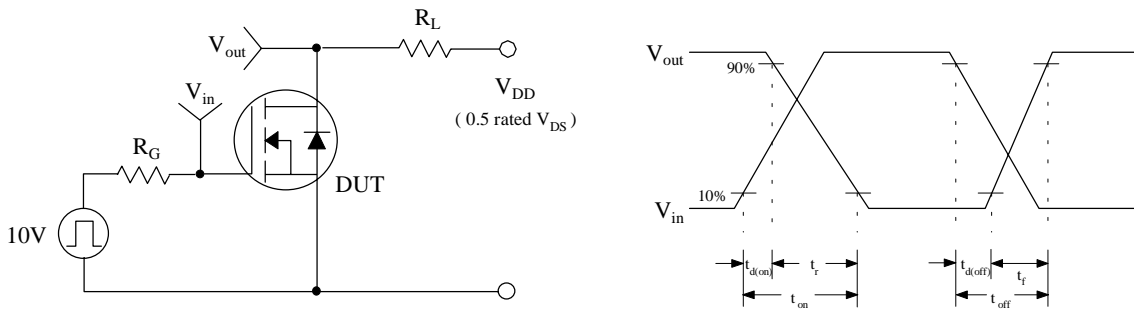
Fig 11. Thermal Response



**Fig 12. Gate Charge Test Circuit & Waveform**



**Fig 13. Resistive Switching Test Circuit & Waveforms**



**Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms**

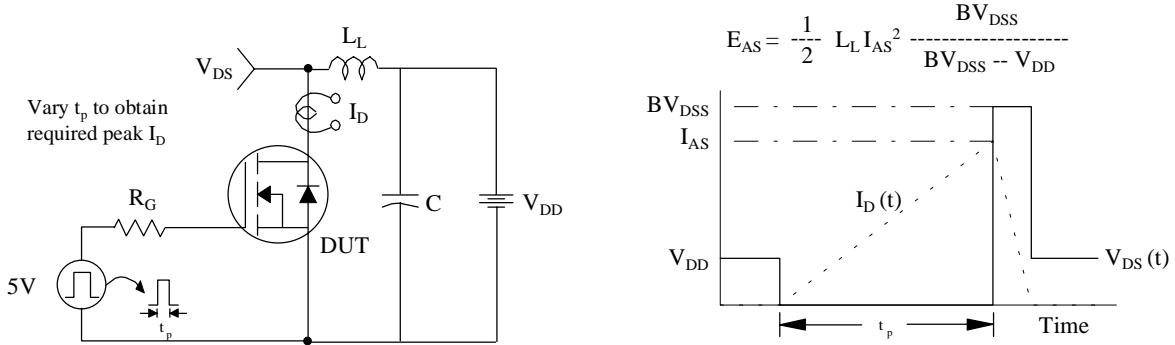
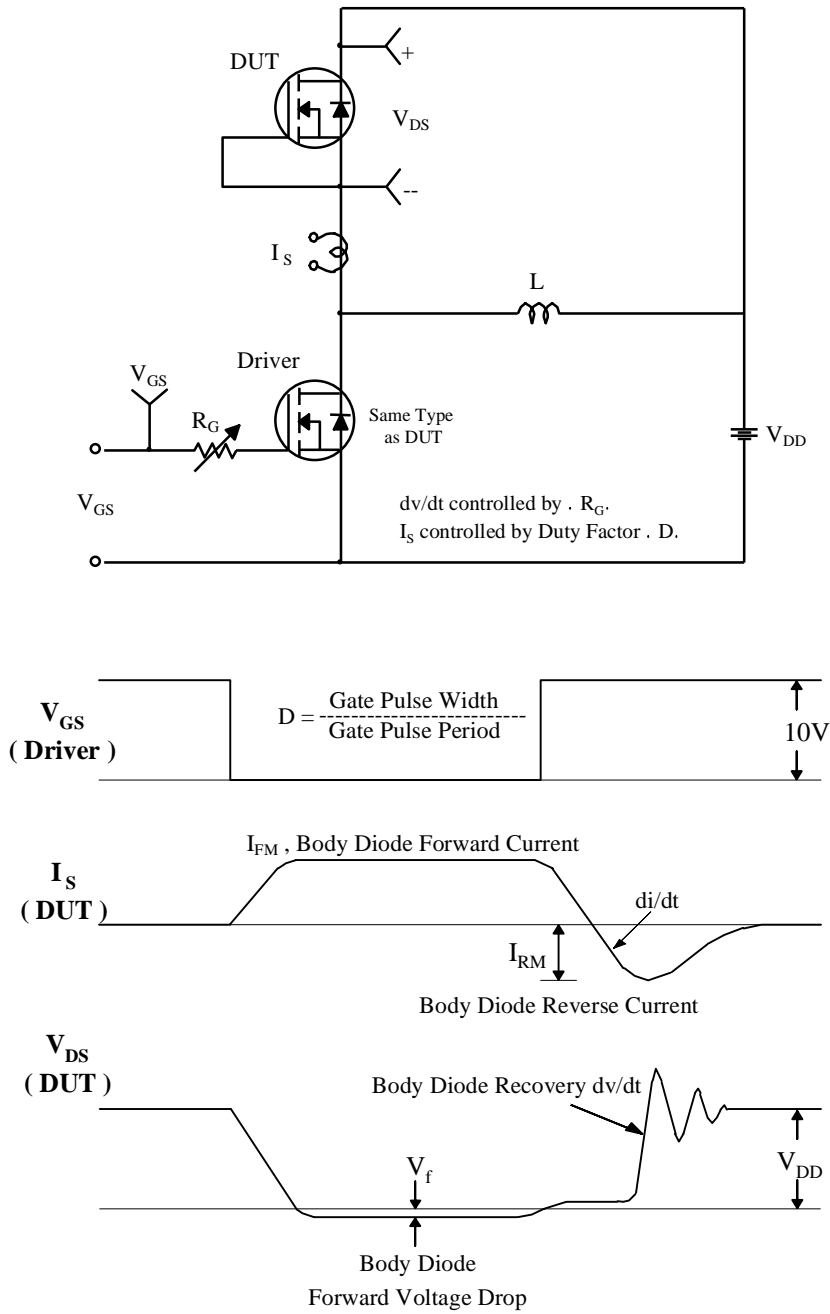


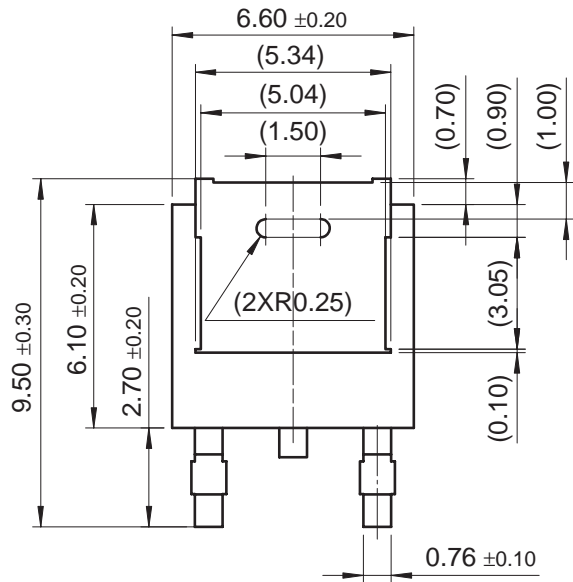
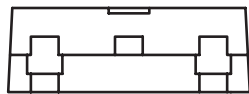
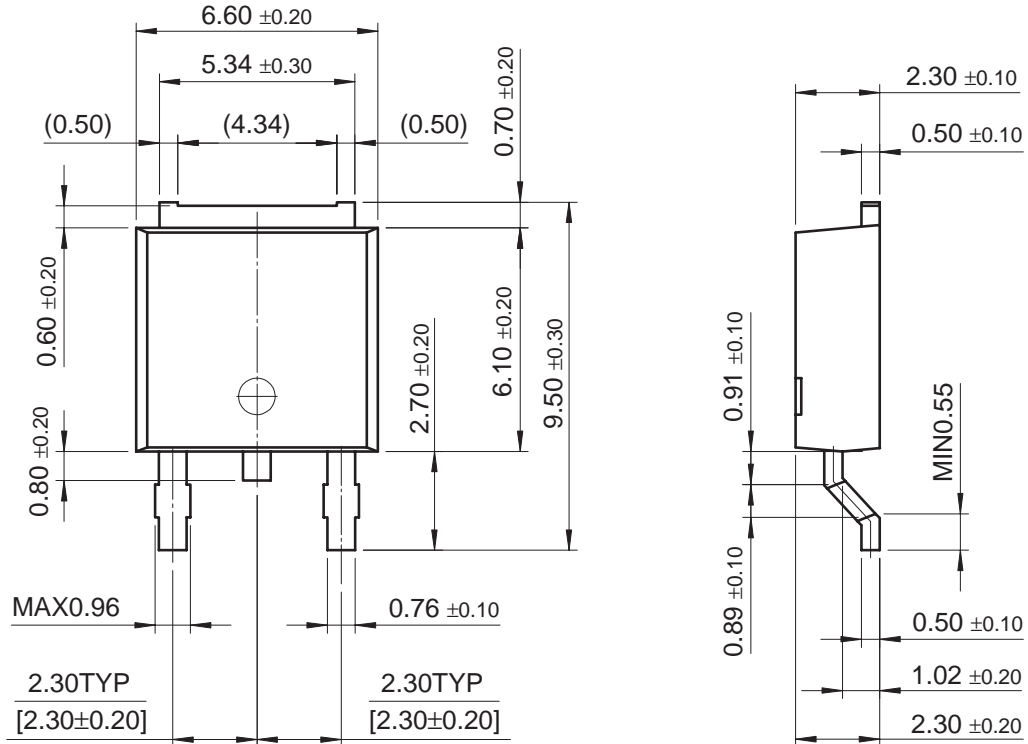
Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



DPAK Package Dimensions



DPAK (FS PKG CODE AA)

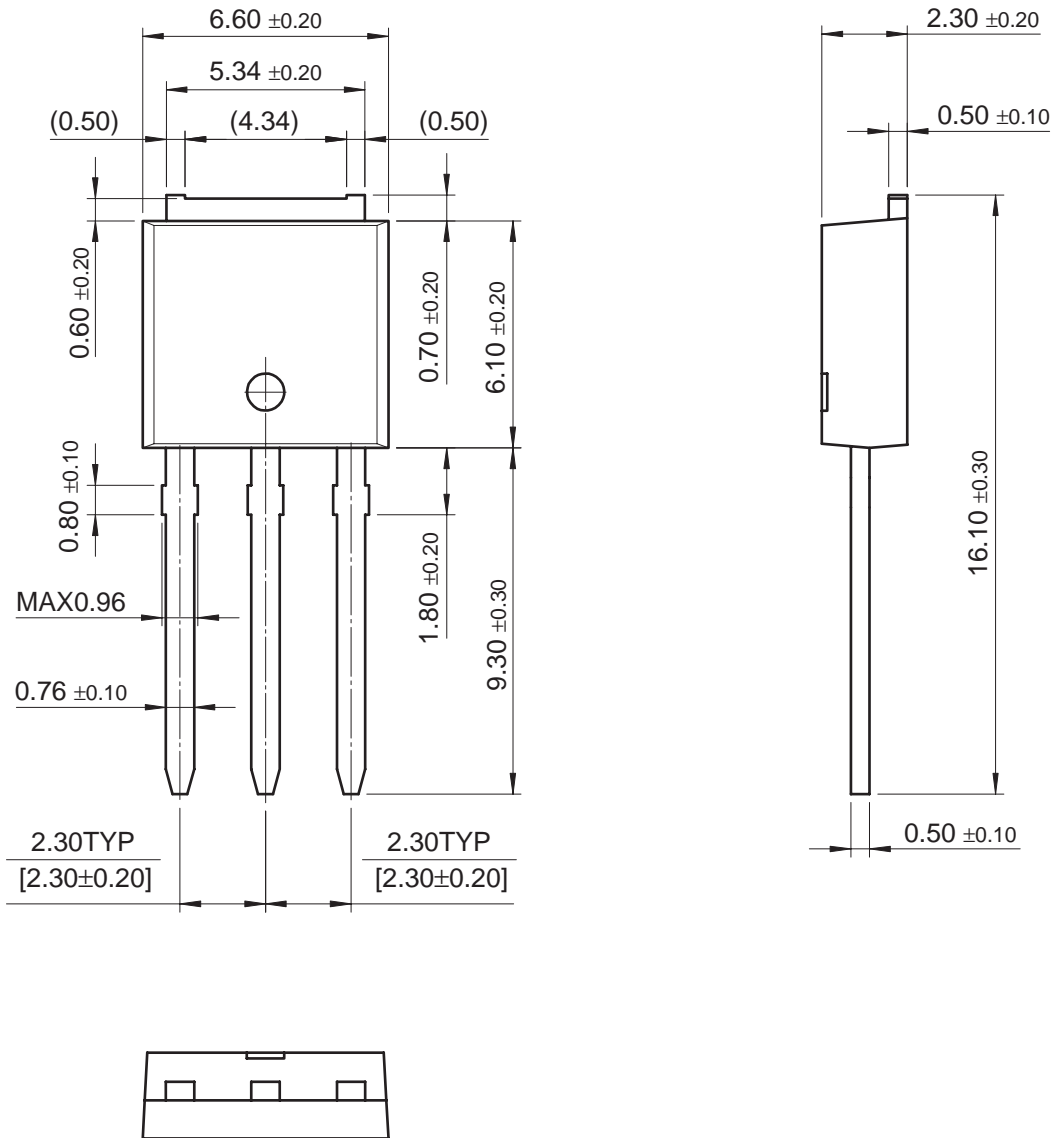


Dimensions in Millimeters

IPAK Package Dimensions



IPAK (FS PKG CODE AL)



Dimensions in Millimeters

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