ANX7150
Ultra-Low Power HDMI™ Transmitter

Programmer Guide ***Revision 0.93***

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Contents

List of Figures

List of Tables

Revision History

Rev. #	Date	Author	Comments
0.9	May 2009		Initial version.
0.92	July 2009		1. Delete Appendix in Chapter 12 and 13. 2. Add the description of achieving lower stand-by power in **Wait Hotplug**, **Firmware State Diagram**, chapter 2**.**
0.93	Sept 2009		1. Update description of initialization in chapter 3. 2. Update description of read and parse EDID in chapter 5.

1 Introduction

The ANX7150 is an HDMI (High-Definition Multimedia Interface) transmitter device supporting HDMI 1.2 and HDCP 1.1 specifications. The ANX7150 can be used to send protected digital video and audio data. It provides a low cost digital interface for source devices such as DVD players, set-top boxes, DVRs, computers, and so on. It is also backward compatible with DVI 1.0 and supports any DVI 1.0 display connected with the ANX7150.

This document is a description of the firmware of the ANX7150 Evaluation Board and a guide for system engineers and programmers.

Figure 1-1 illustrates the connection of a HDMI transmitter and receiver in a digital multimedia display system.

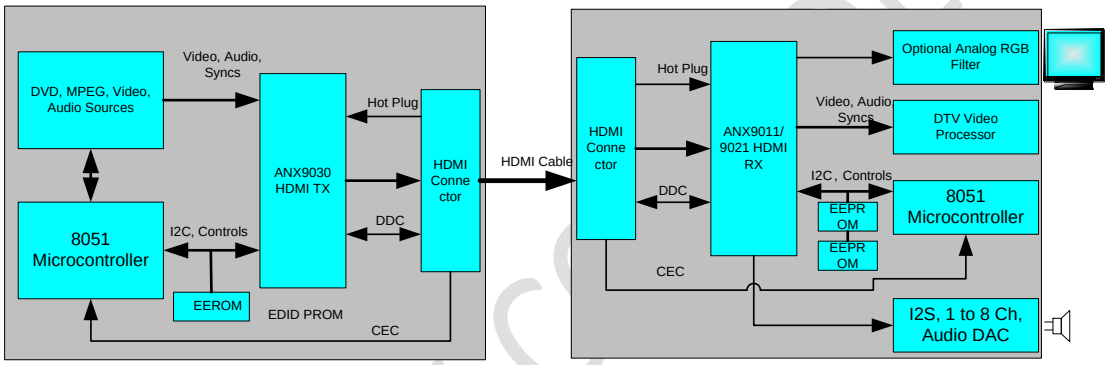

Figure 1-1 Digital Multimedia Display System with HDMI Interface

2 Firmware Overview

The top level state diagram of the ANX7150 firmware is shown in Figure 2-1.

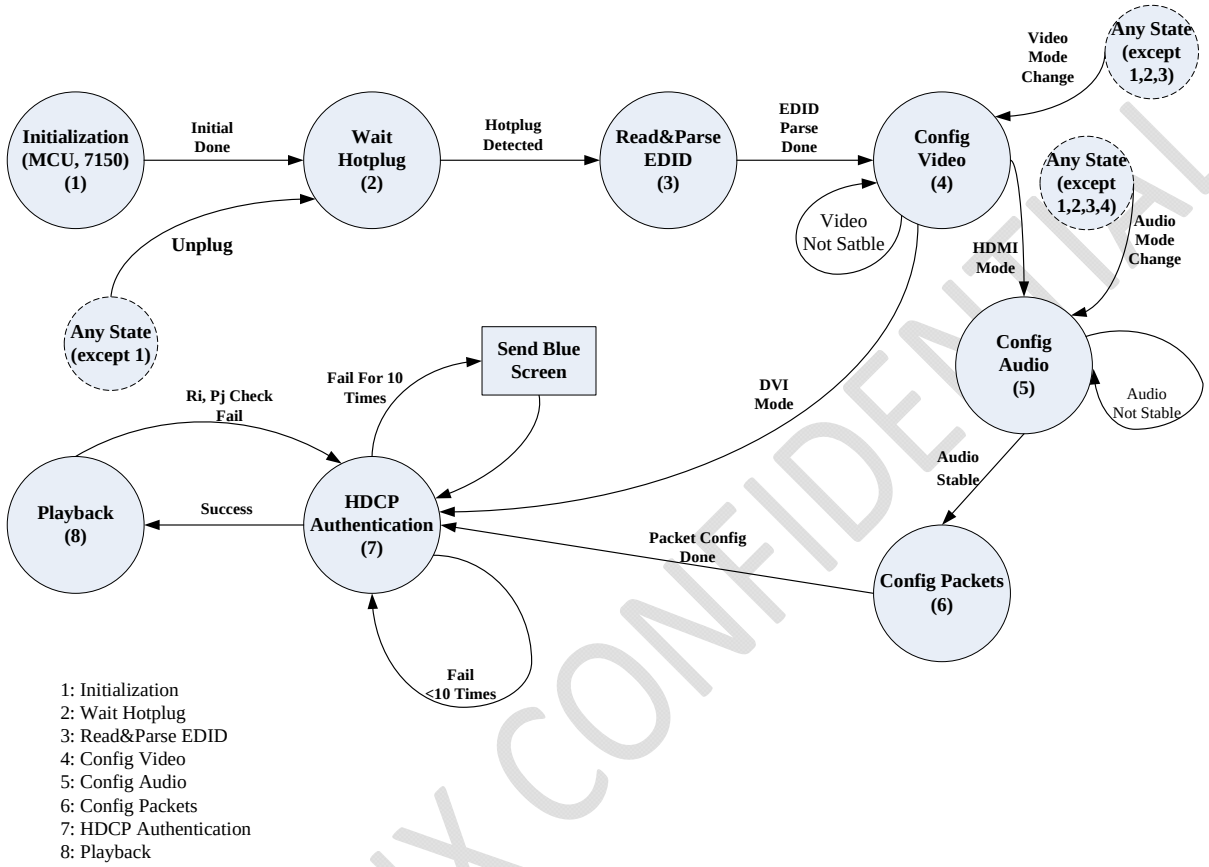

Figure 2-1 State Diagram of the ANX7150 Firmware

A total of eight states are specified in the ANX7150 firmware state machine.

Initialization: In the initialization state, the firmware sets necessary registers of the ANX7150 to an appropriate value for the operating mode. In this state, the ANX7150 is in a power down status, only IDCK, MCLK, SCK and the Hotplug module are active.

Wait Hotplug: After the ANX7150 is initialized, the firmware enters the Wait Hotplug state. In this state, when a Hotplug state is detected (an active HDMI receiver is plugged in), the ANX7150 powers on and enters into a Read & Parse EDID state.

This is a stand-by state of ANX7150, to achieve low power consumption in stand-by mode, all the functions of ANX7150 shall be power down, except the I2C slave interface. It is recommended that the AV source (SoC) shall stop sending video/audio to ANX7150 in stand-by mode to achieve even lower stand-by power.

Read & Parse EDID: In this state, the firmware reads and parses the EDID data of the receiver through the DDC channel. Based on the parsing results, the transmitter selects a preferred video/audio mode to send.

Config Video: The firmware configures the video format such as color space, DE generator, embedded SYNC, pixel clock repeat times, and so on.

Config Audio: The firmware configures the audio format such as audio source (I2S, SPDIF, and one bit audio), audio fifo map, audio data down sample, audio channel status, and so on. Some audio configuration contents are specified by the system.

Config Packets: The firmware then configures infoframe packets such as AVI infoframe, audio infoframe, SPD infoframe, and so on. Some contents of infoframe packets are specified by the system.

HDCP Authentication: In this state, the firmware handles HDCP authentication, including HDCP error handling.

Playback: This is the normal work mode of the system. The firmware monitors related status registers and responses to interrupts, and then takes corresponding action.

2.1 Firmware Main Loop

The following program is the main loop of the ANX7150 firmware.

```
while (1)
{
        if (restart_system)
         {
            debug_puts("Restart System...");
            restart_system = 0;
           ANX7150_Initial();
        }
        if (!debug_mode)
        {
           ANX7150_Interrupt_Process();
            ANX7150_Timer_Process();
        }
        CommandProcess ();
        delay_ms(5);
    }
```

After ANX7150 initialization is done, the firmware runs in the loop of ANX7150_Interrupt_Process( ), TimerProcess( ) and CommandProcess( ). ANX7150_Interrupt_Process( ) monitors the ANX7150 interrupt events and calls the corresponding service routines for processing.

ANX7150_Timer_Process( ) includes a scheduler that divides pending tasks into four time slots (ANX7150_Timer_Slot1, ANX7150_Timer_Slot2, ANX7150_Timer_Slot3, ANX7150_Timer_Slot4). Each slot lasts

about 8ms. Slot times are defined as follows: ANX7150_Timer_Slot1 is for HPD detection, EDID reading and parsing; ANX7150_Timer_Slot2 is for video/audio/packet configuration; ANX7150_Timer_Slot3 is for HDCP process; ANX7150_Timer_Slot4 is for future usage. Command Process( ) is for debug purposes.

3 Initialization

Power-On Reset: The RESETN input to the ANX7150 is commonly connected to a general purpose input/output (GPIO) pin of the host microcontroller. Firmware is responsible for generating the hardware reset signal of the ANX7150 by pulling down RESETN for a minimum of 2ms.

Locate ANX7150: After asserting RESETN, the firmware should ensure it has established communications with the ANX7150 by confirming that it can read its vendor and device ID registers.

The following program describes the ANX7150 reset and locates process.

```
for (i=0; i<10; i++)
        {
            ANX7150_Resetn_Pin = 0;
            delay_ms(2);
            ANX7150_Resetn_Pin = 1;
            delay_ms(2);

            c = ANX7150_i2c_read_p0_reg(ANX7150_DEV_IDL_REG, &d1);
            if (c) continue;

            c = ANX7150_i2c_read_p0_reg(ANX7150_DEV_IDH_REG, &d2);
            if (c) continue;

            if (d1 == 0x50 && d2 == 0x71)
            {
                debug_puts("ANX7150 detected!");
                return 1;
            }
        }
        debug_puts("device not detected");
```

```
return 0;
```

Register Initialization: After power-on reset, most of the ANX7150 device functions are powered down except for pixel clock detection and Hot Plug Detection. The firmware then needs to configure the other registers appropriately for system operation. Table 3-1 lists the ANX7150 register functions involved in the initialization sequence.

Table 3-1 Register Settings for ANX7150 Initialization

Register Offset	Register Name	Initialized Vale	Purpose
0x72: 0x45	INTR Mask 1	0x04	
0x72: 0x46	INTR Mask 2	0x00	
0x72: 0x47	INTR Mask 3	0x00	
0x72: 0x9A	Chip Control REG	Set bit 0 to 0	Enable auto set clock range for video PLL
0x72: 0xCC	HDCP_BLUESCREEN0_REG	0x10	Initialize the register value of blue screen. When HDCP fails, the ANX7150 sends the blue screen pattern. The initialization value is for a green field in RGB mode.
0x72: 0xCD	HDCP_BLUESCREEN1_REG	0xEB	
0x72: 0xCE	HDCP_BLUESCREEN2_REG	0x10	

4 Wait Hotplug

In Wait Hotplug state, the chip is in a power down mode. The system only responds to Hotplug change interrupt. When a Hotplug interrupt is detected in the interrupt routine, the firmware determines whether the interrupt is a receiver plug-in or a un-plug. If the interrupt is a plug-in, the chip is powered on, and the system is set to Read and Parse EDID.

5 Read and Parse EDID

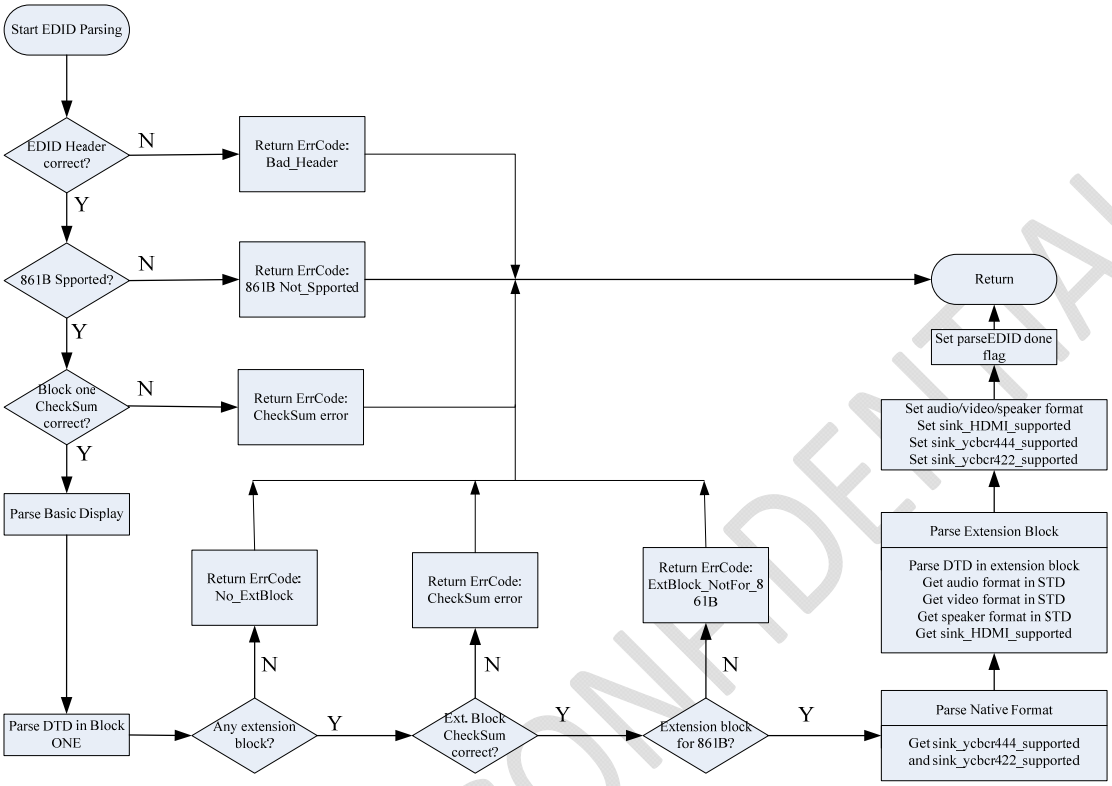

Figure 5-1 Read and Parse EDID Flowchart

Figure 5-1 illustrates EDID parsing. Reading the EDID content from the EEPROM of the receiver across the DDC channel is a simple process. All the EDID data bytes can be read into a MCU local RAM at one time (Enhanced DDC sequential Read), or read piece by piece (Sequential Byte Read) and then parsed on the fly. For the purpose of saving into MCU RAM space, parsing the EDID contents is a complex process. Basically, two fields are important in parsing the EDID: the HDMI or DVI mode (in the “Vender Specific” tag byte data area on extension block #1, HDMI Identifier=0x000c03), and the support capability of YCbCr (byte address 0x03 on extension block #1). This EDID information must be properly transferred from the receiver.

6 Configure Video

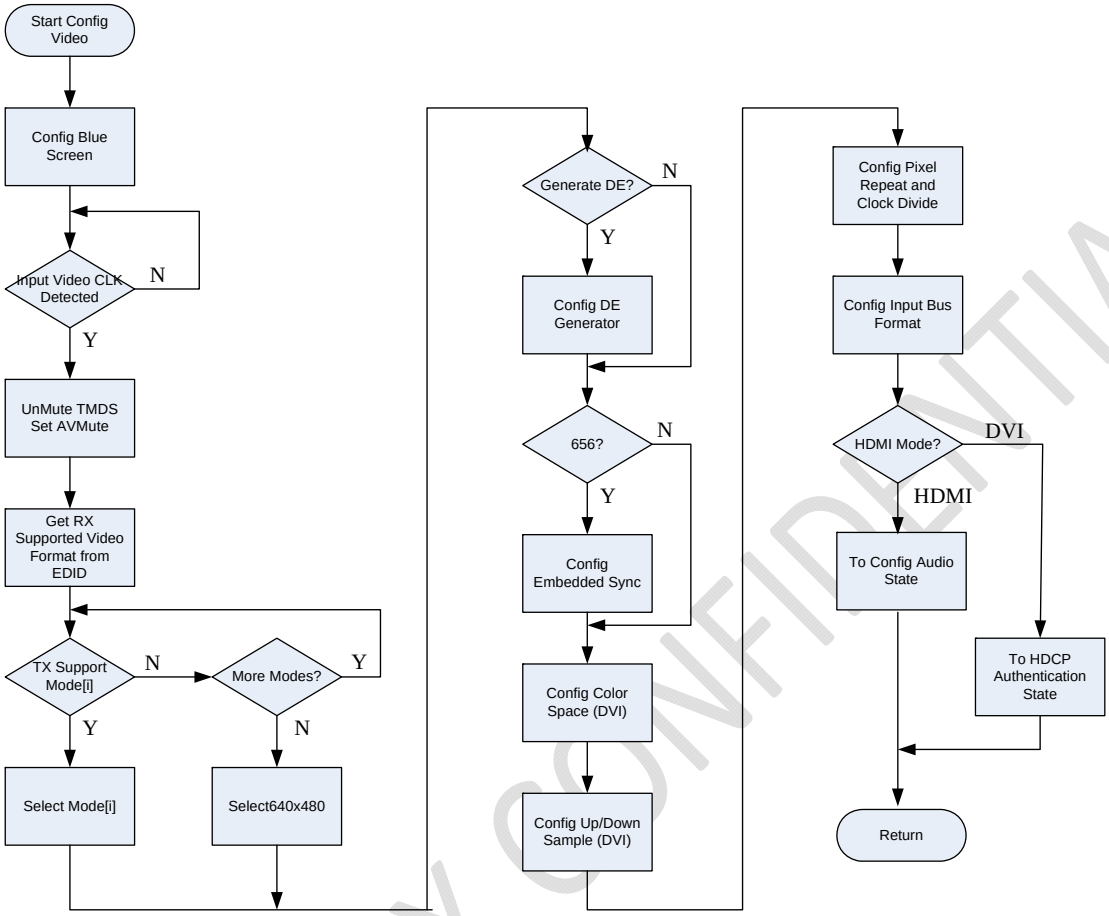

Figure 6-1 Video Configuration Flowchart

Figure 6-1 illustrates the basic video configuration process.

At the beginning of video configuration, the firmware initializes the blue screen registers according to the video format (RGB, YCbCr4:4:4 or YCbCr4:2:2). If HDCP authentication fails, the firmware terminates HDCP encryption and enables the blue screen output instead of normal video output.

After the input pixel clock is detected, the firmware un-mutes the TMDS link (Register 0x72:0x99, bit 7) and sets AVMute.

Based on the parsing result of EDID and the capability of the video source, the transmitter selects a preferred video format to send. If required, DE generator, embedded SYNC, color space, and pixel up-sample are configured.

If HDMI mode is selected, the firmware goes to the Config Audio state. If DVI mode is selected, the firmware goes to the HDCP Authentication state without Config Video and Config packets.

A number of difference video formats are supported by the ANX7150 chip. The supported video formats are listed in the HDMI transmitter design specification. Based on the configuration process of video, the video interface format is configured by the controller writing to the following registers.

6.1 Video Format Capture

- **RGB and YcbCr 4:4:4 Formats with Separate Syncs (24-bpp mode)**
- **YCbCr 4:2:2 Formats with Separate Syncs**
- **YCbCr 4:2:2 Formats with Embedded Syncs**

Setting EMB_SYNC_MODE bit-6 of Video Capture Control register #0 (0x72:0x13) to enable de-embedded sync.

- **YC Mux 4:2:2 Formats with Separate Sync**

Configure VID_YC_BIT_SEL bit-3 of Video Control register (0x72:0x12) and DEMUX_YC_EN bit-5 of Video Capture Control register #0 (0x72:0x13) to enable YC-Mux 4:2:2 Formats with bit-mapping options.

	bit-mapping option 1	**bit-mapping option 2**
VID_YC_BIT_SEL	0x0	0x1

- **YC Mux 4:2:2 with Embedded Sync**

Setting EMB_SYNC_MODE bit-6 of Video Capture Control register #0 (0x72:0x13) to enable de-embedded sync. Configure VID_YC_BIT_SEL bit-3 of Video Control register (0x72:0x12) and DEMUX_YC_EN bit-5 of Video Capture Control register #0 (0x72:0x13) to enable YC-Mux 4:2:2 Formats with bit-mapping options.

	bit-mapping option 1	**bit-mapping option 2**
VID_YC_BIT_SEL	0x0	0x1

- **12-bit RGB and YCbCr 4:4:4 DDR Formats with Separate Syncs (24-bpp)**

Setting DV_BUS_MODE bit-3 of Video Capture Control register #0 (0x72:0x13) to enable Dual-Data-Rate (DDR) mode.

- **12-bit RGB and YCbCr 4:4:4 DDR Formats with Separate Syncs (18-bpp)**

Setting DV_BUS_MODE bit-3 of Video Capture Control register #0 (0x72:0x13) to enable Dual-Data-Rate (DDR) mode.

6.2 Color Space Convert and Up-sample

When the input video data are YCbCr 4:4:4 for DVI mode, color space convert configuration is necessary. Set CSPACE_Y2R of Video Mode register (0x72:0x11) bit-4 to enable the color space converter. When the input video data are YCbCr 4:2:2 for DVI mode, color space convert and up-sample must be set. Set UP_SAMPLE of Video Mode register (0x72:0x11) bit-2 to enable up-sample. RANGE_Y2R and Y2R_SEL are used for color space convert.

6.3 Pixel Repeat and Clock Divide

There is a video FIFO with 4 * 3 bytes size to convert video data from IDCK to HDMI link clock domain. This FIFO also can perform pixel repetition and clock divide for some combinations of video input clock frequency and audio sampling rate. The value of pixel repetition is determined by the input video clock frequency and link pixel data clock frequency. IN_PIXEL_RPT (0x72:0x11 bits 0, 1), TR_PIXEL_RPT (0x72:0x12 bits 0, 1) and DEMUX_YC_EN (0x72:0x13 bit 5) must be set properly and reflect the format relationship of input video data and output link data.

6.4 Register Set for Embedded Sync Decode

When input video stream is embedded sync encoded, the EMB_SYNC_MODE (0x72:0x13 bit-6) should be configured with 1. To decode embedded sync correctly, the following registers must be configured:

a) VSYNC_POL (0x72:0x14 bit-6)

b) HSYNC_POL (0x72:0x14 bit-5)

c) VSYNC_FP_LINE (0x72:0x23)

d) VSYNC_ACT_WID_LINE (0x72:0x24)

e) VH_FP_LOW(0x72:0x19) VH_FP_HIGH (0x72:0x1A) horizon_front_porch

f) HSYNC_WIDTH (0x72:0x1B and 0x72:0x1C) horizon_sync_width

g) INV_FLD_POL (0x72:0x14 bit-4) invert_field_polarity (optional)

6.5 Register Set for DE Generator

When the user wants to re-generate the DE signal, the DE_GEN_EN (0x72:0x13 bit-7) should be configured with 1. To re-generation the DE signal correctly, the following registers must be configured:

1. VSYNC_POL (0x72:0x14 bit-6)
2. HSYNC_POL (0x72:0x14 bit-5)
3. ACT_LINE (0x72:0x21 and 0x72:0x22) active_lines
4. VV_RES (0x72:0x1F and 0x72:0x20) total_lines
5. VSYNC_ACT_WID_LINE (0x72:0x24)
6. VSYNC_BP_LINE (0x72:0x25) vertical_back_porch
7. ACT_PIX (0x72:0x17 and 0x72:0x18) active_pixels
8. VH_RES_LOW and VH_RES_HIGH (0x72:0x15 and 0x72:0x16) total_pixels
9. HSYNC_WIDTH (0x72:0x1B and 0x72:0x1C) horizon_sync_width

10. VH_BP_LOW and VH_BP_HIGH (0x72:0x1D and 0x72:0x1E) horizon_back_porch
11. VIDEO_TYPE (0x72:0x14 bit-3)

The video register set from 0x72:0x26 to 0x72:0x36 is used by the firmware to check the input video format parameters.

Note: After configuring the corresponding video registers, the firmware should set VID_IN_EN of Video Control Register (0x72:0x12 bit-4) to turn on video capture input.

7 Configure Audio

As Figure 7-1 illustrates, the ANX7150 supports three audio input formats including SPDIF, I^2S, and Super Audio.

Audio source select: At the beginning of audio configuration, the firmware must select the audio source by setting Audio Control Register#1(0x72: 0x51).

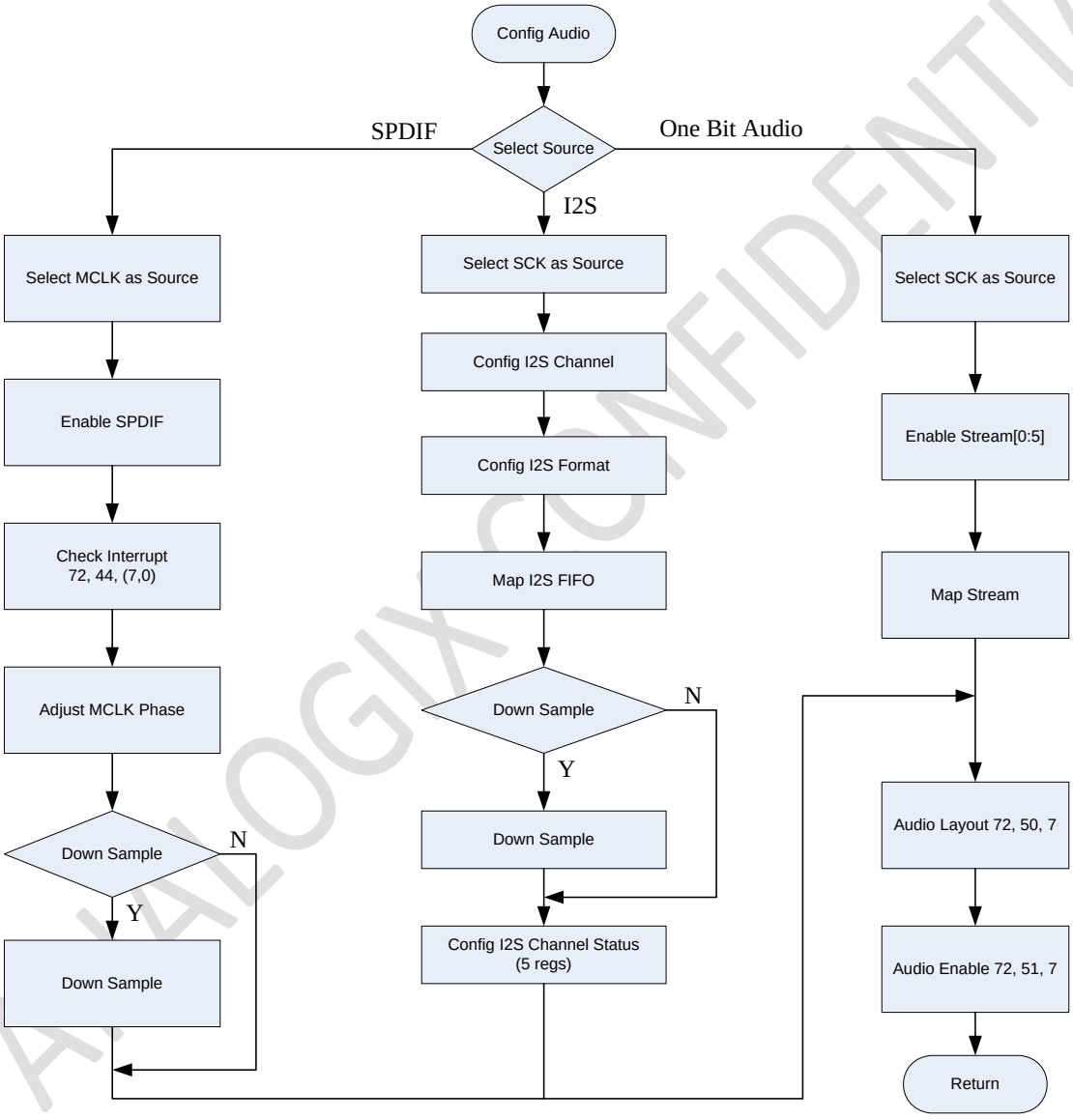

Figure 7-1 Audio Configuration Flowcharts

7.1 Audio Clock Source Select for CTS Generation

The ANX7150 can support MCLK and SCK (64*f_s) for CTS generation. Configure CTS_ GEN_SC to select the CTS generation source clock. When using MCLK, the firmware needs to configure FREQ_MCLK of register HDMI Audio Control Register #0 (0x72:0x50).

7.2 SPDIF Format Configure and Clock Phase Control

Because the input MCLK phase is uncertain with SPDIF data, the firmware needs to check the SPDIF_ERR, SPDIF_BI_PHASE_ERR, and SPDIF_UNSTBL interrupts status. If a SPDIF error is detected, the firmware should configure the register INV_AUD_CLK (0x72:0x50 bit-3) and MCLK_PHS_CTRL (0x72:0x52 bit 5 and bit 6) with the following values.

Table 7-1 Value of the register INV_AUD_CLK and MCLK_PHS_CTRL

FREQ_MCLK	INV_AUD_CLK	MCLK_PHS_CTRL
128*Fs	1'b1	n/a
256*Fs	n/a	2'b01
384*Fs	n/a	2'b01 or 2'b10
512*Fs	n/a	2'b10

When using the SPDIF as input audio source, the firmware should read the FS_FREQ and WORD_SIZE from Input Audio SPDIF Channel Status Register (0x72:0x55). If the value of FS_FREQ is not correct, the firmware should configure FS_FREQ of Audio I2S Channel Status Register #4 (0x72:0x59) with the correct value and set SPDIF_FS_OVRWR of HDMI Audio Control Register #1 (0x72:0x51).

7.3 I2S Format Configure

When selecting the I^2S input source, the firmware should configure I^2S Format Control Register (0x72:0x52) and I^2S Channel Status Register 1 to Register 5. The I^2S capture block decodes the input audio data based on settings of SHIFT_CTRL, DIR_CTRL, WS_POL and JUST_CTRL of register 0x72:0x52.

7.4 Super Audio Configure (TBD)

7.5 Audio Down Sample

The ANX7150 supports audio down sample 2-to-1 or 4-to-1. When the sample frequency of input audio needs to be reduced, the firmware should configure AUD_DOWN_SMPL of HDMI Audio Control Register #0 (0x72:0x50). If the audio source is SPDIF, the firmware should also configure FS_FREQ and SPDIF_FS_OVRWR.

After selecting the input audio source, the firmware should configure the HDMI_AUD_LAYOUT of HDMI Audio Control Register #0 (0x72:0x50 bit-7) based on the audio channel number. After configuring the corresponding audio registers, the firmware should set AUD_IN_EN of HDMI Audio Control Register #1 (0x72:0x51 bit-7) to enable audio data path.

8 Configure Auxiliary Information Packets

The detailed auxiliary information carried from source to DTV monitor is described in the HDMI 1.1 Specification (Section 8) and EIA/CEA-861C Specification (Section6).

Note: In ANX7150 Firmware Rev. 1.0, only AVI infoframe and audio infoframe are implemented. The Vender Specific, MPEG source, ACP, ISRC1, ISRC2 infoframe will be added in the firmware future release.

The AVI infoframe location in the ANX7150 is showed in Table 8-1.

Table 8-1 AVI infoframe location

Register Address	Name	Type	Default	Description
0x7A:0x00	AVI_HB0 (Type)	R/W	0x00	Type
0x7A:0x01	AVI_HB1 (Version)	R/W	0x00	Version
0x7A:0x02	AVI_HB2 (Length)	R/W	0x00	Length
0x7A:0x03	AVI_PB0	R/W	0x00	Checksum
0x7A:0x04	AVI_PB1	R/W	0x00	AVI Data Byte 1
0x7A:0x05	AVI_PB2	R/W	0x00	AVI Data Byte 2
0x7A:0x06	AVI_PB3	R/W	0x00	AVI Data Byte 3
0x7A:0x07	AVI_PB4	R/W	0x00	AVI Data Byte 4
0x7A:0x08	AVI_PB5	R/W	0x00	AVI Data Byte 5
0x7A:0x09	AVI_PB6	R/W	0x00	AVI Data Byte 6
0x7A:0x0A	AVI_PB7	R/W	0x00	AVI Data Byte 7
0x7A:0x0B	AVI_PB8	R/W	0x00	AVI Data Byte 8
0x7A:0x0C	AVI_PB9	R/W	0x00	AVI Data Byte 9
0x7A:0x0D	AVI_PB10	R/W	0x00	AVI Data Byte 10
0x7A:0x0E	AVI_PB11	R/W	0x00	AVI Data Byte 11
0x7A:0x0F	AVI_PB12	R/W	0x00	AVI Data Byte 12
0x7A:0x10	AVI_PB13	R/W	0x00	AVI Data Byte 13
0x7A:0x11	AVI_PB14	R/W	0x00	AVI Data Byte 14
0x7A:0x12	AVI_PB15	R/W	0x00	AVI Data Byte 15

The Audio infoframe location in ANX7150 is showed in Table 8-2.

Table 8-2 Audio Infoframe's location

Register Address	Name	Type	Default	Description
0x7A:0x20	Audio_HB0 (Type)	R/W	0x00	Audio InfoFrame packet type.
0x7A:0x21	Audio_HB1	R/W	0x00	Version
0x7A:0x22	Audio_HB2	R/W	0x00	Length
0x7A:0x23	Audio_PB0	R/W	0x00	Checksum

0x7A:0x24	Audio_PB1	R/W	0x00	Audio InfoFrame Data Byte 1
0x7A:0x25	Audio_PB2	R/W	0x00	Audio InfoFrame Data Byte 2
0x7A:0x26	Audio_PB3	R/W	0x00	Audio InfoFrame Data Byte 3
0x7A:0x27	Audio_PB4	R/W	0x00	Audio InfoFrame Data Byte 4
0x7A:0x28	Audio_PB5	R/W	0x00	Audio InfoFrame Data Byte 5
0x7A:0x29	Audio_PB6	R/W	0x00	Audio InfoFrame Data Byte 6
0x7A:0x2A	Audio_PB7	R/W	0x00	Audio InfoFrame Data Byte 7
0x7A:0x2B	Audio_PB8	R/W	0x00	Audio InfoFrame Data Byte 8
0x7A:0x2C	Audio_PB9	R/W	0x00	Audio InfoFrame Data Byte 9
0x7A:0x2D	Audio_PB10	R/W	0x00	Audio InfoFrame Data Byte 10

Figure 8-1 illustrates infoframe packets configuration. When processing a new packet, the firmware gets the packet type and determines whether it is a new packet or not. If a new packet comes, according to the packet type, the firmware disables the transmission enable bit and repeat bit of this kind of packet in the Infoframe Packet Control Register 1 (0x7A:0xC0). For example, if a new AVI infoframe packet is received, the firmware should disable bit 4 and bit 5. Then, the firmware configures the packet type, version, length and calculates the checksum. After the packet has been loaded to the registers, the firmware enables the corresponding enable bit and repeat bit in the Infoframe Packet Control Register 1 (0x7A:0xC0).

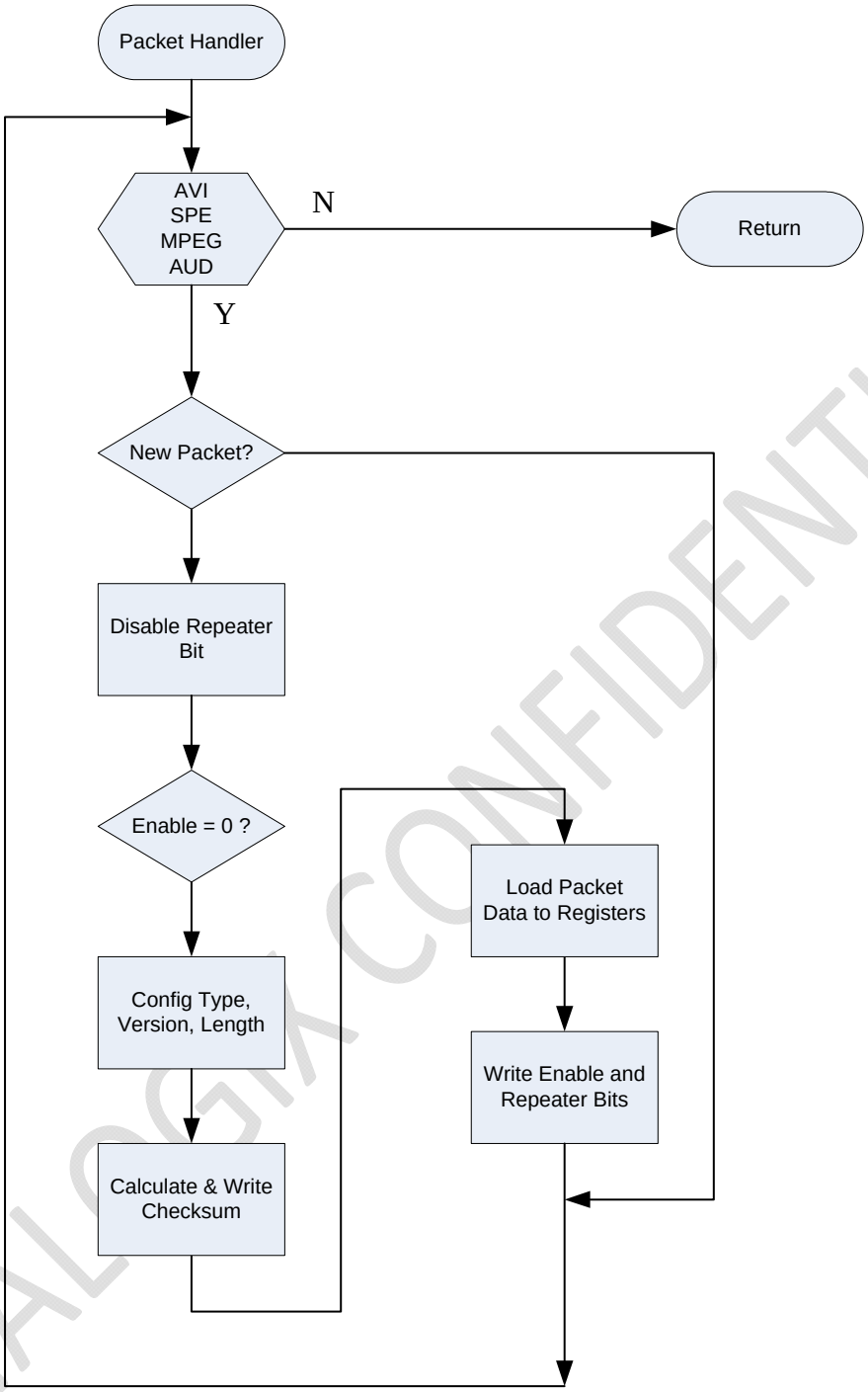

Figure 8-1 Infoframe Packets Configuration Flowchart

9 HDCP Authentication

ANX7150 Evaluation Board supports HDCP enable/disable by setting the dip switch #4 of piano switch (S10). Setting to 1 means enable HDCP, and setting to 0 means disable HDCP.

In HDMI link mode, after infoframe packets configuration is complete, the firmware enters the HDCP authentication state. In DVI link mode, the firmware enters the HDCP authentication state when video configuration is complete.

The ANX7150 supports two HDCP authentication methods: Hardware HDCP authentication and Software HDCP authentication. In ANX7150 Firmware Rev1.0, only use the Hardware HDCP authentication. In a future firmware release, the Software HDCP authentication will be added as an optional feature.

Figure 9-1 illustrates the initialization process of HDCP authentication. The transmitter reads the BCAPS(0x74:0x40) and BStatus register(0x74:0x41 and 0x74:0x42) of the receiver through the DDC channel to get information whether the receiver supports the HDMI mode and the HDCP 1.1 feature.

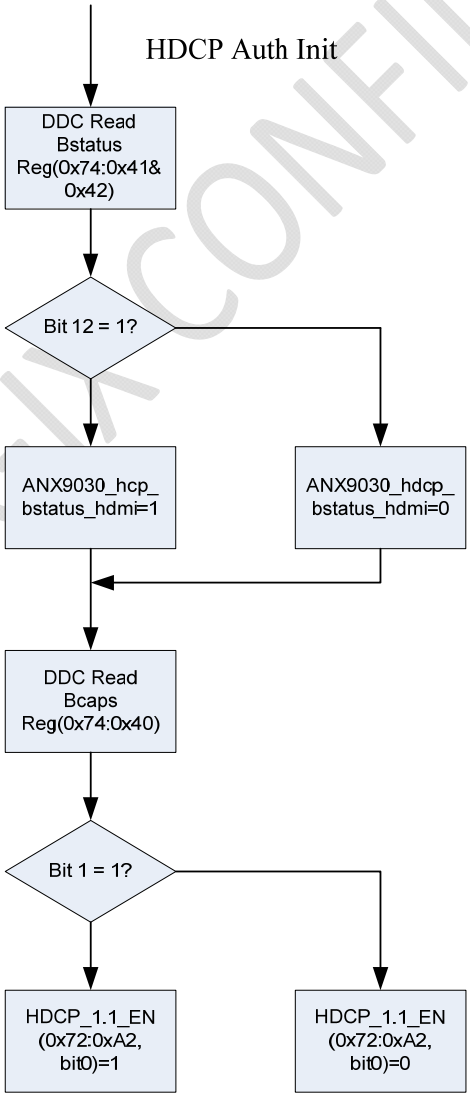

Figure 9-1 Initialization of HDCP Authentication

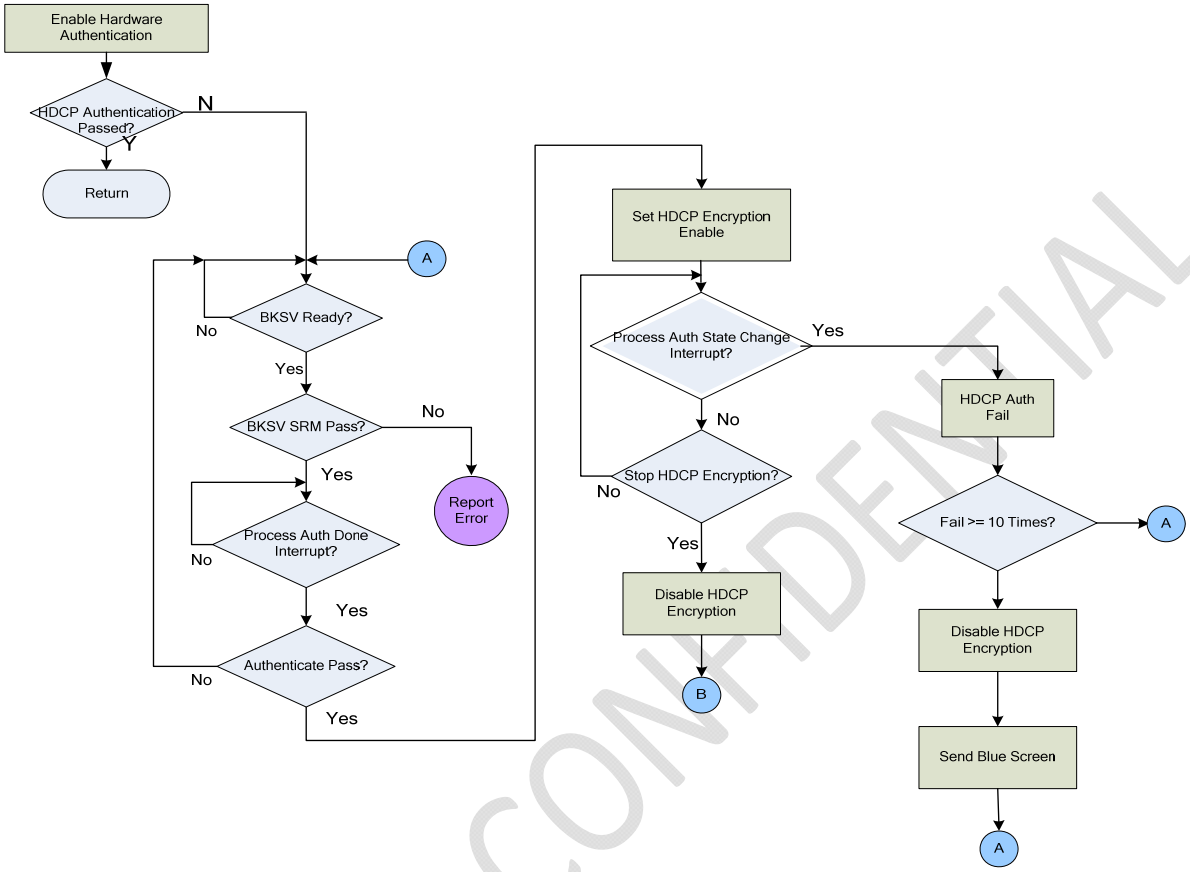

Figure 9-2 Hardware HDCP Authentication Flowchart

Figure 9-2 illustrates the Hardware HDCP authentication. When selecting hardware method for HDCP authentication, the firmware configures the HARD_AUTH_EN (0x72:0xA1 bit-3) to start the HDCP authentication process, and then check whether BKSV is on a revocation list. After authentication completes successfully, the firmware sets HDCP_ENC_EN (0x72:0xA1 bit-3) to enable HDCP encryption.

BKSV SRM Check: KSV SRM check is described in Part 5 of the HDCP Standard. The ANX7150 supports BKSV SRM check performed by software. When processing the BKSV_RDY (Interrupt Status Register 2 0x72:0x43 bit-4) interrupt, the firmware reads out the 5-byte BKSV from the BKSV register 0x72:0xB2~0xB6 and checks whether the BKSV is on a revocation list. If the BKSV SRM check is ok, the firmware writes BKSV_SRM_PASS and KSVLIST_VLD (0x72:0xA1 bit-1 and bit-0) to "1."

HDCP Authentication Monitor and Control: When processing the AUTH_DONE (Interrupt Status Register 2 0x72:0x43 bit-0) interrupt, the firmware reads AUTHEN_PASS (0x72:0xA0 bit-1) and determines whether the hardware authentication has completed properly or not. If authentication passes, the firmware enables HDCP encryption.

When processing the AUTH_STATE_CHG (Interrupt Status Register 2 0x72:0x43 bit-1) interrupt in normal work mode, the firmware reads AUTHEN_PASS (0x72:0xA0 bit-1) to confirm that the hardware authentication failed and then to disable the encryption. Hardware will do re-authentication immediately. When authentication failed times exceeds 10, the firmware should send blue screen until authentication passes again.

10 Playback

Playback is the normal work mode of ANX7150 firmware. When entering the Playback state, if AVMUTE is already set, the firmware should clear the AVMUTE.

11 Interrupt Process

The ANX7150 has interrupt sources such as Hotplug change, Video format change, and so on. Once an interrupt event occurs, the corresponding bit in the interrupt register is set. When firmware enters the interrupt process routine, these bits will be recorded and cleared, and then the corresponding interrupt will be handled. Figure 11-1, Figure 11-2, Figure 11-3 and Figure 11-4 illustrate the interrupt process flowchart.

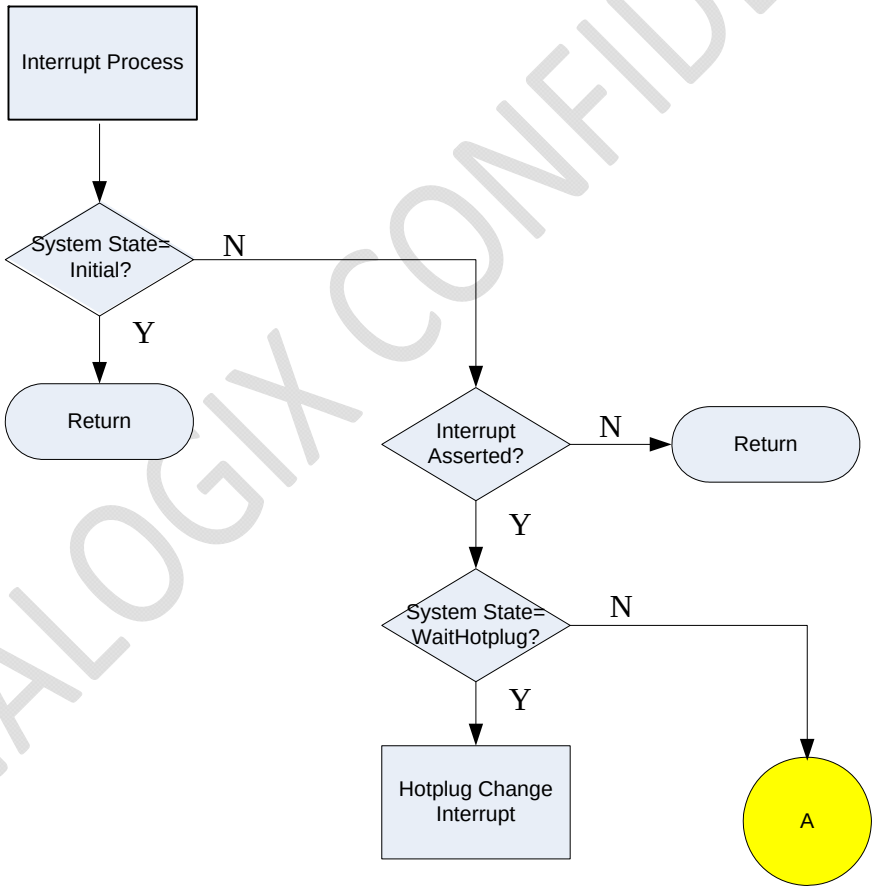

Figure 11-1 Interrupt Process Flowchart (1)

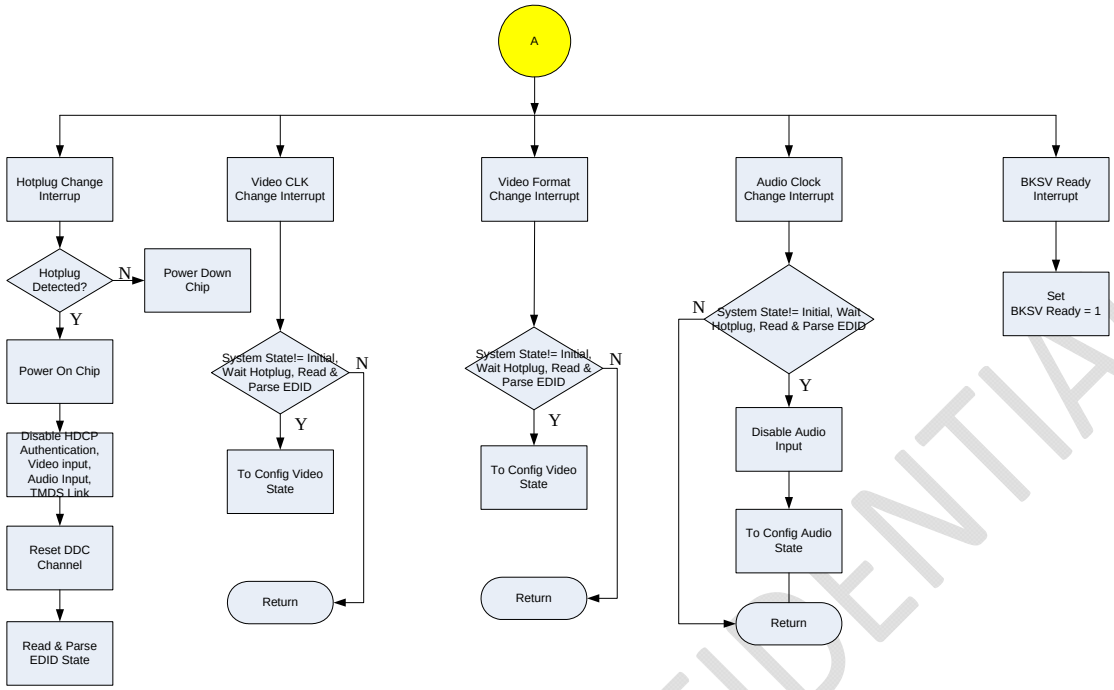

Figure 11-2 Interrupt Process Flowchart (2)

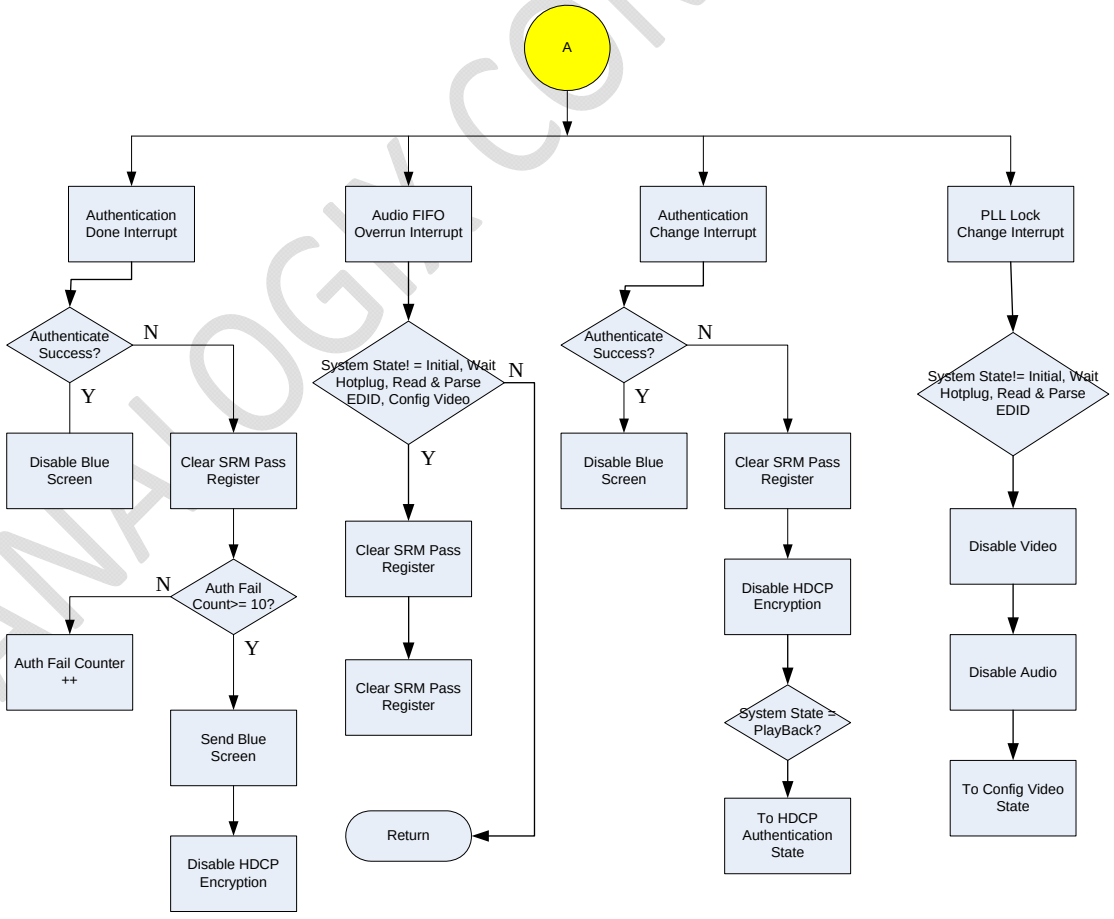

Figure 11-3 Interrupt Process Flowchart (3)

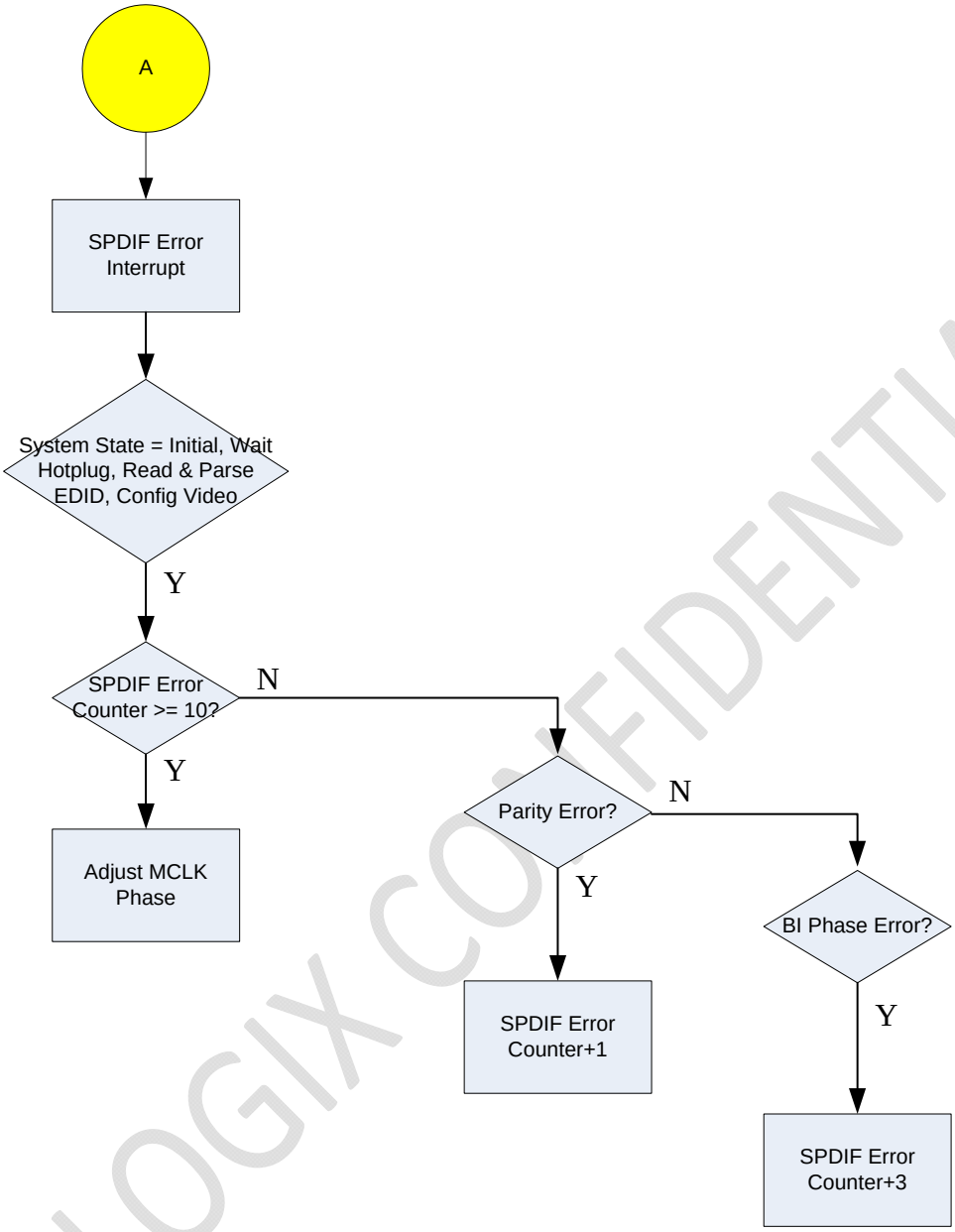

Figure 11-4 Interrupt Process Flowchart (4)

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