

N-Channel 20-V (D-S) MOSFET with Trench Schottky Diode

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)
20	0.225 at V _{GS} = 4.5 V	1.5	1.1 nC
	0.270 at V _{GS} = 2.5 V	1.5	
	0.345 at V _{GS} = 1.8 V	1.5	
	0.960 at V _{GS} = 1.5 V	0.5	

SCHOTTKY PRODUCT SUMMARY		
V _{KA} (V)	V _f (V) Diode Forward Voltage	I _F (A) ^a
30	0.29 at 10 mA	0.4

FEATURES

- Halogen-free According to IEC 61249-2-21
- LITTLE FOOT[®] Plus Schottky Power MOSFET
- New Thermally Enhanced PowerPAK[®] SC-75 Package
 - Small Footprint Area
 - Low On-Resistance
 - Thin 0.75 mm profile
- Typical ESD Protection 2800 V

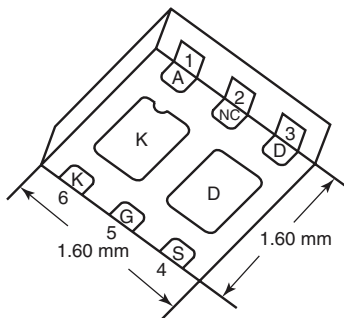


RoHS
COMPLIANT
HALOGEN
FREE

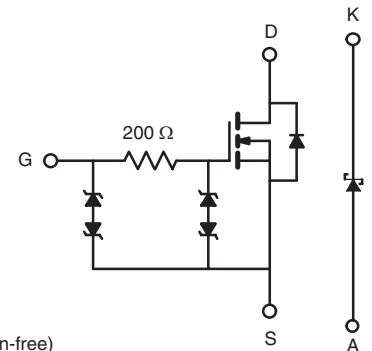
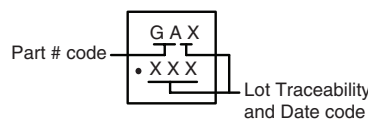
APPLICATIONS

- Portable Devices
- DC/DC Converters

PowerPAK SC75-6L-Dual



Marking Code



Ordering Information: SiB800EDK-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted					
Parameter	Symbol	Limit	Unit		
Drain-Source Voltage (MOSFET)	V _{DS}	20	V		
Reverse Voltage (Schottky)	V _{KA}	30			
Gate-Source Voltage (MOSFET)	V _{GS}	± 6			
Continuous Drain Current (T _J = 150 °C) (MOSFET)	I _D	T _C = 25 °C	1.5 ^a	A	
		T _C = 70 °C	1.5 ^a		
		T _A = 25 °C	1.5 ^{a, b, c}		
		T _A = 70 °C	1.3 ^{b, c}		
Pulsed Drain Current (MOSFET)	I _{DM}	4	A		
Continuous Source-Drain Diode Current (MOSFET Diode Conduction)	I _S	T _C = 25 °C			1.5 ^a
		T _A = 25 °C			0.9 ^{b, c}
Average Forward Current (Schottky)	I _F	0.4 ^b	A		
Pulsed Forward Current (Schottky)	I _{FM}	0.8			
Maximum Power Dissipation (MOSFET)	P _D	T _C = 25 °C	3.1	W	
		T _C = 70 °C	2		
		T _A = 25 °C	1.1 ^{b, c}		
		T _A = 70 °C	0.7 ^{b, c}		
Maximum Power Dissipation (Schottky)	P _D	T _C = 25 °C	3.1		
		T _C = 70 °C	2		
		T _A = 25 °C	1.1 ^{b, c}		
		T _A = 70 °C	0.7 ^{b, c}		
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C		
Soldering Recommendations (Peak Temperature) ^{d, e}		260			



THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient (MOSFET) ^{b, f}	$t \leq 5$ s	R_{thJA}	90	115	°C/W
Maximum Junction-to-Case (Drain) (MOSFET)	Steady State	R_{thJC}	32	40	
Maximum Junction-to-Ambient (Schottky) ^{b, f}	$t \leq 5$ s	R_{thJA}	90	115	
Maximum Junction-to-Case (Drain) (Schottky)	Steady State	R_{thJC}	32	40	

Notes:

- Package limited.
- Surface Mounted on 1" x 1" FR4 board.
- $t = 5$ s.
- See Solder Profile (www.vishay.com/ppg?73257). The PowerPAK SC-75 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under Steady State conditions is 125 °C/W.

SPECIFICATIONS $T_J = 25$ °C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0$ V, $I_D = 250$ μ A	20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250$ μ A		21		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			-2.3		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250$ μ A	0.4		1.0	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 3$ V			± 1	μ A
		$V_{DS} = 0$ V, $V_{GS} = \pm 6$ V			± 1	mA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20$ V, $V_{GS} = 0$ V			1	μ A
		$V_{DS} = 20$ V, $V_{GS} = 0$ V, $T_J = 55$ °C			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5$ V, $V_{GS} = 4.5$ V	4			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 4.5$ V, $I_D = 1.6$ A		0.183	0.225	Ω
		$V_{GS} = 2.5$ V, $I_D = 1.5$ A		0.220	0.270	
		$V_{GS} = 1.8$ V, $I_D = 1.3$ A		0.275	0.345	
		$V_{GS} = 1.5$ V, $I_D = 0.3$ A		0.320	0.960	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10$ V, $I_D = 1.6$ A		3.5		S
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 10$ V, $V_{GS} = 4.5$ V, $I_D = 1.7$ A		1.1	1.7	nC
Gate-Source Charge	Q_{gs}			0.2		
Gate-Drain Charge	Q_{gd}			0.1		
Gate Resistance	R_g	$f = 1$ MHz		200		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10$ V, $R_L = 7.7$ Ω $I_D \cong 1.3$ A, $V_{GEN} = 4.5$ V, $R_g = 1$ Ω		20	30	ns
Rise Time	t_r			12	20	
Turn-Off Delay Time	$t_{d(off)}$			70	105	
Fall Time	t_f			20	30	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25$ °C			1.5	A
Pulse Diode Forward Current	I_{SM}				4	
Body Diode Voltage	V_{SD}	$I_S = 1.3$ A, $V_{GS} = 0$ V		0.9	1.2	V

Notes:

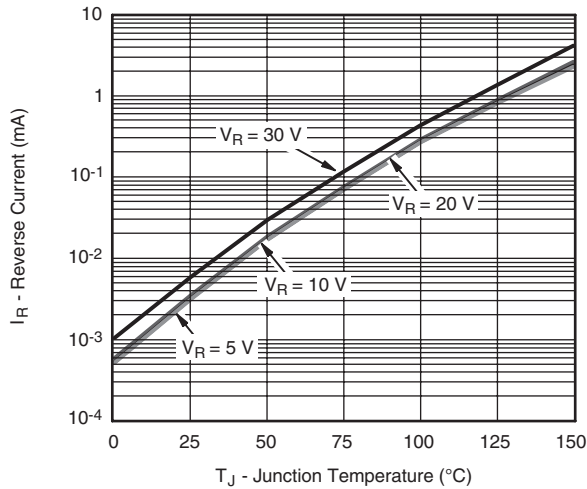
- Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %.
- Guaranteed by design, not subject to production testing.



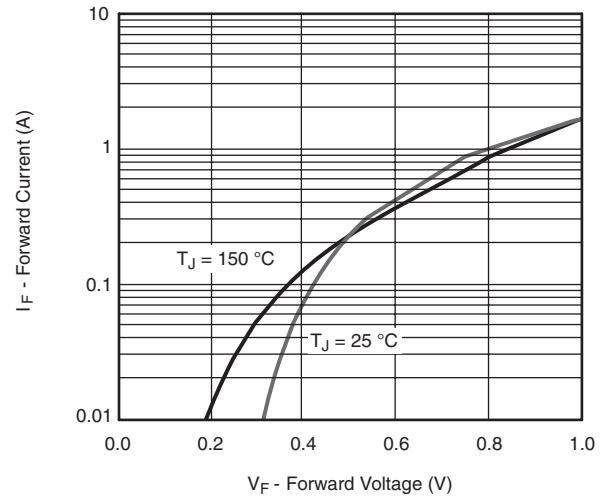
SCHOTTKY SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Forward Voltage Drop	V_F	$I_F = 10\text{ mA}$		0.23	0.29	V
		$I_F = 10\text{ mA}, T_J = 125\text{ }^\circ\text{C}$		0.11	0.14	
		$I_F = 0.1\text{ A}$		0.32	0.38	
Maximum Reverse Leakage Current	I_{rm}	$V_r = 20\text{ V}$		0.005	0.050	mA
		$V_r = 20\text{ V}, T_J = 85\text{ }^\circ\text{C}$		0.150	1.5	
Junction Capacitance	C_T	$V_r = 15\text{ V}$		16		pF

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

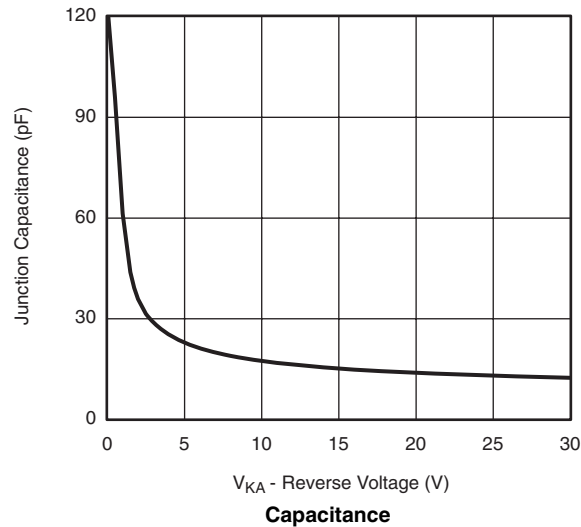
SCHOTTKY TYPICAL CHARACTERISTICS $T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted



Reverse Current vs. Junction Temperature



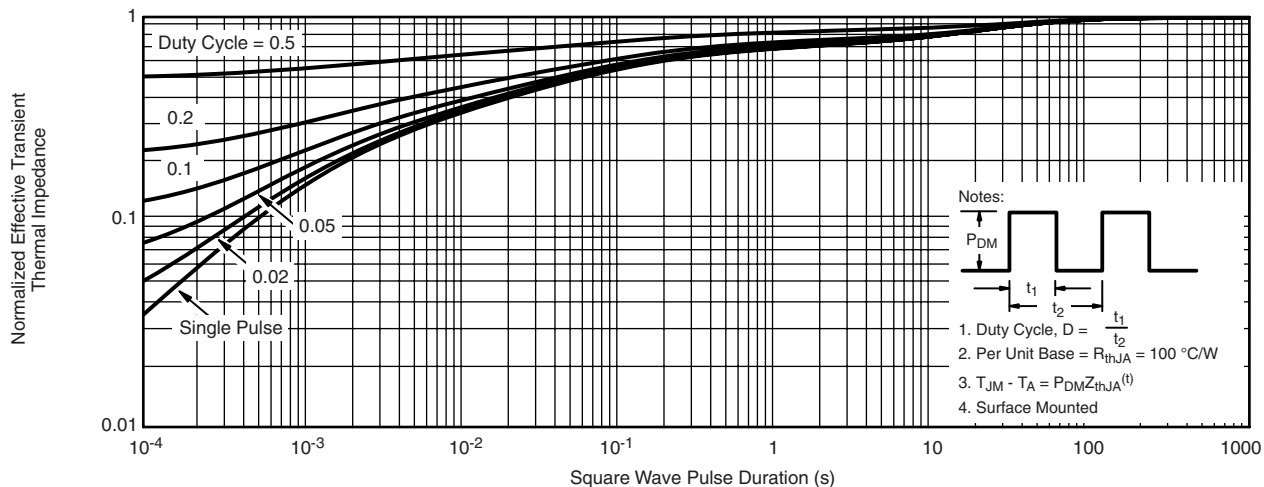
Forward Voltage Drop



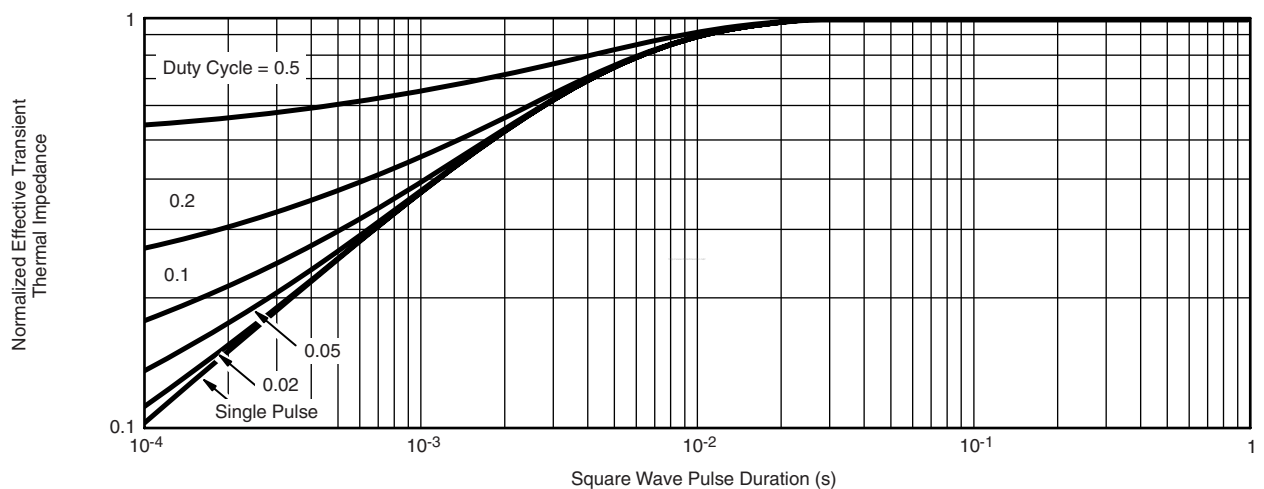
Capacitance



SCHOTTKY TYPICAL CHARACTERISTICS $T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted

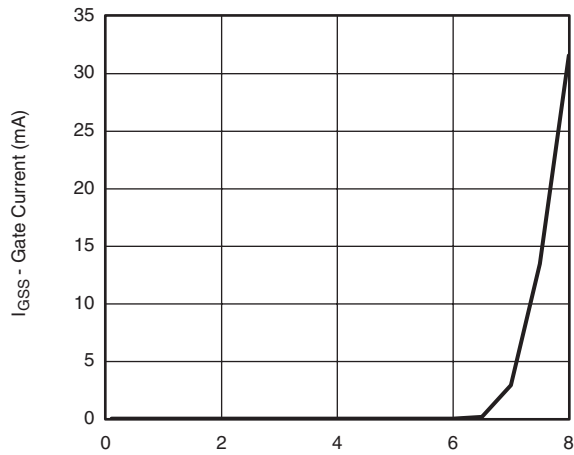


Normalized Thermal Transient Impedance, Junction-to-Ambient

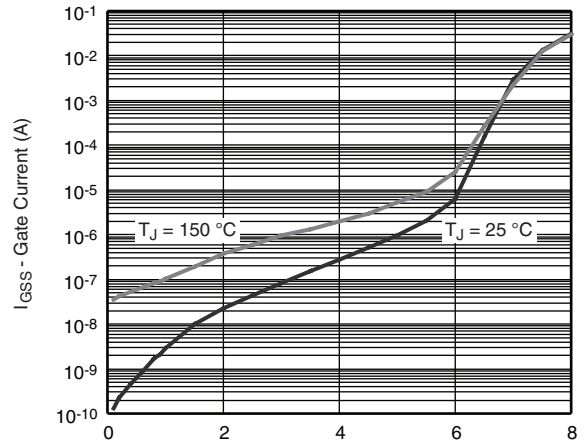


Normalized Thermal Transient Impedance, Junction-to-Case

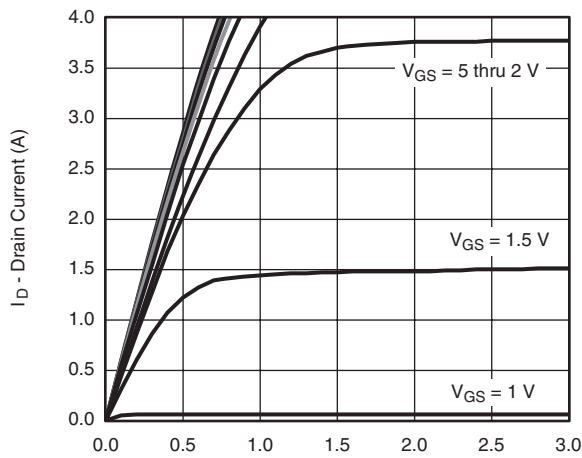
MOSFET TYPICAL CHARACTERISTICS $T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted



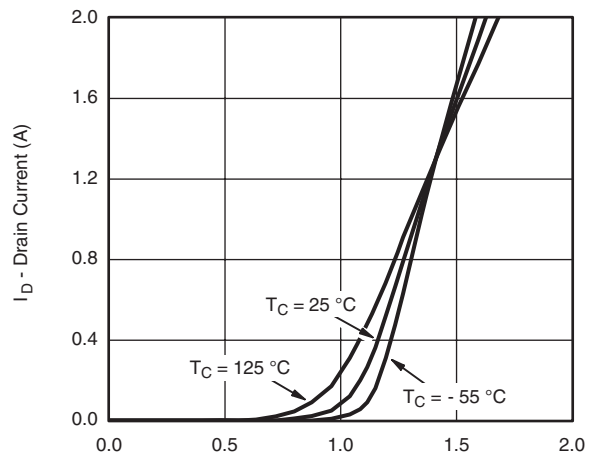
I_{GSS} - Gate Current (mA)
 V_{GS} - Gate-to-Source Voltage (V)
Gate Current vs. Gate-to-Source Voltage



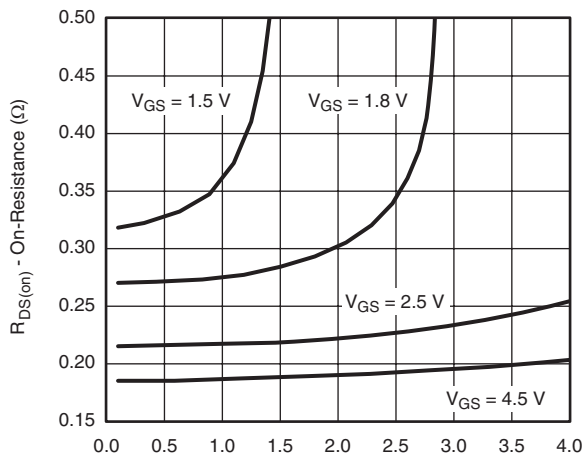
I_{GSS} - Gate Current (A)
 V_{GS} - Gate-to-Source Voltage (V)
Gate Current vs. Gate-to-Source Voltage



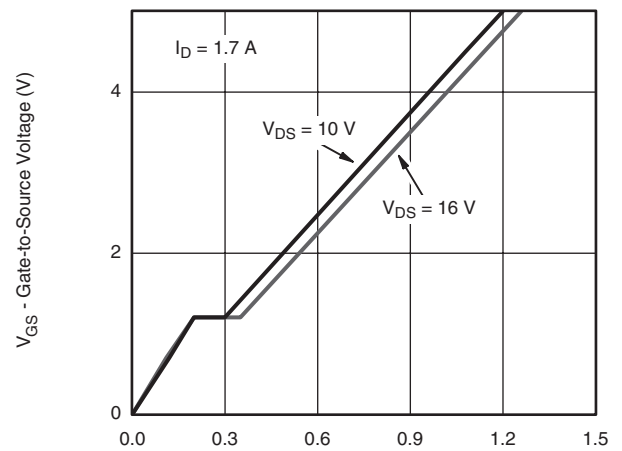
I_D - Drain Current (A)
 V_{DS} - Drain-to-Source Voltage (V)
Output Characteristics



I_D - Drain Current (A)
 V_{GS} - Gate-to-Source Voltage (V)
Transfer Characteristics



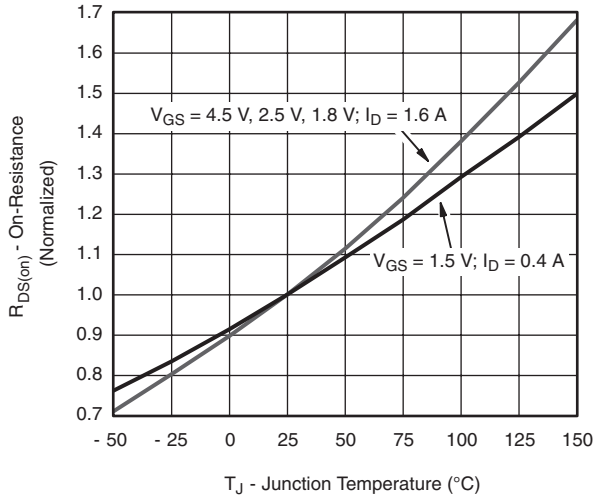
$R_{DS(on)}$ - On-Resistance (Ω)
 I_D - Drain Current (A)
On-Resistance vs. Drain Current



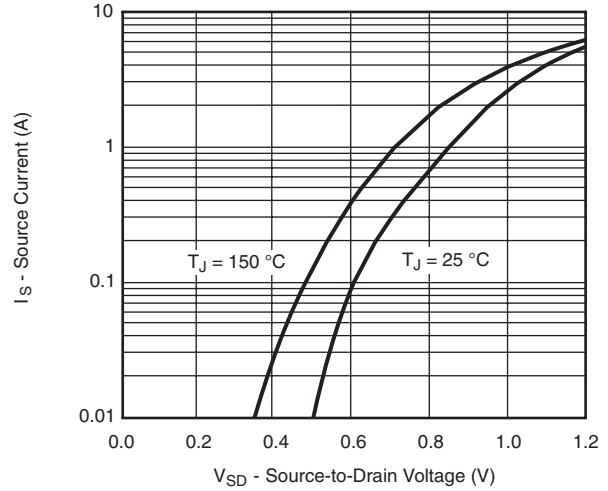
V_{GS} - Gate-to-Source Voltage (V)
 Q_g - Total Gate Charge (nC)
Gate Charge



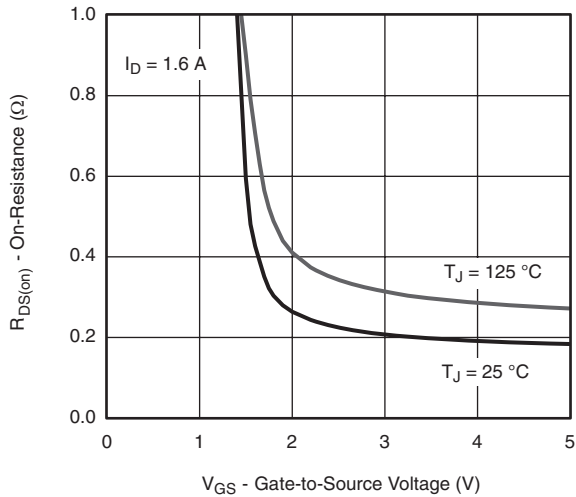
MOSFET TYPICAL CHARACTERISTICS $T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted



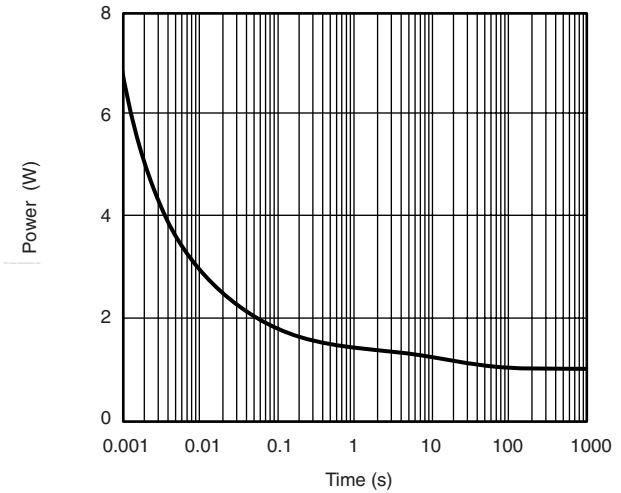
Normalized On-Resistance vs. Junction Temperature



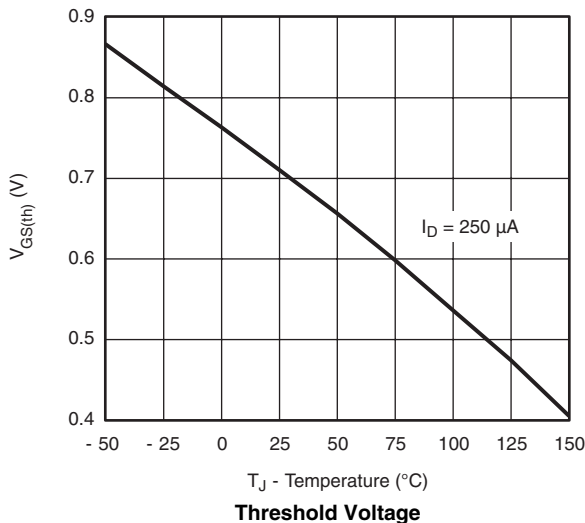
Source-Drain Diode Forward Voltage



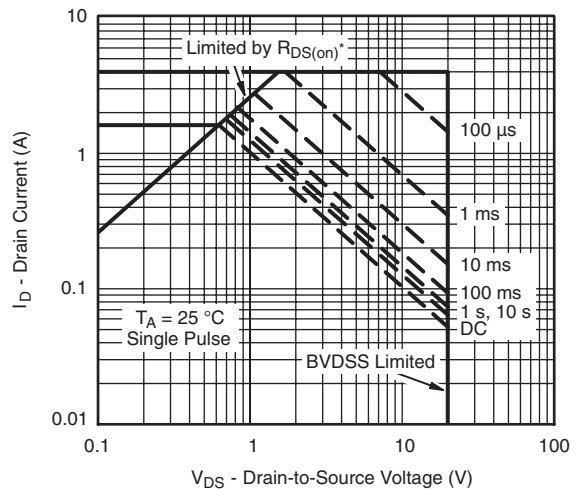
On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient



Threshold Voltage

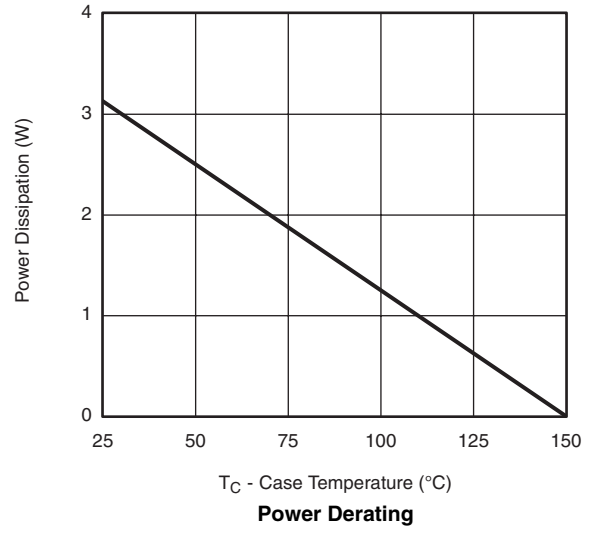
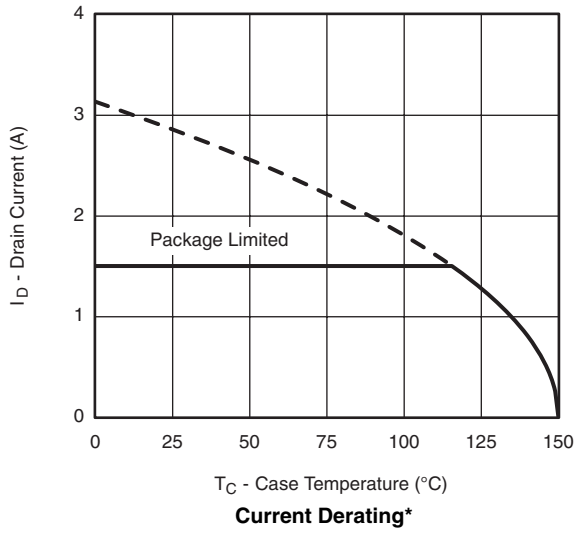


* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient



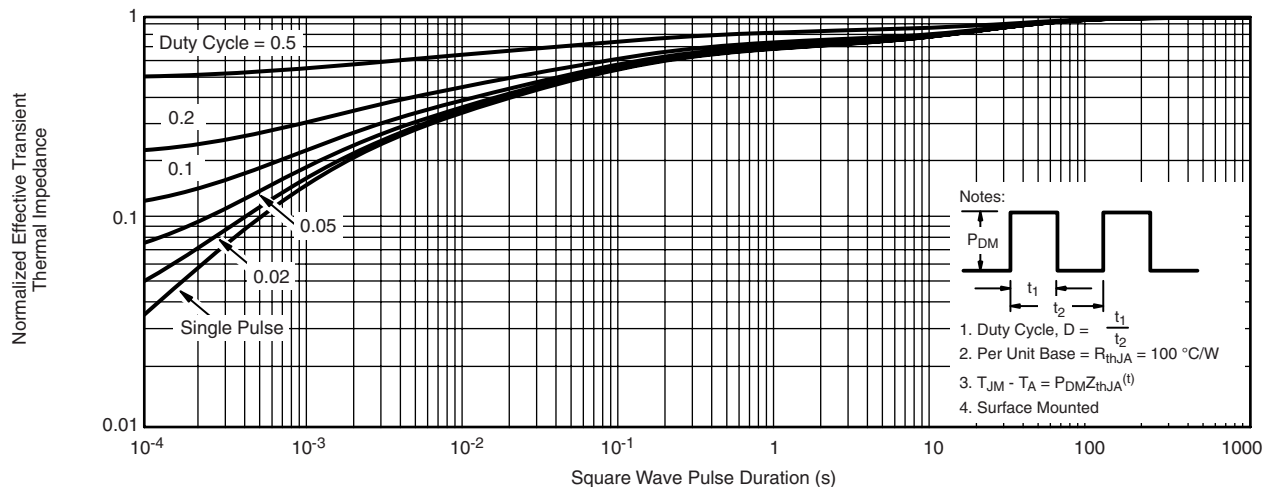
MOSFET TYPICAL CHARACTERISTICS $T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted



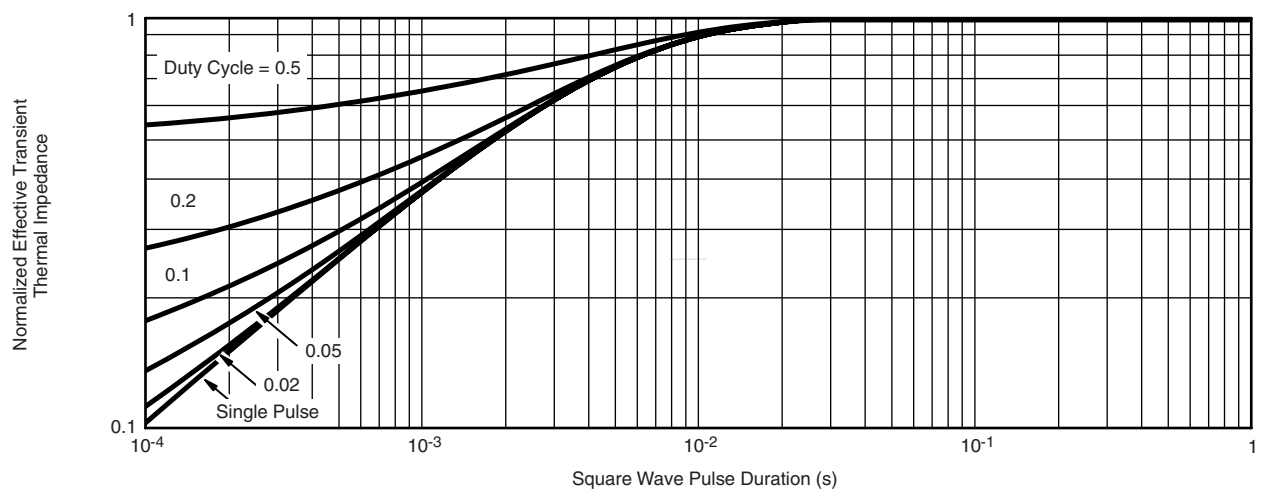
* The power dissipation P_D is based on $T_{J(max)} = 150\text{ }^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



MOSFET TYPICAL CHARACTERISTICS $T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient

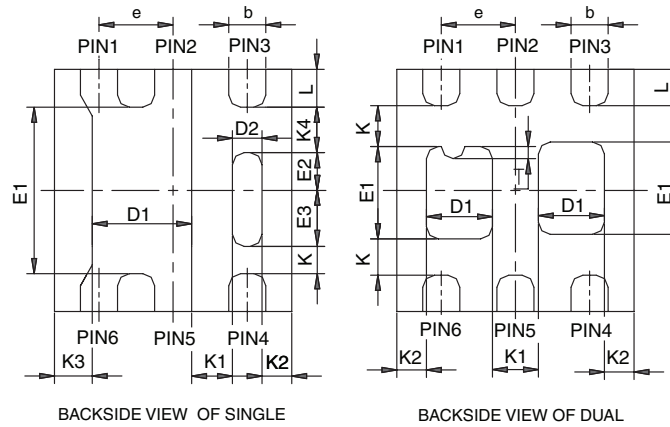


Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?68860.

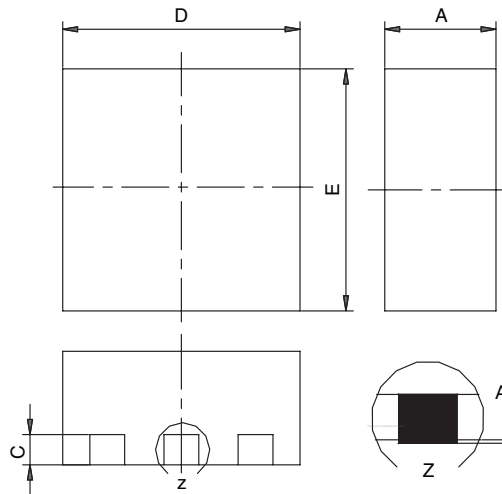


PowerPAK® SC75-6L



BACKSIDE VIEW OF SINGLE

BACKSIDE VIEW OF DUAL



Notes:

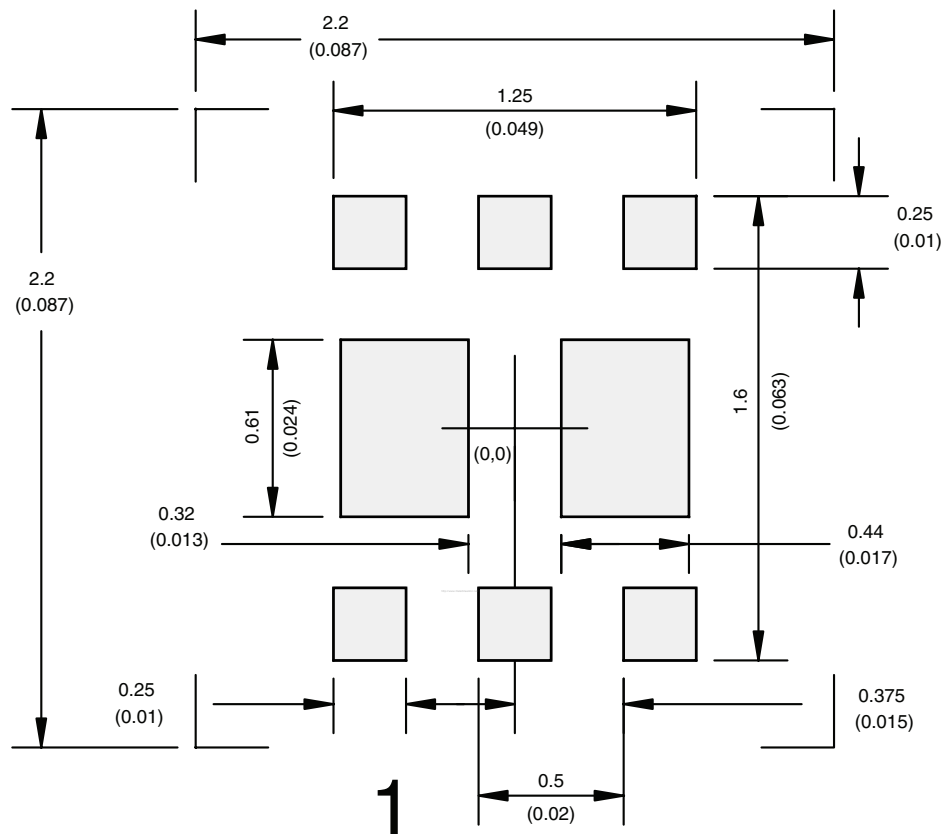
1. All dimensions are in millimeters
2. Package outline exclusive of mold flash and metal burr
3. Package outline inclusive of plating

DETAIL Z

DIM	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.18	0.25	0.33	0.007	0.010	0.013	0.18	0.25	0.33	0.007	0.010	0.013
C	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.53	1.60	1.70	0.060	0.063	0.067	1.53	1.60	1.70	0.060	0.063	0.067
D1	0.57	0.67	0.77	0.022	0.026	0.030	0.34	0.44	0.54	0.013	0.017	0.021
D2	0.10	0.20	0.30	0.004	0.008	0.012						
E	1.53	1.60	1.70	0.060	0.063	0.067	1.53	1.60	1.70	0.060	0.063	0.067
E1	1.00	1.10	1.20	0.039	0.043	0.047	0.51	0.61	0.71	0.020	0.024	0.028
E2	0.20	0.25	0.30	0.008	0.010	0.012						
E3	0.32	0.37	0.42	0.013	0.015	0.017						
e	0.50 BSC			0.020 BSC			0.50 BSC			0.020 BSC		
K	0.180 TYP			0.007 TYP			0.245 TYP			0.010 TYP		
K1	0.275 TYP			0.011 TYP			0.320 TYP			0.013 TYP		
K2	0.200 TYP			0.008 TYP			0.200 BSC			0.008 TYP		
K3	0.255 TYP			0.010 TYP								
K4	0.300 TYP			0.012 TYP								
L	0.15	0.25	0.35	0.006	0.010	0.014	0.15	0.25	0.35	0.006	0.010	0.014
T							0.03	0.08	0.13	0.001	0.003	0.005

ECN: C-07431 – Rev. C, 06-Aug-07
DWG: 5935

RECOMMENDED PAD LAYOUT FOR PowerPAK® SC75-6L Dual



Dimensions in mm/(Inches)

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