SIEMENS

MULTIBANK DRAMS (MDRAMS)

HYB 39M93200 288k x 32 MDRAM
HYB 39M83200 256k x 32 MDRAM

Advanced Information

- **Ultra-High Performance**
  666 MByte/sec single device transfer rate
  36 ns RAS access
  12 ns CAS access
  6 ns burst cycle
- **Multibank Architecture**
  RAS and precharge may overlap CAS READ or WRITE to different banks effectively hiding RAS / precharge time.
- **Ideal Organization for Embedded Applications**

Type	Organisation	MBytes	No. Banks	Speed Grades [MHz]	Package
HYB 39M93200Q	288k x 32	1.15	36	166 / 125 /100	P-QFP-128
HYB 39M93200L	288k x 32	1.15	36	166 / 125 /100	P-LCC-68
HYB 39M83200Q	256k x 32	1.0	32	166 / 125 /100	P-QFP-128
HYB 39M83200L	256k x 32	1.0	32	166 / 125 /100	P-LCC68

- **Variable Length Burst**
  Supports 4 to 128 byte interruptable bursts
- **Byte-level Write Control**
- **Low Internal and Interface Power.**
- **Small Footprint**
  Single package: 14 mm x 20 mm PQFP or 68 pin P-LCC.
- **Compact, Easily Implemented Interface**
  26 signal, bus interface employs standard CMOS/LVCMOS/LVTTL signaling.
- **3.3 V Power Supply and Interface.**

Description

The MoSys Multibank DRAM (MDRAM) is an extended performance synchronous DRAM optimized for ultra-high performance applications where high bandwidth, extremely short access latency and low cost are required. MDRAMs feature fully synchronous I/O at frequencies up to 166 MHz providing 666 MBytes per second of peak bandwidth.

An MDRAM can be viewed as an array of many independent 256 Kbit (32 KByte) DRAMs, - each with a 32-bit interface - connected to a common bus internal to the MDRAM. The external interface is simply a buffered version of the internal bus, seen through a bus repeater. The small bank size and the simplicity of the repeater yield extremely short CAS access latency. The independence of bank facilitates overlapping, or hiding the RAS access and precharge penalty so that average access times will approach the CAS access time.

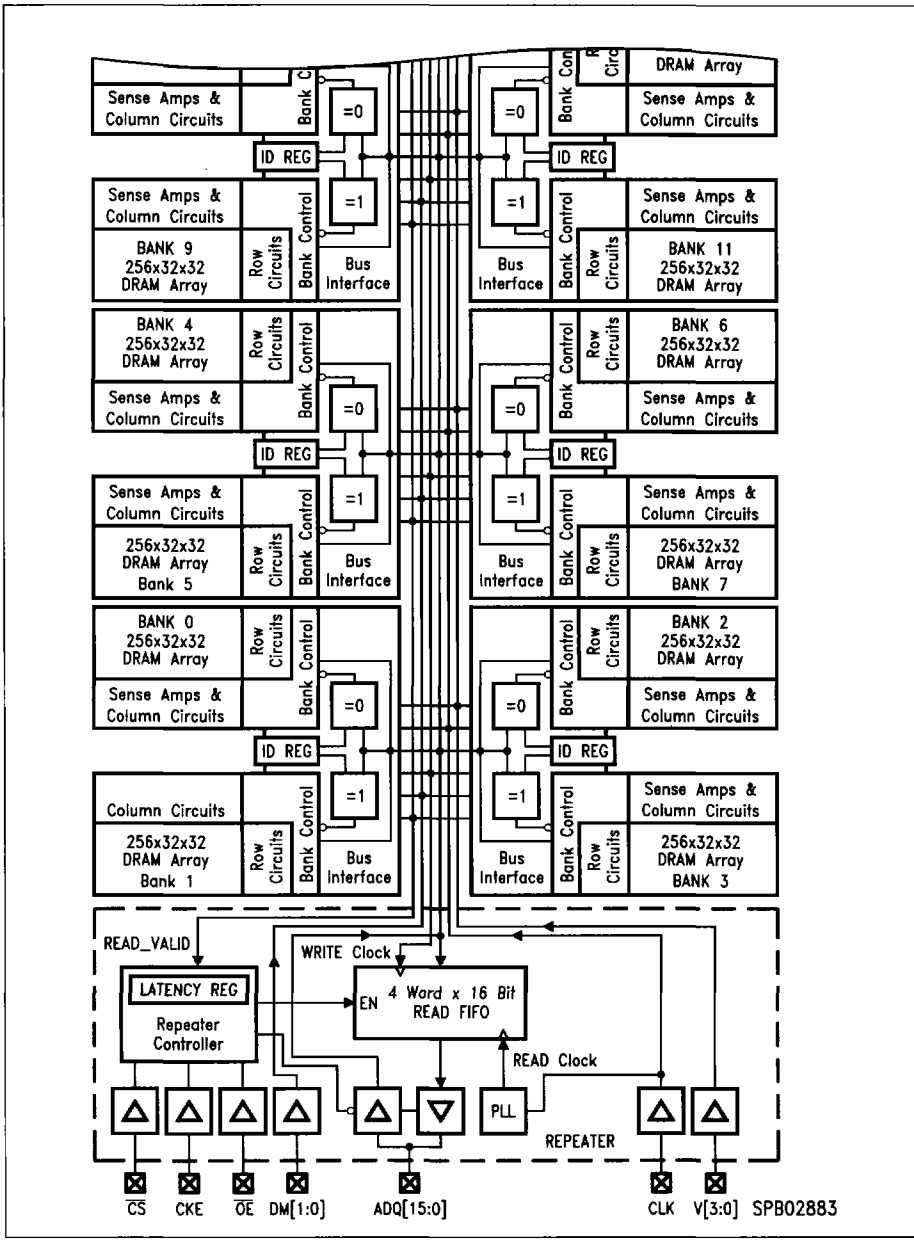


Figure 1
MDRAM Block Diagram

MDRAM Organization

Figure 1 illustrates the internal structure of the MDRAM. The memory is composed of independent and fully functional 32 KByte DRAM banks. The control of each bank is local to each bank rather than centralized.

Address recognition is normally accomplished within the bank so that no external address decoding is required. Programmable bank ID registers are used to map banks to a logical address space. Multiple devices may be cascaded to form larger memory arrays by programming each bank ID register with a unique address. Up to 8 MBytes of memory may be accumulated on a single bus without external address decoding.

Banks are organized in 256 rows by 32 words. Each word is 32 bits wide. All banks are tied to a common internal bus that terminates on a single bus repeater unit at one end of the chip.

Both the internal and external bus consist primarily of a multiplexed address and data bus, a command bus and clock. During data transfer, both clock edges are used for synchronous transfer of 32 bits per clockcycle on only 16 pins. Data mask (DM) facilitate byte level write masking.

The bus repeater buffers the internal bus from the external bus. The repeater also contains a phase lock loop (PLL) and a four 1/2 word deep FIFO with programmable latency that guarantees accurate I/O timing.

MDRAM Operation

A RAS operation (typically called ACTIVATE in SDRAM devices) copies a single row of a single bank into its sense amps. Successive RAS/ACTIVATE commands can activate a single bank or multiple banks.

CAS operations (READ or WRITE) proceed with any activated bank with short latency and high bandwidth. READ or WRITE operations continue in a burst, at ascending column addresses, until terminated by a STOP command. Reading or writing past the end of a row (column address 0x1fH) will wrap to the beginning of the row.

A bank is deactivated by the PRECHARGE command. PRECHARGE writes the contents of the sense amps into the memory array - deactivating the bank. Unlike DRAMs, PRECHARGE is optional when changing banks. READ/WRITE operations may proceed at any activated bank. PRECHARGE may be delayed until another row in an already active bank is to be accessed.

Memory is addressed to the 32-bit word. DM bits facilitate byte-level write masking. Banks have a preprogrammed address at power-on which may be overwritten by a command. Each bank can be treated as a single, independent memory module. Large memory arrays are implemented by programming each bank of a multichip memory to a unique address.

Signal Description

All MDRAM devices share identical packages and pinout. There are 26 active signal pins and 12 power/ground pins. All high speed signals are arranged on one side of the package, in order to equalize and reduce PC board trace length, routing capacitance and inductance.

ADQ[15:0], (In/Out), Address/Data Bus:

These bidirectional pins carry multiplexed address and data. During the cmmand phase of an operation, the ADQ bus carries address information to the MDRAM. The address is sampled on the rising edge of clock.

During the data phase of READ or WRITE the ADQ bus carries 32-bit data words. Data is transferred synchronously, 16 bits at a time, on the rising and falling edge of the clock.

Table 1. Pin Grouping

Datapath		
ADQ[15:0]	16	Multiplexed Address/Data
DM[1:0]	2	Write Data Mask
Command		
CRE or V3	1	Control Register Enable
RAS# or V2	1	Row Address Strobe
CAS# or V1	1	Column Address Strobe
WE or V0	1	Write Enable
Control		
CLK	1	Clock Input
CKE	1	Clock Enable
OE#	1	Output Enable
CS1#	1	Chip Select 1
CS2#	1	Chip Select 2

Total Signals: 26

DM[1:0], (In) Data, Mask:

These signals are used for data masking during the write operation. They are sampled on the rising and falling edge of the clock. A high on a DM bit prevents the corresponding byte from being written. If data masking is required, all DM signals must be high during the rising and falling edges of the WRITE command phase. If write masking is not required, the DM signals should be tied permanently low.

CRE, RAS#, CAS#, WE, (In), Command Bus:

These signals collectively named as V[3:0], form the command bus. They are sampled on the rising edge of the clock. The names V[3:0]and the conventional names (CRE, RAS#, CAS# and WE) are used interchangeably in this data-sheet.

CLK, (In), Memory Clock:

All signals except OE# and CS# are synchronously sampled by this clock.

OE#, (In), Output Enable:

This asynchronous control signal can be used to turn around the data bus in system operating at relatively low frequencies but requiring short access latency. For most applications OE# should be tied permanently low.

CKE, (In), Clock Enable:

This control signal enables the memory clock. CKE is sampled on the rising edge of CLK and is effective on the next rising edge. CKE can be used to freeze the data that is clocked out on the falling edge on the memory clock. For most applications CKE should be permanently tied high.

CS1#, (In), Chip Select 1:

This asynchronous control signal enables or disables the MDRAM. It is useful for memory initialization, power management, and for address decoding of arrays larger than 8 MBytes.

CS2#, (In), Chip Select 2:

This signal is reserved for larger memories with two die in the same package.

VDD/GND (Power):

Memory core power supply.

IOVDD/IOGND (Power):

I/O driver power supply.

SH, (Passive), Short:

These are No-Connect (NC) pins shorted together.

ICS, IC Substrate:

These pins are connected to the chip substrate and should remain unconnected.

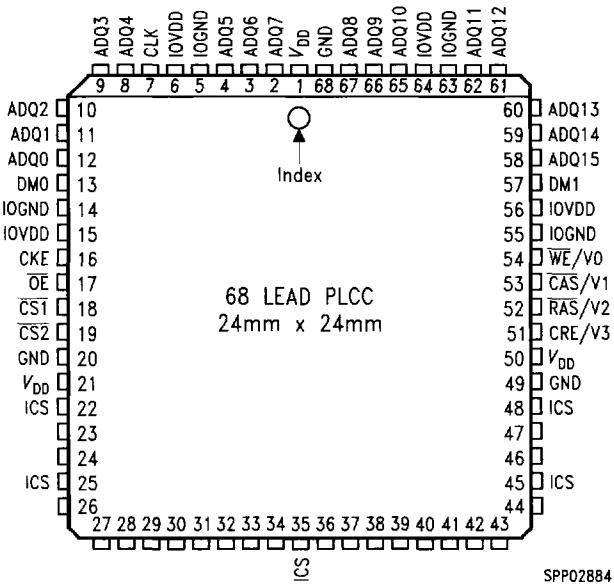


Figure 2
68-Lead PLCC Pinout

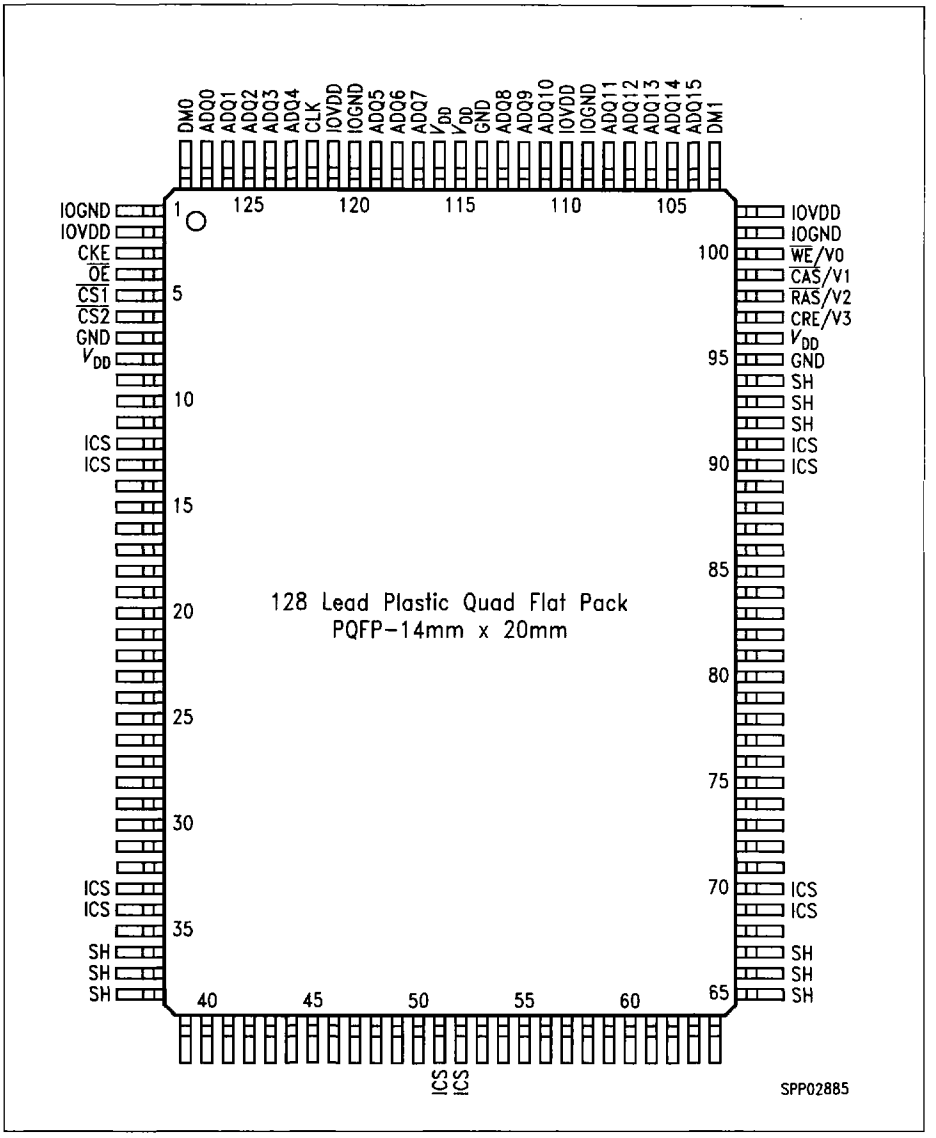


Figure 3
128-Lead PLCC Pinout

Table 2. MDRAM Commands

Operation	CREV3	RAS#V2	CAS#V1	WEV0	X= DONT'CARE Physical Pins: ADQ [15:0] ADQ[15]..... .....ADQ[0]	DM	CLK	CKE	OE#	CS#	

Single Cycle Commands

ACTIVATE(2h)	L	L	H	L	Bank Address	Row Address	X	È	H	X	L	
PRECHARGE(3h)	L	L	H	H	Bank Address	X X X X X X X X	X	È	H	X	L	
STOP&PRE(3h)	L	L	H	H	X X X X X X X X	X X X X X X X X	X	È	H	X	L	1
MODEREGWR(7h)	L	H	H	H	X X X X P Latency	L L L L L L L L	X	È	H	X	L	
STOP(Fh)	H	H	H	H	X X X X X X X X	X X X X X X X X	X	È	H	X	L	

WRITE Command Sequence

WRITE(5h)	L	H	L	H	Bank Address	X X X	Column Address	H	È	H	X	L	2
WRITE(5h)	L	H	L	H	D15----------D0			H L	È	H	X	L	3
WRITE(5h)	L	H	L	H	D31----------D16			H L	.	H	X	L	3

READ Command Sequence

READ(4h)	L	H	L	L	Bank Address	X X X	Column Address	X	È	H	X	L	
READ(4h)	L	H	L	L	Hi Impedance/Turn Around			X	È.	H	L	L	4, 5
READ(4h)	L	H	L	L	D15----------D0			X	È.	H	L	L	5
READ(4h)	L	H	L	L	D31----------D16			X	È.	H	L	L	5

ID Register Write Command Sequence

IDREGWR(Dh)	H	H	L	H	Bank ID	X X X X X X X X	X	È	H	X	L	
STOP(Fh)	H	H	H	H	New Bank ID	X X X X X X X X	X	È	H	X	L	
STOP(Fh)	H	H	H	H	X X X X X X X X	X X X X X X X X	X	.	H	X	L	

Memory Reset Command Sequence

MEMRESET(6h)	L	H	H	L	X X X X X X X X	X X X X X X X X	H	H	X	È	H	X	L
STOP(Fh)	H	H	H	H	X X X X X X X X	X X X X X X X X	X	È	H	X	L	
STOP(Fh)	H	H	H	H	X X X X X X X X	X X X X X X X X	X	È	H	X	L	

Powerdown / Memory Disable

xxxx (xH)	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H	

Notes

1) PRECHARGE interrupting a READ is equivalent to STOP followed by PRECHARGE (STOP&PRE) and affects the bank being read. Any address forced on ADQ bus is ignored.

2) If data masking is required all DM signals must be high during the rising and falling edges of the WRITE command phase. If write masking is not required the DM signals should be tied permanently low.

3) DM[1:0] set mask corresponding data byte. For example, DM[1] high masks D[15:8] on rising clock edges and D[31:24] on falling clock edges.

4) The READ command phase is followed by a specified number of one-half-clock-period Latency phases.

5) Latency Value controls which half-word is latched on rising edge of CLK. The first data half-word latches on rising edges when Latency is even.

Command Description

Ten MDRAM commands are listed on Table 2. The remaining commands are reserved and should never be used. All except four commands are single cycle long. A legal command must be present on the command bus on every clock cycle. A "clock cycle" is from clock rising edge to clock rising edge. All commands are sampled on the rising edge of the clock. All operations begin with a "command/address" phase that is one clock cycle in length.

MEMRESET [ ], (3 Cycles):

Initializes the mode register and ID register to power up defaults and deactivates (precharges) all banks.

- MEMRESET is not data-safe. Data may be lost if all banks are not already precharged.

ACTIVATE [Bank, Row], (1 Cycle):

ACTIVATE is similar to RAS in standard DRAM. It loads the contents of the selected row to the sense amplifier latches of that bank. Subsequent READs or WRITEs to the activated bank operate on the sense amplifier latches. Before another row in the same memory bank can be selected, a PRECHARGE or GRPPRE command must be used to store the data from the sense amplifiers back to the memory cells.

The ACTIVATE command must not be used:

- When T_{RP} timing is violated.
- When the selected bank is already activated.
- Within a READ, WRITE, or IDWRITE operations.

PRECHARGE [Bank], (1 Cycle):

PRECHARGE copies the sense amp contents to the memory cells of the addressed bank and prepares the bank for the next ACTIVATE/RAS operation. A bank may be precharged even if it is in the deactivated or precharged state.

During READ operations, this command terminates the current operation and executes a precharge to the bank currently in a read state (STOP&PRE). WRITEs must be terminated with a STOP. If PRECHARGE is used to terminate a READ, then T_{RP} is measured from the falling edge of the PRECHARGE command cycle to the rising edge of the ACTIVATE command cycle.

The precharge command can be used at any time except:

- To terminate a WRITE
- When it violates T_{RAS} (ACTIVATE to PRECHARGE delay).

READ [Bank, Column], (Multicycle):

READ is siminar to CAS read in standard DRAM. READ transfers data from the sense amps addressed by the column address, to the output. A READ command is followed by a specified nummer of one-half-clock-period latency phases and even number data phases. The number of latency phases is programmable and may be even or odd (see Memory Initialization).

After the column access latency, each succeeding clock edge transfers data from ascending column addresses in a burst. A 16-bit value is read each data phase. The READ command must be maintained on the command bus for the duration of the operation. READ terminates with STOP or PRECHARGE. The MDRAM will terminate a READ and will not send data on the ADQ bus if a STOP command is issued immediately after the READ command phase.

READs past the end of a row (column address 0x1FH) will "wrap" to the beginning of the row.

The READ command can be used:

- Only on activated banks.
- At any time except when T_{RCD} is violated.

WRITE [Bank, Column], (Multicycle):

WRITE transfers data from the ADQ bus to the selected bank and column address. WRITE employs burst transfers. After the one cycle command/address phase, each succeeding clock edge writes to ascending column addresses. A WRITE command phase must always be followed by an even number of data phases of one half-clock period in length. A 16-bit value is written each data phase.

The WRITE command must be maintained on the command bus for the duration of the command phase and data phases. WRITE terminates only with a STOP command. WRITE must be followed by at least two data phases (one 32-bit word) before it can be terminated with a STOP command.

At clock frequencies above 125 MHz, a READ following a WRITE to the same bank or the bank that shares the same upper seven address bits must have two STOP commands between the last data phase of WRITE and the command phase of READ. WRITEs past the end of a row (column address 0x1FH) will "wrap" to the beginning of the row. The latency setting does not effect WRITE.

The WRITE command can be used:

- At any time except when T_{RCD} is violated.

STOP [ ], (1 Cycle):

STOP terminates the current READ/WRITE operation and sets the memory to the idle state without invoking PRECHARGE. Additional READ or WRITE commands to the same bank and row, or to other active banks, can proceed without new ACTIVE commands. Repeated STOP commands are equivalent to no-operation (NOP) and hold the memory in an idle state.

The stop command can be used at any time except:

- Immediately after the WRITE command (before any WRITE data Phases).

GRPACTIV [Banks], (1 Cycle):

Group Activate is similar to ACTIVATE except that the four banks sharing the six MSB of bank address are activated simultaneously. This command can be used to accelerate memory refresh, or to activate multiple banks for READ/WRITE operations.

GRPACTIV command is permitted:

- Whenever ACTIVATE is permitted except when T_{GAP} is violated.

GRPPRE [Banks], (1 Cycle):

Group Precharge precharges four banks. It can be used to accelerate memory refresh or deactivate multiple banks.

GRPPRE command is permitted:

- Whenever PRECHARGE is permitted except when TGAP is violated.

MODEREGWR [Mode Bits], (1 Cycle):

Mode Register Write initializes the mode register.

IDREGWR [Old ID, New ID], (2 Cycle):

ID Register Write loads the bank ID register with a new value. This command is used to map memory banks to logical address space.

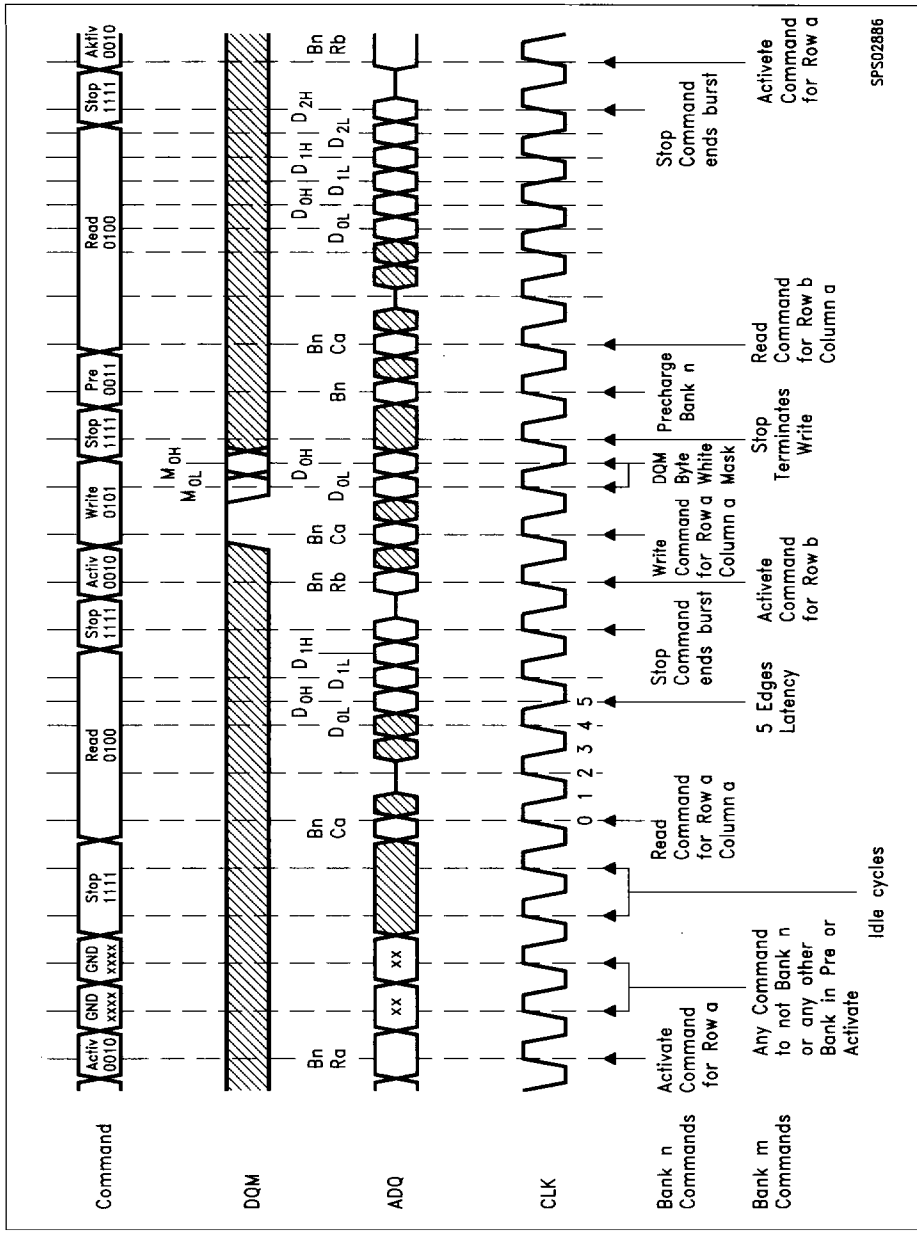


Figure 4
Command Sequence Example

Memory Initialization

On power up the memory must be initialized with a MEMRESET and MODEREGWR commands.

Mode Register

The mode register definition is shown in Table 3. On power up, the eight LSBs and PD bit are reset to zero. The latency Value after power up is undefined. The PD and Latency fields must be initialized by MODEREGWR. PD = "0" is the normal, powered up state. PD = "1" places the memory in power down state by turning off the Phase-Locked-Loop.

Table 3. Mode Register Definition

M[15:12]	M[11]	M[10:8]	M[7:0]
Ignored	PD	LATENCY VALUE	Reserved Must be 0

MDRAM delivers data on both rising and falling edges of the clock. The latency value can be used to relocate the first 16-bit word a data burst on a rising or a falling edge of the clock as desired. Figure 5 shows an example at 125MHz with latency value set to 010. Legal latency settings for each device speed grade versus frequency are given in the AC timing parameter section (Table 11).

Table 4. Latency Value

M10	M9	M8	T_{CAC} in clock edges
0	0	0	3
0	0	1	4
0	1	0	5
0	1	1	6
1	0	0	7
1	0	1	8
1	1	0	9
1	1	1	10

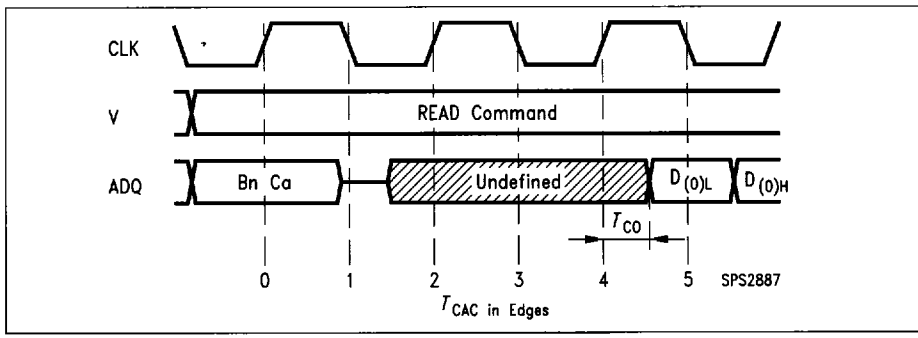


Figure 5
READ with Latency Set to 010

ID Registers

The contents of bank ID registers map each bank to logical address space. On power up, the bank ID registers are preset sequentially starting from bank zero. When multiple devices are tied on the same bus, the bank ID registers of all devices must be initialized in order to remap all memory banks to nonoverlapping space.

The contents of the ID registers are changed with the IDREGWR command. To prevent IDREGWR command from effecting all the devices on the bus, the Chip Select signals (CS1#, CS2#) can be used to enable only one chip at a time. The bank ID register contents are volatile. The default value will be restored each time power is applied or when the MEMRESET command is executed. Note that the ID register contains 7 bits that correspond to the 7 MSB of two banks, meaning that two banks are programmed at a time and share the same 7 MSB of their ID.

Memory Refresh

Memory Refresh is accomplished with an ACTIVATE and PRECHARGE (RAS and precharge) operations to every row of every bank every TREF period. "Group" commands GRPACTIV and GRPPRE can be used to reduce the number of refresh operations by four. The group commands affect four banks simultaneously. The four banks sharing the six MSBs of bank address are activated or precharged.

Table 5. Absolute Maximum Ratings

Parameter	Value
Voltage on V_{DD} pin relative to GND	– 1.0 V to 4.6 V
Voltage on I/O pin relative to GND (During normal operation)	– 1.0 V to 4.6 V
Voltage on input pin relative to GND (No V_{DD} applied)	– 1.0 V to 4.6 V
Short-circuit output current, I_{OS}	20 mA
Operating Temperature, T_{OPR}	0 to + 70 °C
Storage Temperature, T_{STG}	– 55 °C to +125 °C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under Recommended Operating Conditions, DC Current Requirements and AC Characteristics.

Table 6. Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Units	Notes
Supply Voltage	VDD	3.14	3.3	3.47	V	1
Input Voltage High	VIH	0.5x(VDD+1)		Vdd	V	2
Input Voltage Low	VIL	0		0.5x(VDD – 1)	V	
Ambient Temperature	TA	0		70	°C	

Note 1: Functionality is guaranteed between VDDmin = 3.0 V and VDDmax = 3.6 V

Note 2: Output load is 110 ohms to Vdd/2

Table 7. Capacitance T_A = 25 °C, f = 1 MHz, Typical Values in pF

Pin Group	128PQFP	68PLCC
ADQ I/O Pin Capacitance	2.6	5
DM Input Pin Capacitance	1.6	3
Clock Input Capacitance	1.8	3.8
Input Capacitance (all other)	1.8	3.8

Table 8. DC Current Requirements

Parameter	Symbol	Typical	Units	Test Conditions
Operating Current	ICC	195	mA	Burst Length =128 Bytes, tRAS = tRAS(min), tRP = (min), Io = 0mA, 50%read, 50%write,125 MHz. IDD = 40 + (1.2)fCLK mA, fCLK in MHz.
Suspend Current	IDDSUS	20	mA	CKE < VIL, TCLK = TCLK (min), All other inputs grounded.
Inactive Standby Refresh Current	IDDDSLEEP	5	mA	Same as above except between refresh periods: CKE < V_{IL}, PD = "0"
Inactive Standby Current	IDDPD	1	mA	CS# > VIH, PD = "0"

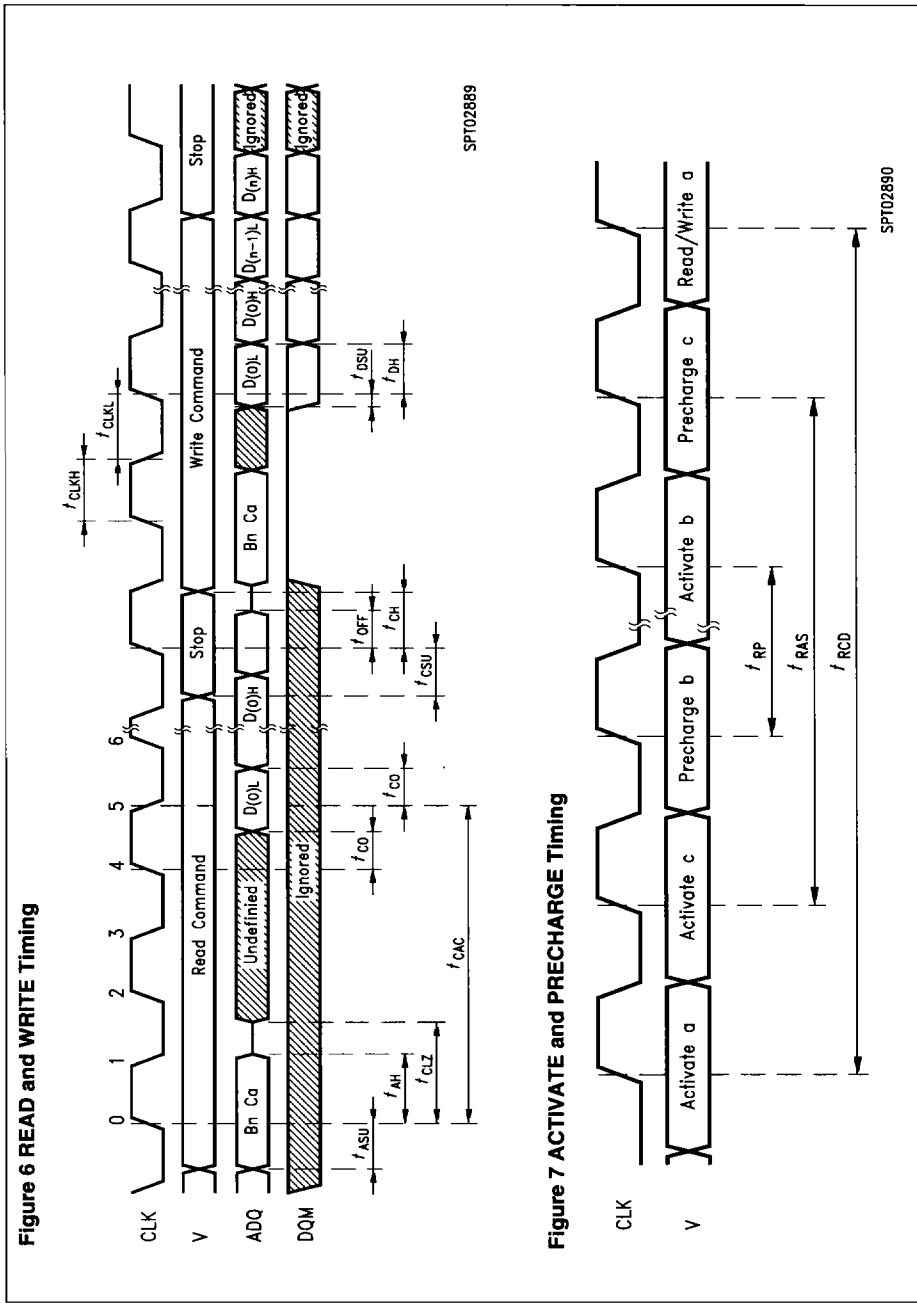
Table 9. AC Characteristics

at Recommended Operating Condition

Speed Grade		-166		-125		-100			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes:**
READ to data valid	T_{CAC}		12		18		24	ns	5,6
ACTIVATE to READ/WRITE delay	T_{RCD}		18		24		30	ns	1,6
ACTIVATE to PRECHARGE delay	T_{RAS}		30		40		40	ns	1,6
PRECHARGE to ACTIVATE delay	T_{RP}		18		24		30	ns	1,6
Group command to group command delay	T_{GAP}		24		32		40	ns	7
Burst mode READ/WRITE cycle	T_{PC}	6		8		10		ns	
CLK frequency	f_{CLK}		166		125		100	MHz	
CLK duty cycle		-10	+10	-10	+10	-10	+10	%	-2
CLK high level width	T_{CLKH}	2.7	3.3	3.6	4.4	4.5	5.5	ns	2
CLK low level width	T_{CLKL}	2.7	3.3	3.6	4.4	4.5	5.5	ns	2
Command setup time	T_{CSU}	2		2		4		ns	3
Command hold time	T_{CH}	1.5		1.5		2.5		ns	3
CKE setup time	T_{ESU}	2		2.5		3		ns	
CKE hold time	T_{EH}	0		1.5		2		ns	
Address setup time	T_{ASU}	2		2		4		ns	
Address hold time	T_{AH}	1		1.5		2		ns	
Data setup time	T_{DSU}	1		1.5		2		ns	
Data hold time	T_{DH}	1.5		1.5		2		ns	
Data Mask setup time	T_{DMSU}	1		1		2		ns	
Data Mask hold time	T_{DMH}	1.5		2		2		ns	
Refresh period	T_{REF}		16		16		16	ms	
Clock to data output	T_{CO}	1	2.5	1	2.5	1	3.5	ns	8
READ Command to ADQ Lo-Z	T_{CLZ}	4		5		5		ns	
Burst STOP/PRE to ADQ Hi-Z	T_{OFF}		4		5.5		6.5	ns	
OE high to ADQ Hi-Z	T_{OEHZ}		3		4		4	ns	
OE low to ADQ Lo-Z	T_{OELZ}		3		4		4	ns	
Chip select high to clock	T_{CSD}		2		3		4	ns	
Chip select low to clock	T_{CSA}	4		4		4		ns	
Chip select high to ADQ Hi-Z	T_{CSO}		2		3		4	ns	
Minimum PLL lock frequency	F_{LOCK}	50		50		50		MHz	
Power-up/power-on time	T_{PU}		10		10		10	µs	4
ACTIVATE to READ/WRITE delay	T_{RCD}	3		3		3		Cycles	1,2
ACTIVATE to PRECHARGE delay	T_{RAS}	5		5		4		Cycles	1,2
PRECHARGE to ACTIVATE delay	T_{RP}	3		3		3		Cycles	1,2

Notes:

1) To same bank.
2) Fclk = max.
3) "Command bus" is CRE, RAS#, CAS# and WE.
4) Power on or PD = "1" -> "0", delay to full function.
5) To any activated bank.
6) Characterized but not tested.
7) Separation between group commands (GRPACTIVE orGRPPRE) addressed to the same chip.
8) Tested with 1/2 of ADQ pins switching to VDD and the other 1/2 switching to GND. Load is 25 pF to GND and 110 ohm to Vdd/2.


CLK
V
ADQ
DQM
Read Command
Write Command
Stop
Bn Ca
Undefinied
Ignored
D(0)L
D(0)H
D(n-1)L
D(n)H
tCLKH
tCLKL
tASU
tAH
tCLZ
tCAC
tCO
tOFF
tCH
tCSU
tDSU
tDH
SPT02889
Figure 6 READ and WRITE Timing
Activate a
Activate c
Precharge b
Activate b
Precharge c
Read/Write a
tRP
tRAS
tRCD
SPT02890
Figure 7 ACTIVATE and PRECHARGE Timing

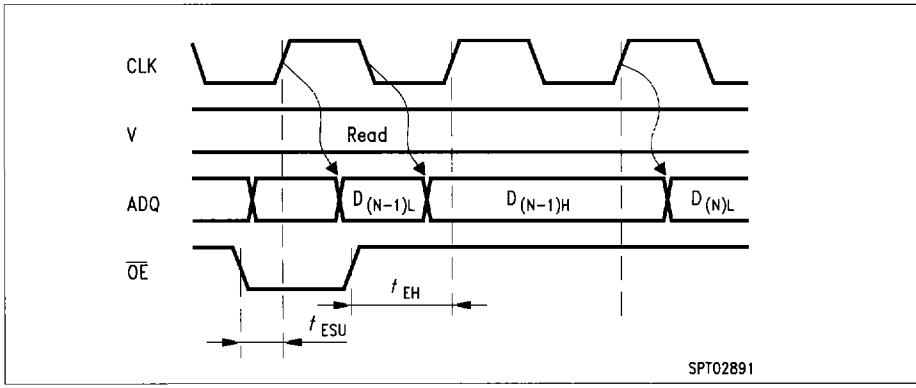


Figure 8
Clock Enable Timing

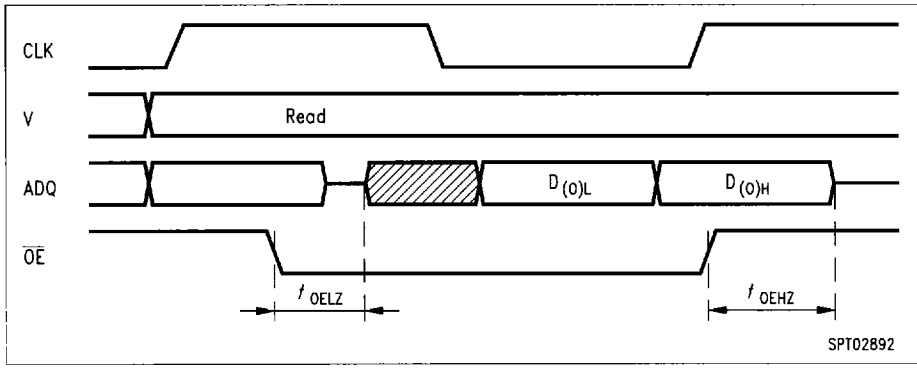


Figure 9
Output Enable Timing

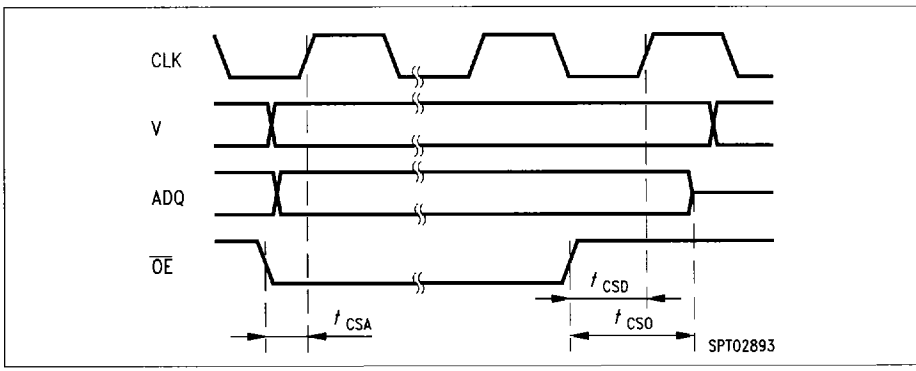


Figure 10
Chip Select Timing

Table 10. Legal Latency Values

Speed Grade	-166		-125		-100		
Latency Value	Frequency Range						
	Min	Max	Min	Max	Min	Max	Units
000 001	50	100	50	100	50	80	MHz
001 010	100	135	90	125	70	100	MHz
010	100	166					MHz
010 011	145	166					MHz

Note: *The latency value must be selected based on frequency of operation and whether the first read data is to be latched on the falling (,) or rising (È) edge of the clock. For example: The MDRAM operation at 123 MHz with the first read data latched on the falling edge of the clock, must have the latency set to (010).*

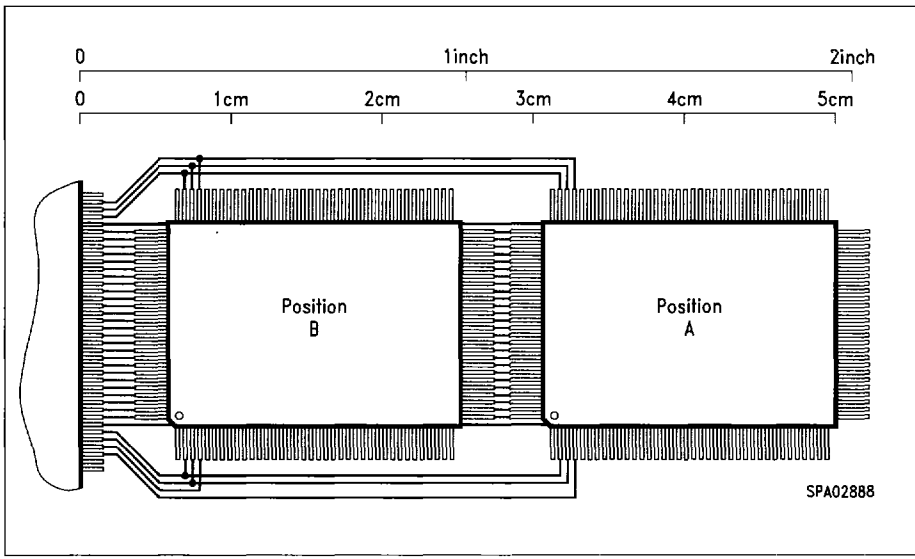
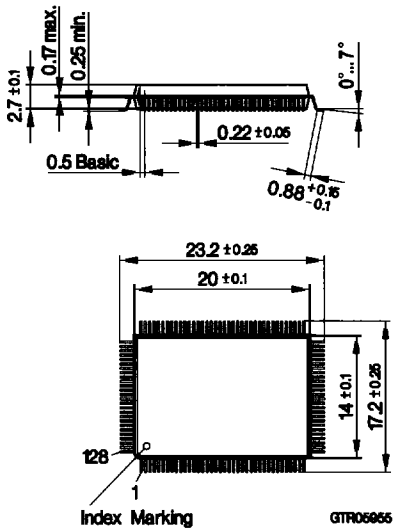


Figure 11
Board Layout Example

Package Outlines

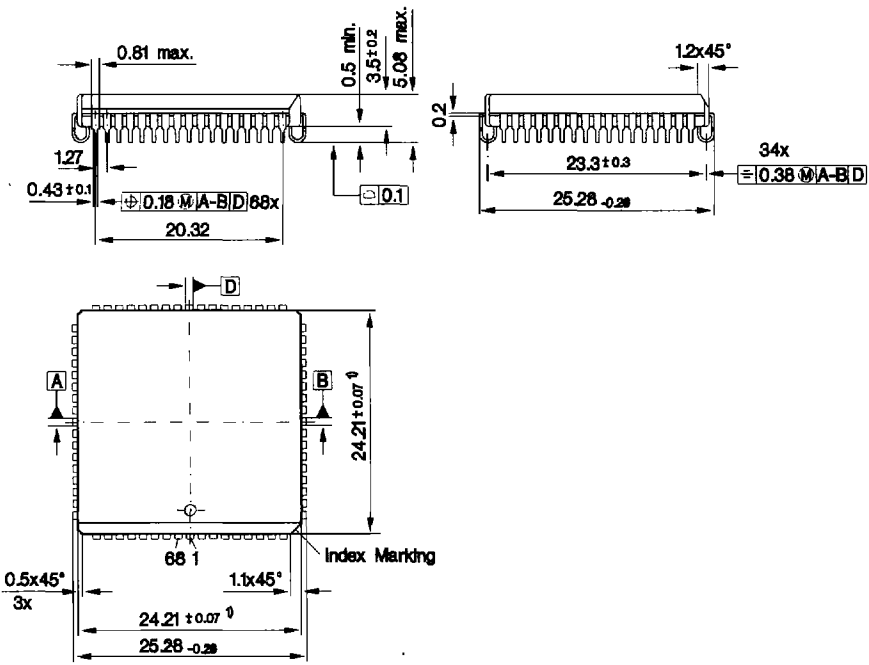
Plastic Package P-QFP 128
(Ceramic/Plastic Quad Flat Package)



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".
SMD = Surface Mounted Device

Dimensions in mm

Plastic Package P-LCC-68
(Plastic Leaded Chip Carrier)



1) Does not include plastic or metal protrusion of 0.15 max. per side

GPL05099

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".
SMD = Surface Mounted Device

Dimensions in mm