LZ93 Series CMOS Gate Array

■ Description

The LZ93 series CMOS gate array provides 300 to 5000 gates of line up with high speed and low power consumption.

It is fabricated using 1.6 μm CMOS silicon gate/ double metal technology.

■ Features

1. CMOS process
2. Number of gates : 300, 600, 1000, 1100, 1600, 2200, 3000, 4000, 5000
3. Internal gate delay : 1.7ns/gate
4. Macro cell : 95 cells
   74LS cell : 126 cells
5. I/O level : CMOS/TTL compatible
6. Supply voltage : 5V±5% (TTL interface)
   5V±10% (CMOS interface)

■ Line Up

Parameter		LZ93300	LZ93600	LZ931000	LZ931100	LZ931600	LZ932200	LZ933000	LZ934000	LZ935000
Gate count (2 input NAND conversion)		300	600	1010	1111	1596	2240	3145	4009	5000
I/O buffer count		37	51	67	77	97	97	112	128	140
Pin count		40	54	70	80	100	100	120	136	150
Process		1.6 μm CMOS silicon gate, double metal								
Delay time	Internal gate	1.7ns/gate (F.O.=3, Wiring length : 2mm)								
	Input buffer	TTL level : 2.4ns/CMOS level : 2.9ns (F.O.=3, Wiring length : 2mm)								
	Output buffer	4.0ns (C_L=20pF)								
I/O level		TTL level/CMOS level								
Supply voltage		5V±5% (TTL interface)/5V±10% (CMOS interface)								

LZ95 Series CMOS Gate Array

■ Description

The LZ95 series CMOS gate array provides 2000 to 10000 gates of line up with 1.2ns/gate of delay time.

It is fabricated using the latest 1.2 μm CMOS silicon gate, double metal technology.

■ Features

1. CMOS process
2. Number of gates : 300, 650, 1170, 2000, 4000, 6000, 8000, and 10000
3. Internal gate delay : 1.2ns/gate
4. Macro cell : 95 cells
   74LS cell : 126 cells
5. I/O level : CMOS/TTL level
6. Supply voltage : 5V ± 5% (TTL interface)
   5V ± 10% (CMOS interface)

■ Line Up

Parameter		LZ95300	LZ95650	LZ951170	LZ952000	LZ954000	LZ956000	LZ958000	LZ9510000
Gate count		315	650	1170	2000	4255	6075	8370	10032
I/O buffer count		46	62	77	97	128	148	176	194
Pin count		48	64	80	100	136	156	184	202
Process		1.2 μm CMOS silicon gate, double metal							
Delay time	Internal gate	1.2ns/gate (F.O. = 3, Wiring length : 2mm)							
	Input buffer	TTL level : 2.4ns/CMOS level : 2.0ns (F.O. = 3, Wiring length : 2mm)							
	Output buffer	TTL level : 4.0ns/CMOS level : 4.2ns (C_L = 20pF)							
I/O level		TTL level/CMOS level							
Supply voltage		5V ± 5% (TTL interface) /5V ± 10% (CMOS interface)							

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	−0.3 to +7	V
Input voltage	V_I	−0.3 to V_{CC} +0.3	V
Output voltage	V_O	−0.3 to V_{CC} +0.3	V
Operating temperature	T_{opr}	−10 to +70	℃
Storage temperature	T_{stg}	−55 to +150	℃

■ Recommended Operating Conditions

Parameter	Symbol	TTL level			CMOS level			Unit
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply voltage	V_{CC}	4.75	5	5.25	4.5	5	5.5	V
Operating temperature	T_{opr}	−10		+70	−10		+70	℃

■ Electrical Characteristics

(Ta = −10 to +70℃, V_{CC} = 5V ± 5% (TTL level), V_{CC} = 5V ± 10% (CMOS level))

Parameter	Symbol	Conditions	TTL level			CMOS level			Unit	Note
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Input "Low" current	V_{IL}				0.8			1.5	V	
Input "High" voltage	V_{IH}		2.0			3.5			V	
Input "High" threshold voltage	V_{T+}	Schmitt input buffer 1			2.2			3.7	V	1
Input "Low" threshold voltage	V_{T-}		0.5			1.0			V	
Hysteresis voltage	V_H		0.2			0.4			V	
Input "High" threshold voltage	V_{T+}	Schmitt input buffer 2						4.3	V	2
Input "Low" threshold voltage	V_{T-}					0.8			V	
Hysteresis voltage	V_H					0.6			V	
Input "High" threshold voltage	V_{T+}	Schmitt input buffer 3						4.5	V	2
Input "Low" threshold voltage	V_{T-}					0.7			V	
Hysteresis voltage	V_H					0.8			V	
Input "High" threshold voltage	V_{T+}	Schmitt input buffer 4						4.7	V	2
Input "Low" threshold voltage	V_{T-}					0.6			V	
Hysteresis voltage	V_H					1.0			V	
Output "Low" voltage	V_{OL}	I_{OL} = 4mA			0.4			0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = −2mA	2.4			4.0			V	
Input leakage current	I_{IL}	V_I = OV to V_{CC}	−10		10	−10		10	μA	
Output leakage current	I_{OZ}	High impedance state	−10		10	−10		10	μA	

Note 1 : Applied to the input buffer cells IBFS and IBFCS for models excepting the LZ931100 and the LZ931600.
Note 2 : Applied to the schmitt trigger input buffer composed of the input buffer transferring the input potential to the interior and internal gates for both LZ93 series and LZ95 series.