OKI semiconductor

MSM511002A

1,048,576-WORD x 1-BIT DYNAMIC RAM

GENERAL DESCRIPTION

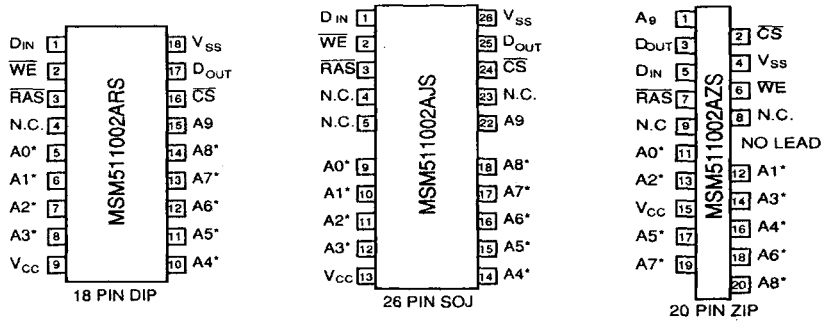
The MSM511002A is a new generation dynamic RAM organized as 1,048,576 words x 1 bit. The technology used to fabricate the MSM511002A is OKI's CMOS silicon gate process technology. The device operates at a single +5V power supply. Its I/O pins are TTL compatible.

FEATURES

- Silicon gate, triple polysilicon CMOS, 1-transistor memory cell
- Single +5V power supply, ±10% tolerance
- Input: TTL compatible, address input, data input latch
- Output: TTL compatible, tristate, nonlatch
- Refresh: 512 cycles/8 ms
- Common I/O capability using Early Write operation
- 1,048,576 words x 1 bit organization
- Static column mode, read/write capability
- $\overline{CS}$ before $\overline{RAS}$ refresh, Hidden refresh, $\overline{RAS}$-only refresh capability
- Built-in V_{BB} generator circuit

Family	Access Time (Max.)	Cycle Time (Min.)	Power Dissipation	
			Operating (Max.)	Standby (Max.)
MSM511002A-70	70ns	140ns	468mW	5.5mW
MSM511002A-80	80ns	160ns	413mW	
MSM511002A-10	100ns	190ns	358mW	

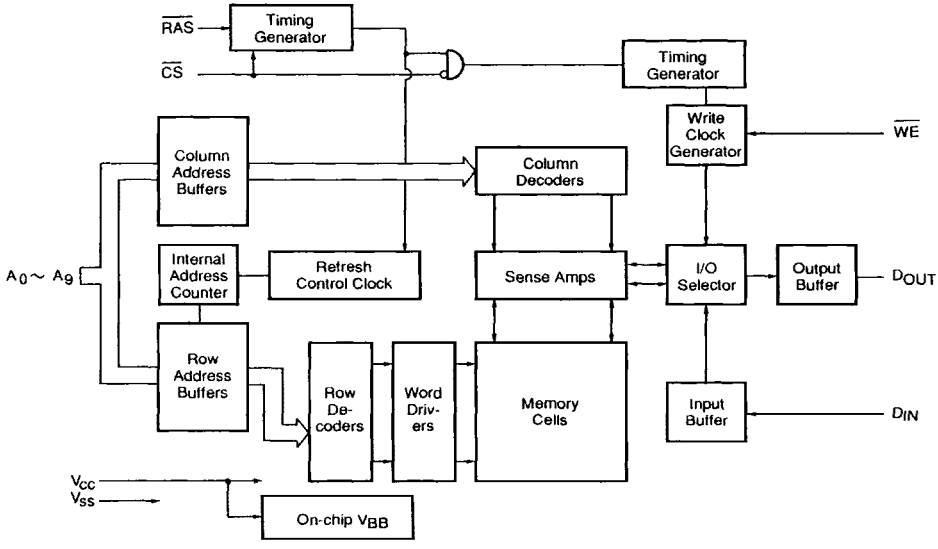
PIN CONFIGURATION (TOP VIEW)



* Refresh Address

Pin Names	Function
A_0 to A_9	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select Input
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{WE}$	Write Enable
Vcc	Power Supply (+5V)
Vss	Ground (0V)
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS
ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Conditions	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	Ta = 25°C	−1.0 to +7.0	V
Short circuit output current	I_{OS}	Ta = 25°C	50	mA
Power dissipation	P_D	Ta = 25°C	1	W
Operating temperature	T_{opr}	–	0 to +70	°C
Storage temperature	T_{stg}	–	−55 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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RECOMMENDED OPERATING CONDITIONS

(Ta = 0 ~ 70°C)

Parameter	Symbol	Conditions	Value			Unit	Operating Temperature
			Min.	Typ.	Max.		
Supply voltage	V_{CC}	–	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	–	0	0	0	V	
Input high voltage	V_{IH}	–	2.4	–	6.5	V	
Input low voltage	V_{IL}	–	−1.0	–	0.8	V	

DC CHARACTERISTICS

(V_{CC} = 5V ± 10%, Ta = 0 to +70°C)

Parameter	Symbol	Conditions		MSM 511002A-70		MSM 511002A-80		MSM 511002A-10		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
Output high voltage	V_{OH}	I_{OH} = -5.0mA		2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	–
Output low voltage	V_{OL}	I_{OL} = 4.2mA		0	0.4	0	0.4	0	0.4	V	–
Input leakage current	I_{LI}	0V ≦ VI ≦ 6.5V; all other pins not under test = 0V		-10	10	-10	10	-10	10	μA	–
Output leakage current	I_{LO}	D_{OUT} disable 0V ≦ VO ≦ 5.5V		-10	10	-10	10	-10	10	μA	–
Average power supply current* (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CS}$ cycling, t_{RC} = min		–	85	–	75	–	65	mA	–
Power supply current* (Standby)	I_{CC2}	$\overline{RAS}$=V_{IH}, $\overline{CS}$=V_{IH}, D_{OUT}=Hz	TTL	–	2	–	2	–	2	mA	–
			MOS	–	1	–	1	–	1		
Average power supply current* ($\overline{RAS}$-only refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CS}$=V_{IH}, t_{RC}=min		–	85	–	75	–	65	mA	–
Average power supply current* ($\overline{CS}$ before $\overline{RAS}$ refresh)	I_{CC6}	$\overline{RAS}$ cycling, $\overline{CS}$ before $\overline{RAS}$		–	85	–	75	–	65	mA	–
Average power supply current* (Static column mode)	I_{CC9}	$\overline{RAS}$=V_{IL}, $\overline{CS}$ cycling t_{SC}=min		–	70	–	60	–	55	mA	–

* I_{CC} depends on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	Value		Unit
			Min.	Max.	
Input capacitance (A_0 to A_9, D_{IN})	C_{IN1}	–	–	6	pF
Input capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{WE}$)	C_{IN2}	–	–	7	pF
Output capacitance (D_{OUT})	C_{OUT}	–	–	7	pF

AC CHARACTERISTICS

(V_{CC} = 5V ± 10%, Ta = 0 to +70°C) Notes 1,2,3

Parameter	Symbol	MSM 511002A-70		MSM 511002A-80		MSM 511002A-10		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Refresh period	t_{REF}	–	8	–	8	–	8	ms	–
Random read or write cycle time	t_{RC}	140	–	160	–	190	–	ns	–
Read/write cycle time	t_{RWC}	165	–	185	–	220	–	ns	–
Static column mode cycle time	t_{SC}	45	–	50	–	55	–	ns	–
Static column mode read/write cycle time	t_{SRWC}	70	–	80	–	100	–	ns	–
Access time from $\overline{RAS}$	t_{RAC}	–	70	–	80	–	100	ns	4,5,6
Access time from $\overline{CS}$	t_{CAC}	–	20	–	20	–	25	ns	4,5
Access time from column address	t_{AA}	–	35	–	40	–	50	ns	4,6,7
Access time from last write	t_{ALW}	–	65	–	75	–	95	ns	4,7
Output low impedance time from $\overline{CS}$	t_{CLZ}	0	–	0	–	0	–	ns	4
Data output hold time reference to column address	t_{AOH}	5	–	5	–	5	–	ns	–
Data output enable time reference to $\overline{WE}$	t_{OW}	–	30	–	30	–	30	ns	–
Output buffer turn-off delay time	t_{OFF}	0	20	0	20	0	20	ns	–
Transition time	t_T	3	50	3	50	3	50	ns	3
$\overline{RAS}$ precharge time	t_{RP}	60	–	70	–	80	–	ns	–
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	–
$\overline{RAS}$ pulse width (Static column mode)	t_{RASC}	70	100,000	80	100,000	100	100,000	ns	–
$\overline{RAS}$ hold time	t_{RSH}	20	–	20	–	25	–	ns	–
$\overline{CS}$ precharge time	t_{CP}	10	–	10	–	10	–	ns	–
$\overline{CS}$ pulse width	t_{CS}	20	10,000	20	10,000	25	10,000	ns	–
$\overline{CS}$ pulse width (Static column mode)	t_{CSC}	20	100,000	20	100,000	25	100,000	ns	–
$\overline{CS}$ hold time	t_{CSH}	70	–	80	–	100	–	ns	–
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	20	50	22	60	25	75	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	17	40	20	50	ns	6
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	10	–	10	–	ns	–
Row address set-up time	t_{ASR}	0	–	0	–	0	–	ns	–
Row address hold time	t_{RAH}	10	–	12	–	15	–	ns	–
Column address set-up time	t_{ASC}	0	–	0	–	0	–	ns	–
Column address hold time	t_{CAH}	15	–	15	–	20	–	ns	–

AC CHARACTERISTICS (CONT.)

Parameter	Symbol	MSM 511002A-70		MSM 511002A-80		MSM 511002A-10		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	–	40	–	50	–	ns	–
Column address hold time reference to $\overline{RAS}$ (WRITE CYCLE)	t_{AWR}	55	–	60	–	75	–	ns	–
Column address hold time reference to $\overline{RAS}$	t_{AR}	85	–	95	–	115	–	ns	–
Column address hold time reference to $\overline{RAS}$ precharge	t_{AH}	10	–	10	–	10	–	ns	–
Column address hold time reference to $\overline{WE}$	t_{AHLW}	65	–	75	–	95	–	ns	–
Last write to column address delay time	t_{LWAD}	20	30	20	35	25	45	ns	7
Read command set-up time	t_{RCS}	0	–	0	–	0	–	ns	–
Read command hold time reference to $\overline{CS}$	t_{RCH}	0	–	0	–	0	–	ns	9
Write command hold time from $\overline{RAS}$	t_{WCR}	55	–	60	–	75	–	ns	–
Write command set-up time	t_{WCS}	0	–	0	–	0	–	ns	8
Write command pulse width	t_{WP}	15	–	15	–	20	–	ns	–
Write invalid time	t_{WI}	10	–	10	–	10	–	ns	–

AC CHARACTERISTICS (CONT.)

Parameter	Symbol	MSM 511002A-70		MSM 511002A-80		MSM 511002A-10		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Write command hold time (Dout disable)	t_{WCH}	15	–	15	–	20	–	ns	–
Data-in hold time from $\overline{RAS}$	t_{DHR}	55	–	60	–	75	–	ns	–
Data output hold time reference to $\overline{WE}$	t_{WOH}	0	–	0	–	0	–	ns	–
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	–	20	–	25	–	ns	–
Write command to $\overline{CS}$ lead time	t_{CWL}	20	–	20	–	25	–	ns	–
Data-in set-up time	t_{DS}	0	–	0	–	0	–	ns	–
Data-in hold time	t_{DH}	15	–	15	–	20	–	ns	–
$\overline{CS}$ to $\overline{WE}$ delay time	t_{CWD}	20	–	20	–	25	–	ns	8
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	70	–	80	–	100	–	ns	8
Column address to $\overline{WE}$ delay time	t_{AWD}	35	–	40	–	50	–	ns	8
$\overline{RAS}$ to second $\overline{WE}$ delay time	t_{RSWD}	80	–	95	–	115	–	ns	–
Read command hold time reference to $\overline{RAS}$	t_{RRH}	0	–	10	–	10	–	ns	9
$\overline{RAS}$ to $\overline{CS}$ set-up time ($\overline{CS}$ before $\overline{RAS}$)	t_{CSR}	10	–	10	–	10	–	ns	–
$\overline{RAS}$ to $\overline{CS}$ hold time ($\overline{CS}$ before $\overline{RAS}$)	t_{CHR}	30	–	30	–	30	–	ns	–
$\overline{CS}$ active delay time from $\overline{RAS}$ precharge	t_{RPC}	10	–	10	–	10	–	ns	–
$\overline{CS}$ precharge time (Refresh counter test)	t_{CPT}	40	–	40	–	50	–	ns	–
$\overline{CS}$ precharge time	t_{CPN}	10	–	10	–	15	–	ns	–

Notes: 1. An initial pause of 100 μs is required after power-up followed by a minimum of any 8 $\overline{RAS}$ cycles (example: $\overline{RAS}$-only Refresh) before proper device operation is achieved.

2. The AC measurements assume the transition time (t_T) = 5 ns.

3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring the timing of the input signals. Transition times are measured between V_{IH} and V_{IL}.

4. Measured using an equivalent load circuit of 2 TTL loads and 100pF.

5. Operating within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. The spec. t_{RCD} (max.) is for reference only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, the access time is controlled exclusively by t_{CAC}.

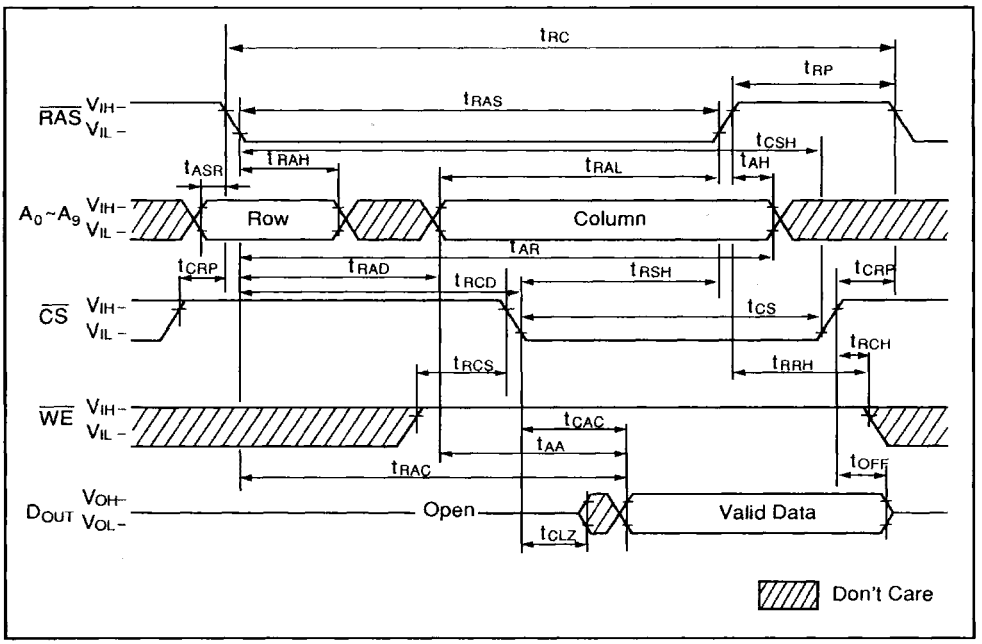
6. Operating within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. The spec. t_{RAD} (max.) is for reference only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled exclusively by t_{AA}.

7. Operating within the t_{LWAD} (max.) limit insures that t_{ALW} (max.) can be met. The spec. t_{LWAD} (max.) is for reference only. If t_{LWAD} is greater than the specified t_{LWAD} (max.) limit, the access time is controlled exclusively by t_{AA}.

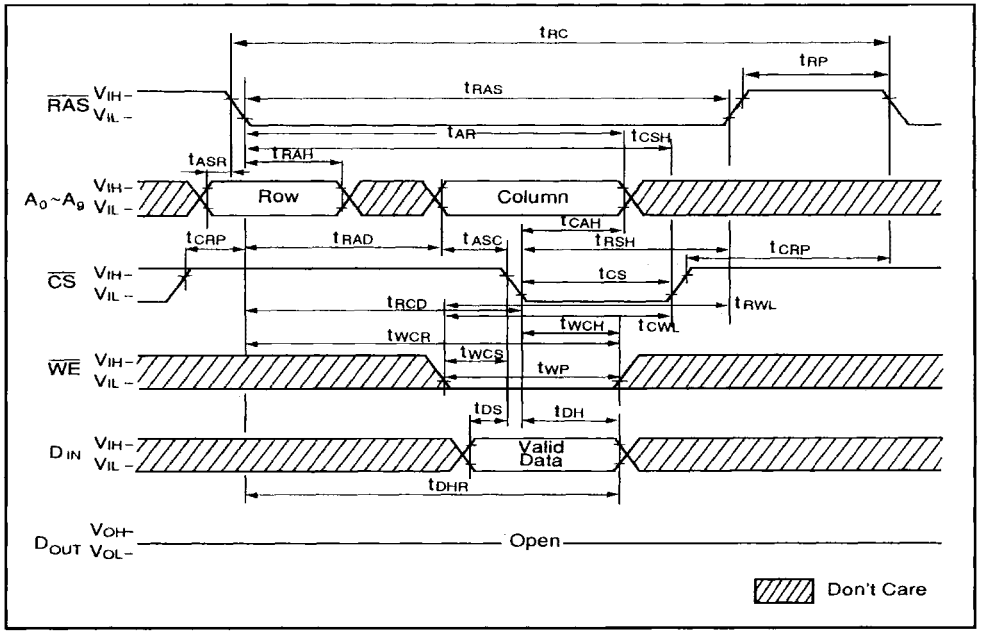
8. The specs t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet for reference only. If $t_{WCS} \geq t_{WCS}$ (min.) the cycle is an Early Write cycle and data out remains in a high impedance state throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} \geq t_{RWD}$ (min.) and $t_{AWD} \geq t_{AWD}$ (min.) the cycle is a Read-Write cycle and the data out contains data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out is indeterminate at access time.

9. Either the t_{RRH} or the t_{RCH} spec. must be satisfied for a proper read cycle.

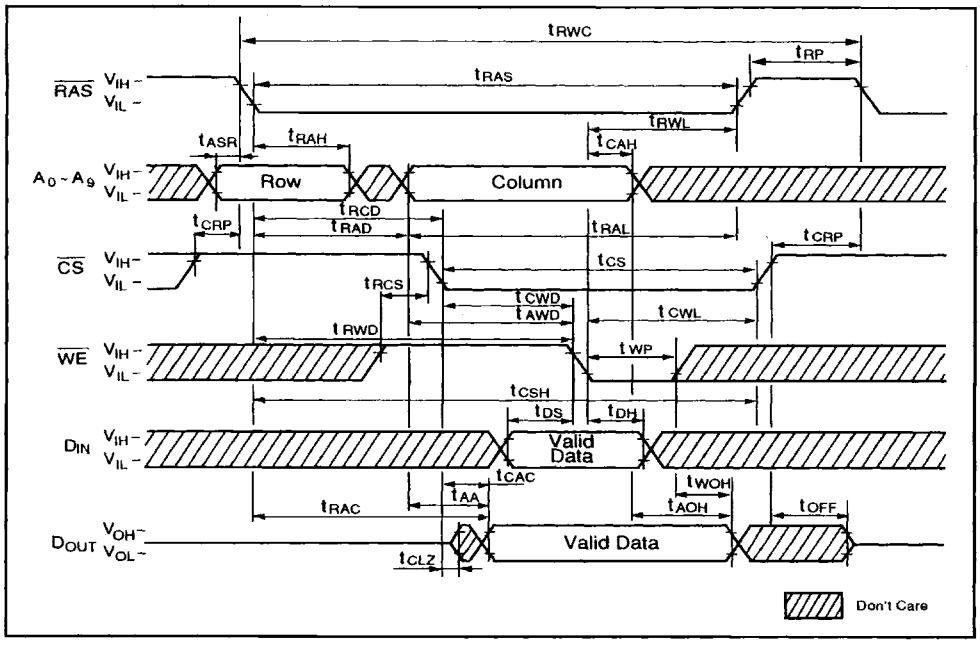
READ CYCLE



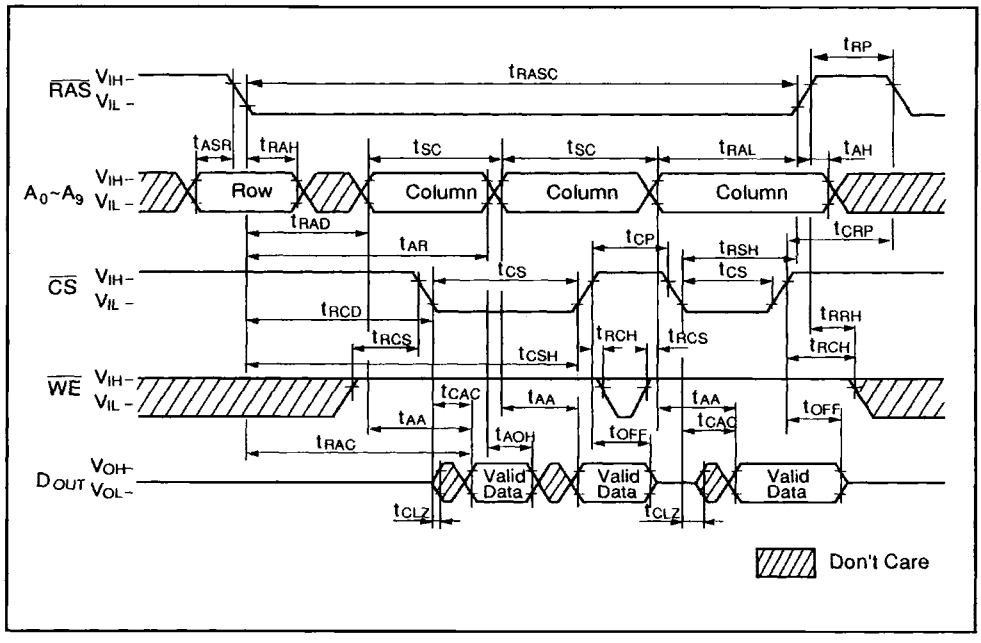
WRITE CYCLE (EARLY TIME)



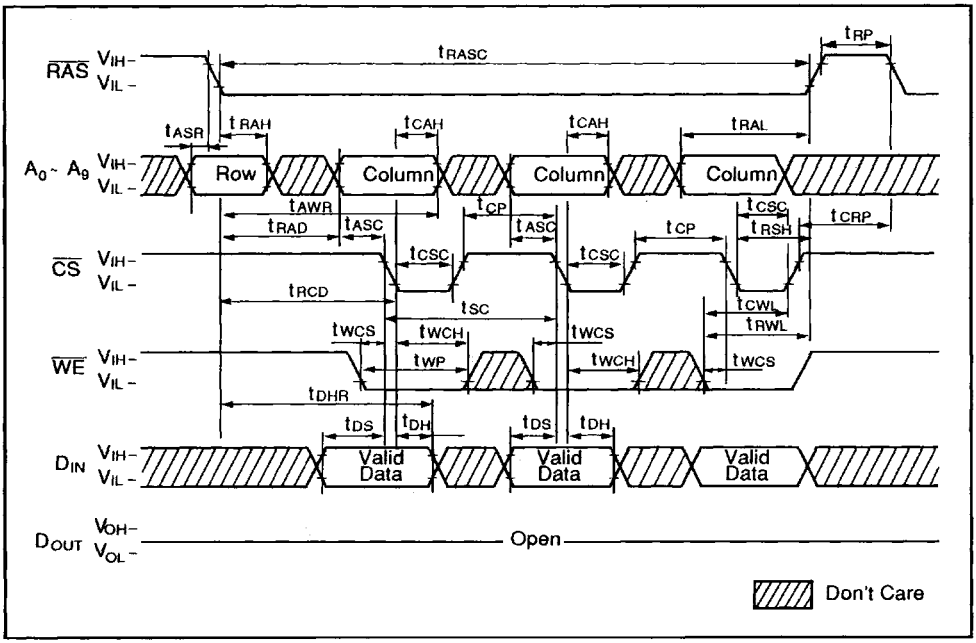
READ/WRITE CYCLE



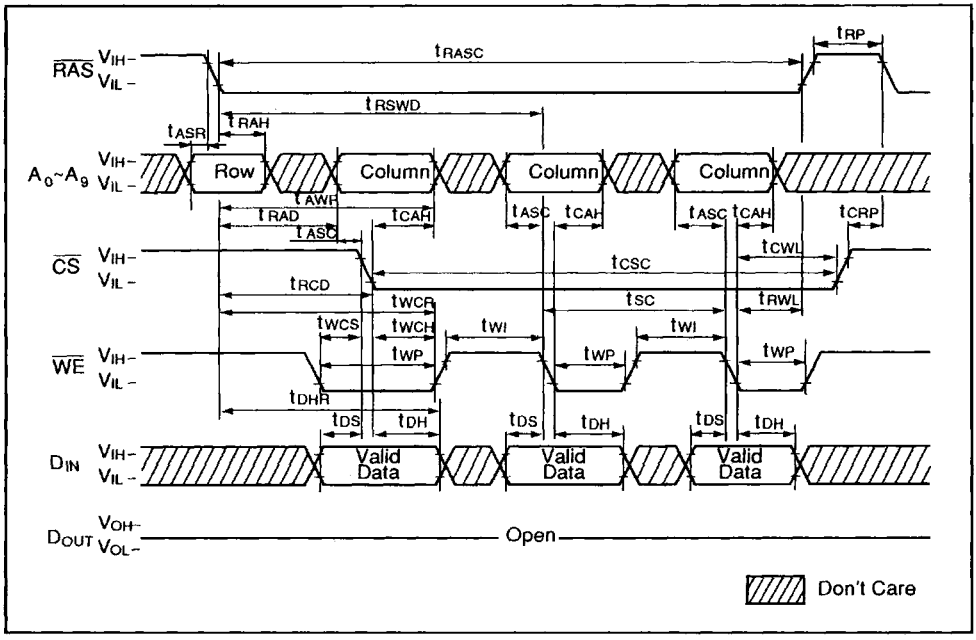
STATIC COLUMN MODE READ CYCLE



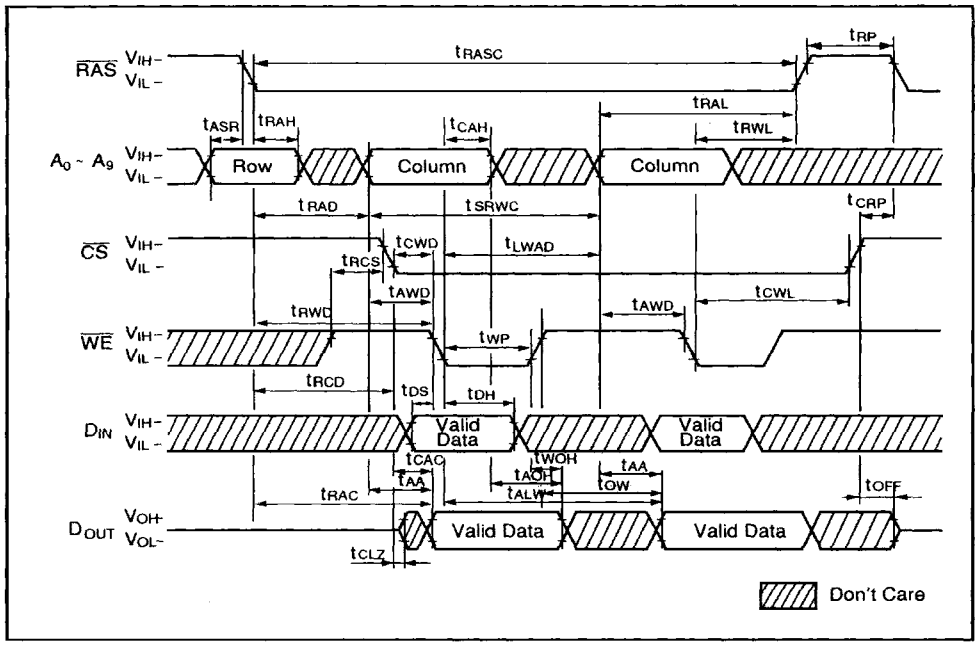
STATIC COLUMN MODE WRITE CYCLE (EARLY TIME)



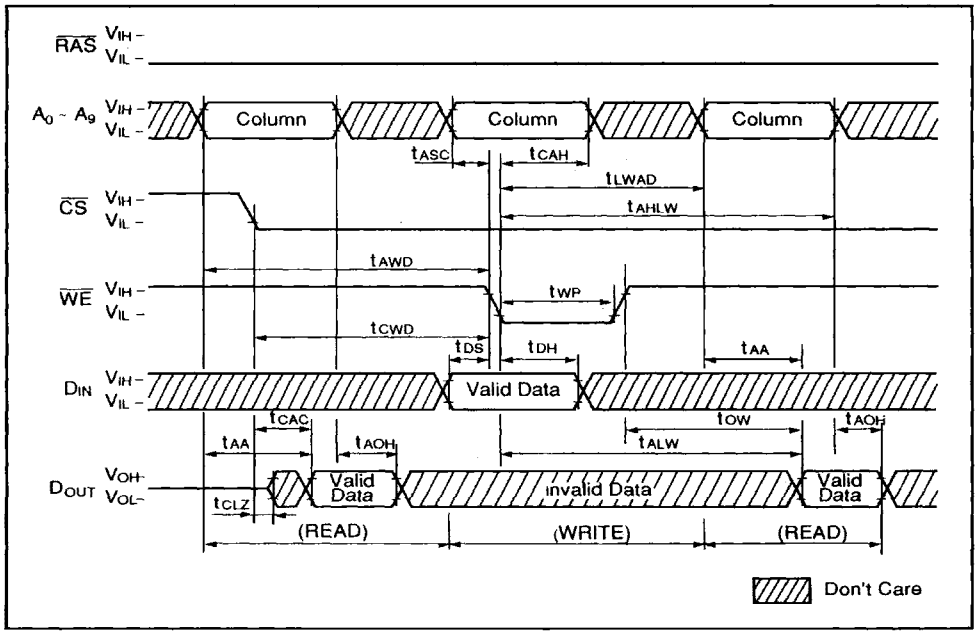
STATIC COLUMN MODE WRITE CYCLE (EARLY TIME)



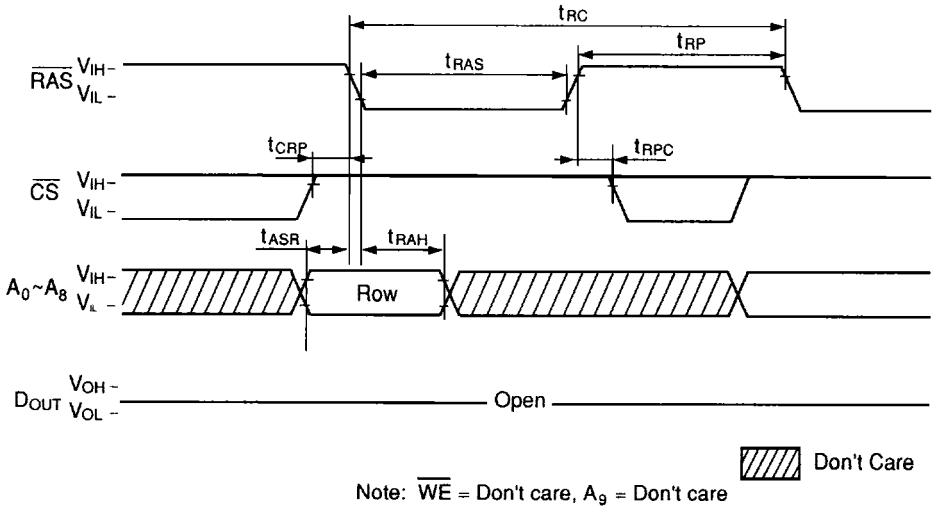
STATIC COLUMN MODE READ/WRITE CYCLE



STATIC COLUMN MODE READ/WRITE MIXED CYCLE

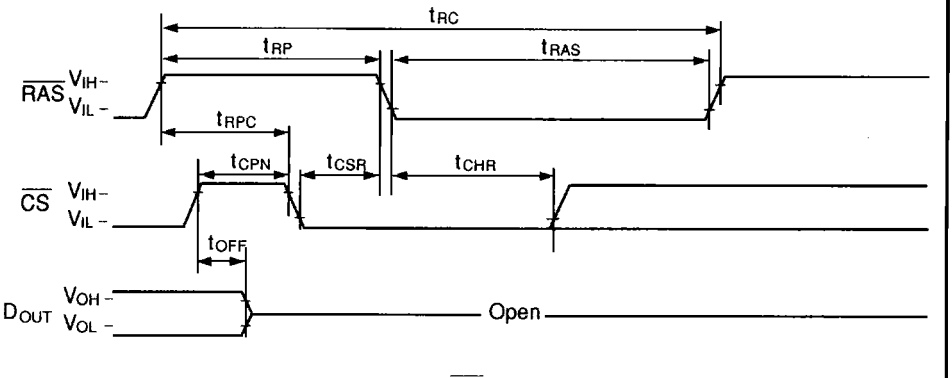


$\overline{RAS}$-ONLY REFRESH CYCLE



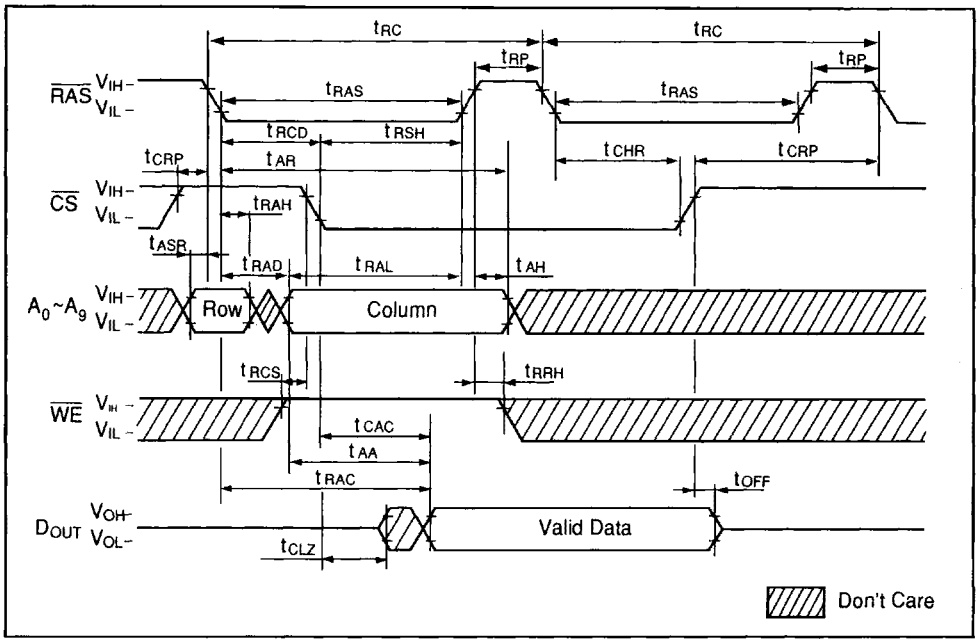
Note: $\overline{WE}$ = Don't care, A_9 = Don't care

$\overline{CS}$ BEFORE $\overline{RAS}$ AUTO-REFRESH CYCLE

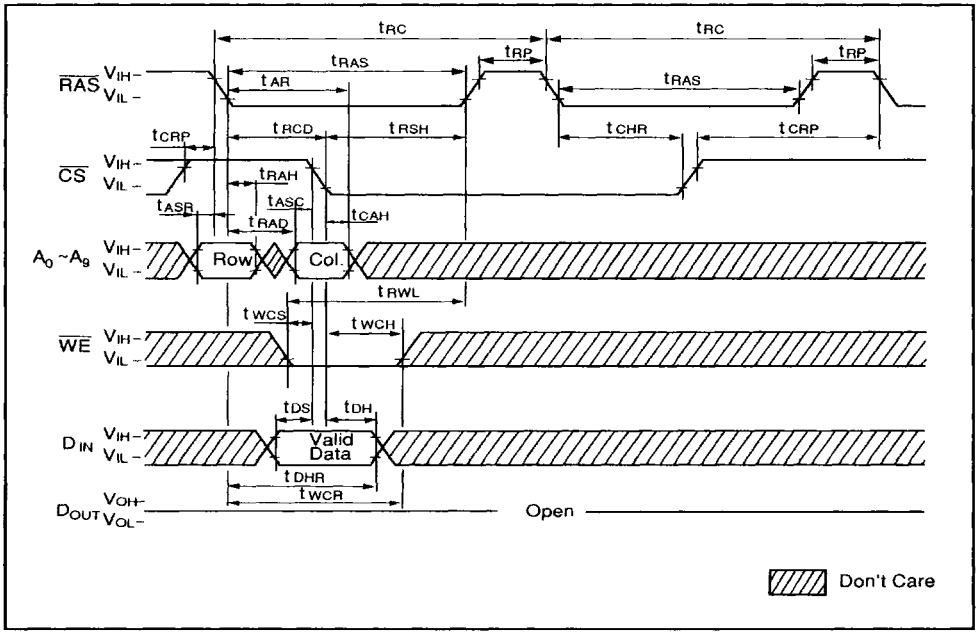


Note: $\overline{WE}$ = Don't care, A_0~A_9 = Don't care

HIDDEN REFRESH READ CYCLE



HIDDEN REFRESH WRITE CYCLE



$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST