QL3040 / QL3040R
40,000 Usable PLD Gate pASIC®3 FPGA
Combining High Performance *and* High Density

PRELIMINARY DATA

pASIC 3 HIGHLIGHTS

High Performance and High Density
-40,000 Usable PLD Gates with 252 I/Os
-16-bit counter speeds over 225 MHz, data path speeds over 275 MHz
-0.35µm four-layer metal non-volatile CMOS process for smallest die sizes

... 40,000 usable PLD gates, 252 I/O pins

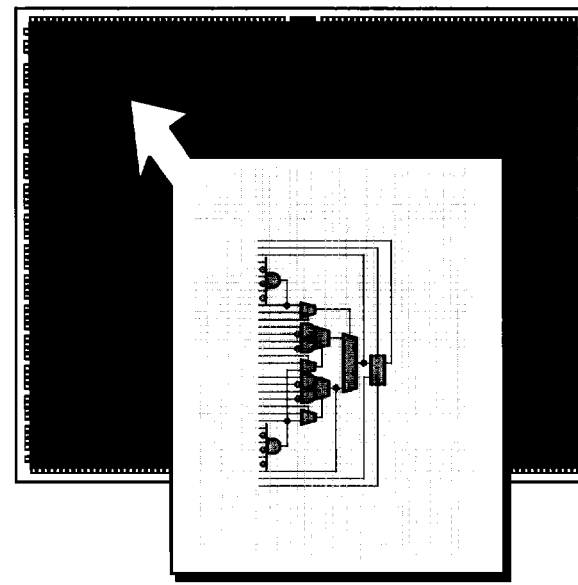
Easy to Use / Fast Development Cycles
-100% routable with 100% utilization and complete pin-out stability
-Variable-grain logic cells provide high performance and 100% utilization
-Comprehensive design tools include high quality Verilog/VHDL synthesis

10,368 bit RAM Option

High Speed Embedded SRAM Available in "R" Versions
-18 dual-port RAM modules, organized in user-configurable 576-bit blocks
-5ns access times, each port independently accessible
-Fast and efficient for FIFO, RAM, and ROM functions

Advanced I/O Capabilities
-Interfaces with both 3.3 volt and 5.0 volt devices
-PCI compliant with 3.3V and 5.0V buses for -1/-2/-3 speed grades
-Full JTAG boundary scan
-Registered I/O cells with individually controlled clocks and output enables

QL3040 Block Diagram



1,008 Logic Cells

QUICKLOGIC

PRODUCT SUMMARY

The QL3040 is a 40,000 usable PLD gate member of the pASIC 3 family of FPGAs. pASIC 3 FPGAs are fabricated on a 0.35µm four-layer metal process using QuickLogic's patented ViaLink technology to provide a unique combination of high performance, high density, low cost, and extreme ease-of-use.

The QL3040 contains 1,008 logic cells. With a maximum of 252 I/Os, the QL3040 is available in 208-PQFP, 256-pin PBGA and 456-pin PBGA packages. The QL3040R also includes 18 dual-port RAM modules, each with 576 bits, for a total of 10,368 bits.

Software support for the complete pASIC 3 family, including the QL3040, is available through three basic packages. The turnkey Quick*Works*® package provides the most complete FPGA software solution from design entry to logic synthesis, to place and route, to simulation. The Quick*Chip*™ and Quick*Tools*™ packages provide a solution for designers who use Cadence, Exemplar, Mentor, Synopsys, Synplicity, Viewlogic, Veribest, or other third-party tools for design entry, synthesis, or simulation.

FEATURES

Total of 252 I/O Pins

- 244 bidirectional input/output pins, PCI-compliant for 5.0 volt and 3.3 volt buses for -1/-2/-3 speed grades
- 8 high-drive input/distributed network pins

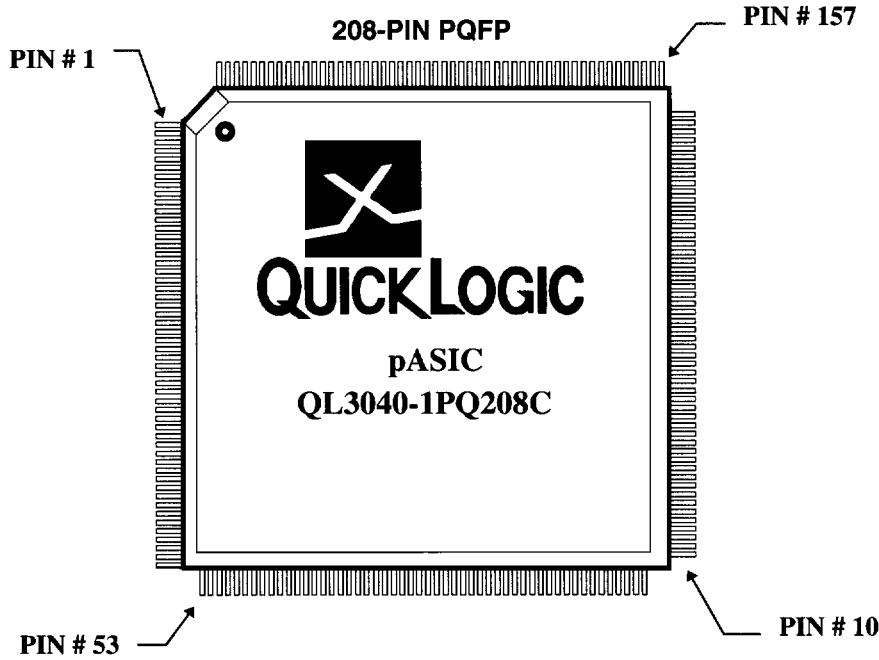
Four Low-Skew (less than 0.5ns) Distributed Networks

- Two array clock/control networks available to the logic cell flip-flop clock, set and reset inputs - each driven by an input-only pin
- Two global clock/control networks available to the logic cell F1, clock, set and reset inputs and the input and I/O register clock, reset and enable inputs as well as the output enable control - each driven by an input-only or I/O pin, or any logic cell output or I/O cell feedback

High Performance

- Input + logic cell + output total delays under 6 ns
- Data path speeds exceeding 275 MHz
- Counter speeds over 225 MHz

PINOUT DIAGRAMS



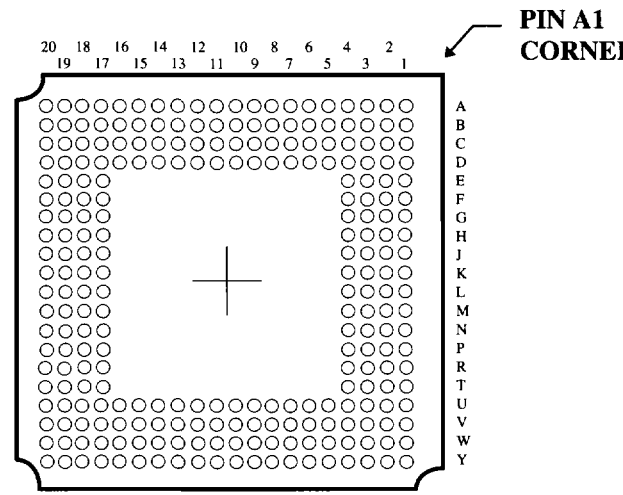
PQFP 208 Pinout Table

208 PQFP	Function	208 PQFP	Function	208 PQFP	Function	208 PQFP	Function	208 PQFP	Function
1	I/O	43	GND	85	I/O	127	GND	169	I/O
2	I/O	44	I/O	86	I/O	128	I/O	170	I/O
3	I/O	45	I/O	87	I/O	129	I	171	I/O
4	I/O	46	I/O	88	I/O	130	ACLK / I	172	I/O
5	I/O	47	I/O	89	I/O	131	VCC	173	I/O
6	I/O	48	I/O	90	I/O	132	I	174	I/O
7	I/O	49	I/O	91	I/O	133	GCLK / I	175	I/O
8	I/O	50	I/O	92	I/O	134	VCC	176	I/O
9	I/O	51	I/O	93	I/O	135	I/O	177	GND
10	VCC	52	I/O	94	I/O	136	I/O	178	I/O
11	I/O	53	I/O	95	GND	137	I/O	179	I/O
12	GND	54	TDI	96	I/O	138	I/O	180	I/O
13	I/O	55	I/O	97	VCC	139	I/O	181	I/O
14	I/O	56	I/O	98	I/O	140	I/O	182	GND
15	I/O	57	I/O	99	I/O	141	I/O	183	I/O
16	I/O	58	I/O	100	I/O	142	I/O	184	I/O
17	I/O	59	GND	101	I/O	143	I/O	185	I/O
18	I/O	60	I/O	102	I/O	144	I/O	186	I/O
19	I/O	61	VCC	103	TRSTB	145	VCC	187	VCCIO
20	I/O	62	I/O	104	TMS	146	I/O	188	I/O
21	I/O	63	I/O	105	I/O	147	GND	189	I/O
22	I/O	64	I/O	106	I/O	148	I/O	190	I/O
23	GND	65	I/O	107	I/O	149	I/O	191	I/O
24	I/O	66	I/O	108	I/O	150	I/O	192	I/O
25	I	67	I/O	109	I/O	151	I/O	193	I/O
26	ACLK / I	68	I/O	110	I/O	152	I/O	194	I/O
27	VCC	69	I/O	111	I/O	153	I/O	195	I/O
28	I	70	I/O	112	I/O	154	I/O	196	I/O
29	GCLK / I	71	I/O	113	I/O	155	I/O	197	I/O
30	VCC	72	I/O	114	VCC	156	I/O	198	I/O
31	I/O	73	GND	115	I/O	157	TCK	199	GND
32	I/O	74	I/O	116	GND	158	STM	200	I/O
33	I/O	75	I/O	117	I/O	159	I/O	201	VCC
34	I/O	76	I/O	118	I/O	160	I/O	202	I/O
35	I/O	77	I/O	119	I/O	161	I/O	203	I/O
36	I/O	78	GND	120	I/O	162	I/O	204	I/O
37	I/O	79	I/O	121	I/O	163	GND	205	I/O
38	I/O	80	I/O	122	I/O	164	I/O	206	I/O
39	I/O	81	I/O	123	I/O	165	VCC	207	TDO
40	I/O	82	I/O	124	I/O	166	I/O	208	I/O
41	VCC	83	VCCIO	125	I/O	167	I/O		
42	I/O	84	I/O	126	I/O	168	I/O		

PINOUT DIAGRAM

256-PIN PBGA

TOP



BOTTOM

Contact QuickLogic regarding availability of the 456-pin PBGA.

PBGA 256 Pinout Table

256 PBGA	Function	256 PBGA	Function	256 PBGA	Function	256 PBGA	Function	256 PBGA	Function	256 PBGA	Function
A1	VSS	C4	I/O	E19	I/O	L2	ACLK / I	T17	I/O	V20	I/O
A2	I/O	C5	I/O	E20	I/O	L3	I	T18	I/O	W1	I/O
A3	I/O	C6	I/O	F1	I/O	L4	GCLK / I	T19	I/O	W2	I/O
A4	I/O	C7	I/O	F2	I/O	L17	VCC	T20	I/O	W3	TDI
A5	I/O	C8	I/O	F3	I/O	L18	I/O	U1	I/O	W4	I/O
A6	I/O	C9	VCCIO	F4	VCC	L19	I/O	U2	I/O	W5	I/O
A7	I/O	C10	I/O	F17	VCC	L20	I/O	U3	I/O	W6	I/O
A8	I/O	C11	I/O	F18	I/O	M1	I/O	U4	VSS	W7	I/O
A9	I/O	C12	I/O	F19	I/O	M2	I/O	U5	I/O	W8	I/O
A10	I/O	C13	I/O	F20	I/O	M3	I/O	U6	VCC	W9	I/O
A11	I/O	C14	I/O	G1	I/O	M4	I/O	U7	I/O	W10	I/O
A12	I/O	C15	I/O	G2	I/O	M17	I/O	U8	VSS	W11	I/O
A13	I/O	C16	I/O	G3	I/O	M18	I/O	U9	I/O	W12	I/O
A14	I/O	C17	I/O	G4	I/O	M19	I/O	U10	VCC	W13	I/O
A15	I/O	C18	I/O	G17	I/O	M20	I/O	U11	I/O	W14	I/O
A16	I/O	C19	I/O	G18	I/O	N1	I/O	U12	I/O	W15	I/O
A17	I/O	C20	I/O	G19	I/O	N2	I/O	U13	VSS	W16	I/O
A18	I/O	D1	I/O	G20	I/O	N3	I/O	U14	I/O	W17	I/O
A19	TCK	D2	I/O	H1	I/O	N4	VSS	U15	VCC	W18	I/O
A20	I/O	D3	I/O	H2	I/O	N17	VSS	U16	I/O	W19	I/O
B1	TDO	D4	VSS	H3	I/O	N18	I/O	U17	VSS	W20	TRSTB
B2	I/O	D5	I/O	H4	VSS	N19	I/O	U18	I/O	Y1	I/O
B3	I/O	D6	VCC	H17	VSS	N20	I/O	U19	I/O	Y2	I/O
B4	I/O	D7	I/O	H18	I/O	P1	I/O	U20	I/O	Y3	I/O
B5	I/O	D8	VSS	H19	I/O	P2	I/O	V1	I/O	Y4	I/O
B6	I/O	D9	I/O	H20	I/O	P3	I/O	V2	I/O	Y5	I/O
B7	I/O	D10	I/O	J1	I/O	P4	I/O	V3	I/O	Y6	I/O
B8	I/O	D11	VCC	J2	I/O	P17	I/O	V4	I/O	Y7	I/O
B9	I/O	D12	I/O	J3	I/O	P18	I/O	V5	I/O	Y8	I/O
B10	I/O	D13	VSS	J4	I/O	P19	I/O	V6	I/O	Y9	I/O
B11	I/O	D14	I/O	J17	I/O	P20	I/O	V7	I/O	Y10	I/O
B12	I/O	D15	VCC	J18	I/O	R1	I/O	V8	I/O	Y11	I/O
B13	I/O	D16	I/O	J19	I/O	R2	I/O	V9	I/O	Y12	I/O
B14	I/O	D17	VSS	J20	GCLK / I	R3	I/O	V10	I/O	Y13	I/O
B15	I/O	D18	I/O	K1	I/O	R4	VCC	V11	I/O	Y14	I/O
B16	I/O	D19	I/O	K2	I/O	R17	VCC	V12	VCCIO	Y15	I/O
B17	I/O	D20	I/O	K3	I/O	R18	I/O	V13	I/O	Y16	I/O
B18	STM	E1	I/O	K4	VCC	R19	I/O	V14	I/O	Y17	I/O
B19	I/O	E2	I/O	K17	I	R20	I/O	V15	I/O	Y18	I/O
B20	I/O	E3	I/O	K18	ACLK / I	T1	I/O	V16	I/O	Y19	I/O
C1	I/O	E4	I/O	K19	I	T2	I/O	V17	I/O	Y20	I/O
C2	I/O	E17	I/O	K20	I/O	T3	I/O	V18	I/O		
C3	I/O	E18	I/O	L1	I	T4	I/O	V19	TMS		

PIN DESCRIPTIONS

Pin	Function	Description
TDI	Test Data In for JTAG	Hold HIGH during normal operation. Connect to VCC if not used for JTAG.
TRSTB	Active low Reset for JTAG	Hold LOW during normal operation. Connect to ground if not used for JTAG.
TMS	Test Mode Select for JTAG	Hold HIGH during normal operation. Connect to VCC if not used for JTAG.
TCK	Test Clock for JTAG	Hold HIGH or LOW during normal operation. Connect to VCC or ground if not used for JTAG.
TDO	Test data out for JTAG	Output that must be left unconnected if not used for JTAG.
STM	Special Test Mode	Must be grounded during normal operation.
I/ACLK	High-drive input and/or array network driver	Can be configured as either or both.
I/GCLK	High-drive input and/or global network driver	Can be configured as either or both.
I	High-drive input	Use for input signals with high fanout.
I/O	Input/Output pin	Can be configured as an input and/or output.
VCC	Power supply pin	Connect to 3.3V supply.
VCCIO	Input voltage tolerance pin	Connect to 5.0 volt supply if 5 volt input tolerance is required, otherwise connect to 3.3V supply.
GND	Ground pin	Connect to ground.

ORDERING INFORMATION

QL 3040 R - 1 PQ208 C

- QL — QuickLogic pASIC device
- 3040 — pASIC 3 device part number
- R — Blank: 3.3V 0.35 micron CMOS; R: 3.3V 0.35 micron CMOS with embedded RAM
- 1 — Speed Grade: 0 = quick, 1 = fast, 2 = faster, 3 = fastest
- PQ208 — Package Code: PQ208 = 208-pin PQFP, PB256 = 256-pin PBGA, *PB456 = 456-pin PBGA
- C — Operating Range: C = Commercial, I = Industrial, *M = Military

* Contact QuickLogic regarding availability.

ABSOLUTE MAXIMUM RATINGS

VCC Voltage ..... -0.5 to 4.6V
VCCIO Voltage.....-0.5 to 7.0V
Input Voltage ..... -0.5 to VCC +0.5V
Latch-up Immunity ..... ±200 mA

DC Input Current .....±20 mA
ESD Pad Protection .....±2000V
Storage Temperature.....-65°C to + 150°C
Lead Temperature .....300°C

OPERATING RANGE

Symbol	Parameter		Military		Industrial		Commercial		Unit
			Min	Max	Min	Max	Min	Max	
VCC	Supply Voltage		3.0	3.6	3.0	3.6	3.0	3.6	V
VCCIO	I/O Input Tolerance Voltage		3.0	5.5	3.0	5.5	3.0	5.25	V
TA	Ambient Temperature		-55		-40	85	0	70	°C
TC	Case Temperature			125					°C
K	Delay Factor	-0 Speed Grade			0.42	1.92	0.46	1.85	
		-1 Speed Grade	0.41	1.69	0.42	1.55	0.46	1.50	
		-2 Speed Grade	0.41	1.41	0.42	1.29	0.46	1.25	
		-3 Speed Grade			0.42	1.14	0.46	1.10	

DC CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Max	Unit
VIH	Input HIGH Voltage		0.5VCC	VCCIO+0.5	V
VIL	Input LOW Voltage		-0.5	0.3VCC	V
VOH	Output HIGH Voltage	IOH = -12 mA	2.4		V
		IOH = -500 µA	0.9VCC		V
VOL	Output LOW Voltage	IOL = 16 mA [1]		0.45	V
		IOL = 1.5 mA		0.1VCC	V
II	I or I/O Input Leakage Current	VI = VCCIO or GND	-10	10	µA
IOZ	3-State Output Leakage Current	VI = VCCIO or GND	-10	10	µA
CI	Input Capacitance [2]			10	pF
IOS	Output Short Circuit Current [3]	VO = GND	-15	-180	mA
		VO = VCC	40	210	mA
ICC	D.C. Supply Current [4]	VI, VIO = VCCIO or GND	0.50 (typ)	2	mA
ICCIO	D.C. Supply Current on VCCIO		0	100	µA

Notes:

[1] Applies only to -1/-2/-3 commercial grade devices. These speed grades are also PCI-compliant. All other devices have 8 mA IOL specifications.
[2] Capacitance is sample tested only. Clock pins are 12 pF maximum.
[3] Only one output at a time. Duration should not exceed 30 seconds.
[4] For -1/-2/-3 commercial grade devices only. Maximum ICC is 3 mA for -0 commercial grade and all industrial grade devices, and 5 mA for all military grade devices. For AC conditions, contact QuickLogic customer engineering.

AC CHARACTERISTICS at VCC = 3.3V, TA = 25°C (K = 1.00)

(To calculate delays, multiply the appropriate K factor in the "Operating Range" section by the following numbers.)

Logic Cells

Symbol	Parameter	Propagation Delays (ns) Fanout [5]				
		1	2	3	4	8
tPD	Combinatorial Delay [6]	1.4	1.7	2.0	2.3	3.5
tSU	Setup Time [6]	1.8	1.8	1.8	1.8	1.8
tH	Hold Time	0.0	0.0	0.0	0.0	0.0
tCLK	Clock to Q Delay	0.8	1.1	1.4	1.7	2.9
tCWHI	Clock High Time	1.6	1.6	1.6	1.6	1.6
tCWLO	Clock Low Time	1.6	1.6	1.6	1.6	1.6
tSET	Set Delay	1.4	1.7	2.0	2.3	3.5
tRESET	Reset Delay	1.2	1.5	1.8	2.1	3.3
tSW	Set Width	1.9	1.9	1.9	1.9	1.9
tRW	Reset Width	1.8	1.8	1.8	1.8	1.8

Input-Only Cells

Symbol	Parameter	Propagation Delays (ns) Fanout [5]						
		1	2	3	4	8	12	24
tIN	High Drive Input Delay	2.5	2.6	2.6	2.7	3.5	4.6	5.8
tINI	High Drive Input, Inverting Delay	2.6	2.7	2.7	2.8	3.6	4.7	5.9
tISU	Input Register Set-Up Time	4.8	4.8	4.8	4.8	4.8	4.8	4.8
tIH	Input Register Hold Time	0.0	0.0	0.0	0.0	0.0	0.0	0.0
tICLK	Input Register Clock To Q	0.9	1.0	1.0	1.1	1.9	3.0	4.2
tIRST	Input Register Reset Delay	0.8	0.9	0.9	1.0	1.8	2.9	4.1
tIESU	Input Register clock Enable Set-Up Time	4.1	4.1	4.1	4.1	4.1	4.1	4.1
tIEH	Input Register Clock Enable Hold Time	0.0	0.0	0.0	0.0	0.0	0.0	0.0

Notes:

[5] Stated timing for worst case Propagation Delay over process variation at VCC=3.3V and TA=25°C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage and temperature settings as specified in the Operating Range.

[6] These limits are derived from a representative selection of the slowest paths through the pASIC 3 logic cell *including typical net delays*. Worst case delay values for specific paths should be determined from timing analysis of your particular design.

Clock Cells

Symbol	Parameter	Propagation Delays (ns) Loads per Half Column [7]								
		1	2	3	4	8	10	12	14	16
tACK	Array Clock Delay	2.2	2.2	2.3	2.4	2.5	2.6	2.7	2.7	
tGCKP	Global Clock Pin Delay	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2
tGCKB	Global Clock Buffer Delay	1.5	1.6	1.6	1.7	1.8	1.9	2.0	2.1	2.2

I/O Cells

Symbol	Parameter	Propagation Delays (ns) Fanout [5]					
		1	2	3	4	8	10
tI/O	Input Delay (bidirectional pad)	1.8	2.1	2.4	2.7	3.9	4.6
tISU	Input Register Set-Up Time	4.8	4.8	4.8	4.8	4.8	4.8
tIH	Input Register Hold Time	0.0	0.0	0.0	0.0	0.0	0.0
tIOCLK	Input Register Clock To Q	0.8	1.1	1.4	1.7	2.9	3.6
tIORST	Input Register Reset Delay	0.7	1.0	1.3	1.6	2.8	3.5
tIESU	Input Register clock Enable Set-Up Time	4.1	4.1	4.1	4.1	4.1	4.1
tIEH	Input Register Clock Enable Hold Time	0.0	0.0	0.0	0.0	0.0	0.0

Symbol	Parameter	Propagation Delays (ns) Output Load Capacitance (pF)				
		30	50	75	100	150
tOUTLH	Output Delay Low to High	2.6	3.0	3.6	4.1	5.2
tOUTHL	Output Delay High to Low	2.8	3.3	3.9	4.5	5.7
tPZH	Output Delay Tri-state to High	2.1	2.6	3.1	3.7	4.8
tPZL	Output Delay Tri-state to Low	2.6	3.3	4.1	4.9	6.5
tPHZ	Output Delay High to Tri-State [8]	2.9				
tPLZ	Output Delay Low to Tri-State [8]	3.3				

Notes:

[7] The array distributed networks consist of 72 half columns and the global distributed networks consist of 76 half columns, each driven by an independent buffer. The number of half columns used does not affect clock buffer delay. The array clock has up to 14 loads per half column. The global clock has up to 16 loads per half column.

[8] The following loads are used for tPXZ: