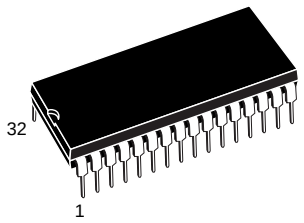
M28010

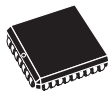
1 Mbit (128K x 8) Parallel EEPROM With Software Data Protection

DATA BRIEFING

- Fast Access Time: 100 ns
- Single Supply Voltage:
  - 4.5 V to 5.5 V for M28010
  - 2.7 V to 3.6 V for M28010-W
  - 1.8 V to 2.4 V for M28010-R
- Low Power Consumption
- Fast BYTE and PAGE WRITE (up to 128 Bytes)
- Enhanced Write Detection and Monitoring:
  - Data Polling
  - Toggle Bit
  - Page Load Timer Status
- JEDEC Approved Bytewide Pin-Out
- Software Data Protection
- Hardware Data Protection
- Software Chip Erase
- 100000 Erase/Write Cycles (minimum)
- Data Retention (minimum): 10 Years



PDIP32 (BA)



PLCC32 (KA)

TSOP32 (NA)
8 x 20 mm

DESCRIPTION

The M28010 devices consist of 128Kx8 bits of low power, parallel EEPROM, fabricated with STMicroelectronics' proprietary double polysilicon CMOS technology. The devices offer fast access time, with low power dissipation, and require a single voltage supply (5V, 3V or 2V, depending on the option chosen).

Table 1. Signal Names

A0-A16	Address Input
DQ0-DQ7	Data Input / Output
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

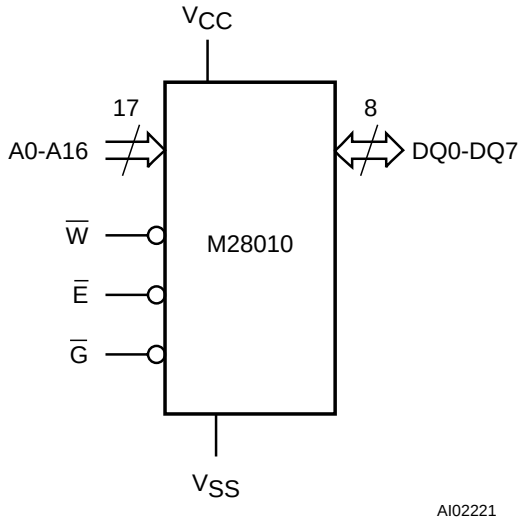
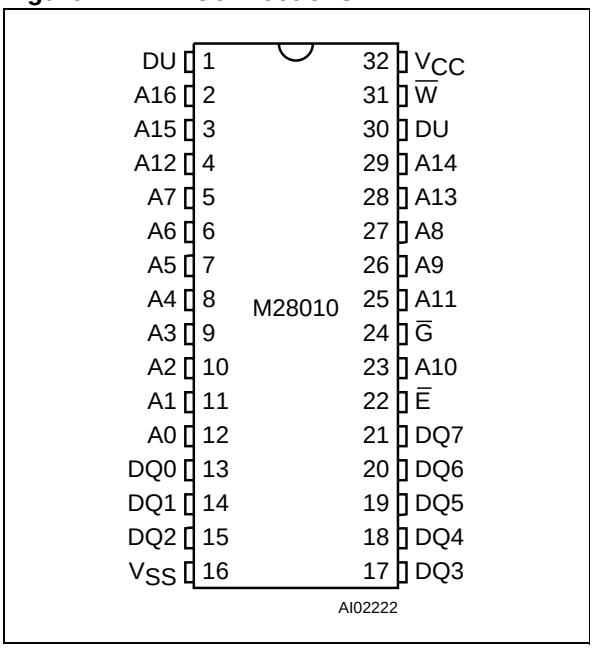
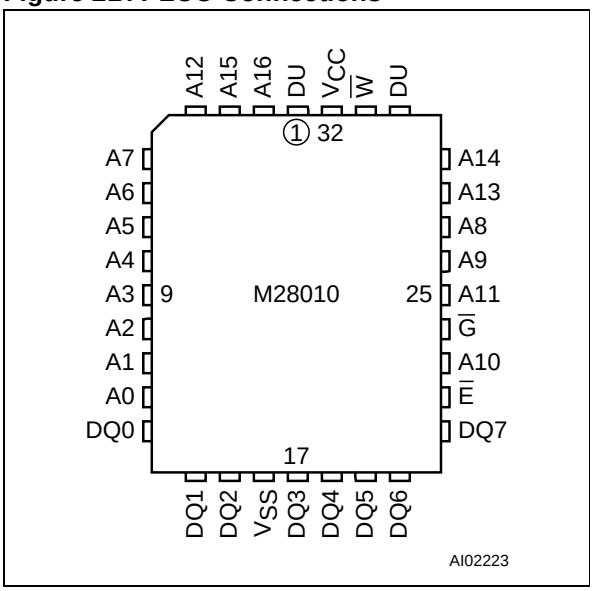


Figure 2A. DIP Connections



Note: 1. DU = Do Not Use

Figure 2B. PLCC Connections

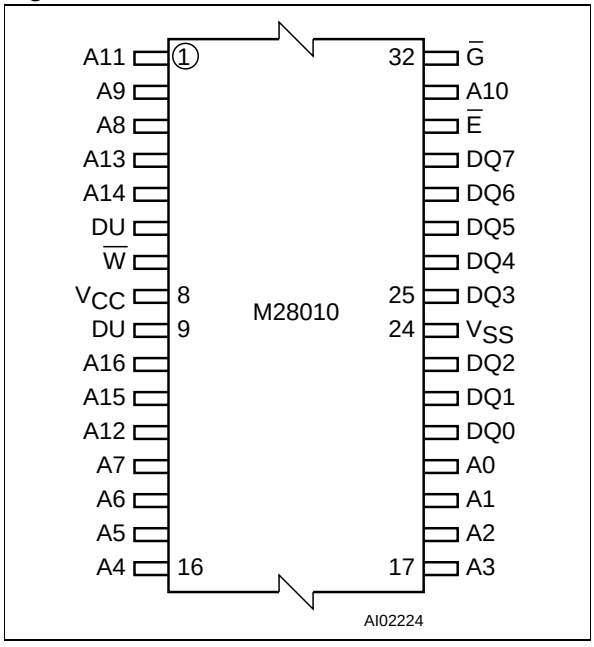


Note: 1. DU = Do Not Use

The device has been designed to offer a flexible microcontroller interface, featuring both hardware and software hand-shaking, with Data Polling and Toggle Bit. The device supports a 128 byte Page Write operation. Software Data Protection (SDP) is also supported, using the standard JEDEC algorithm.

The M28010 is designed for applications requiring as much as 100,000 write cycles and ten years of

Figure 2C. TSOP Connections



Note: 1. DU = Do Not Use

data retention. The organization of the data in a 4 byte (32-bit) “word” format leads to significant savings in power consumption. Once a byte has been read, subsequent byte read cycles from the same “word” (with addresses differing only in the two least significant bits) are fetched from the previously loaded Read Buffer, not from the memory array. As a result, the power consumption for these subsequent read cycles is much lower than the power consumption for the first cycle. By careful design of the memory access patterns, a 50% reduction in the power consumption is possible.

ORDERING INFORMATION

Devices are shipped from the factory with the memory content set at all ‘1’s (FFh).

The notation used for the device number is as shown in Table 2. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

Table 2. Ordering Information Scheme

Example: M28010 -10 W KA 6 T

Speed

-10	100 ns
-12	120 ns
-15	150 ns
-20	200 ns
-25	250 ns

Operating Voltage

blank	4.5 V to 5.5 V
W	2.7 V to 3.6 V
R	1.8 V to 2.4 V

Option

T	Tape & Reel Packing

Temperature Range

1[1]	0 to 70 °C
6	–40 to 85 °C

Package

BA	PDIP32
KA	PLCC32
NA	TSOP32: 8 x 20mm

Note: 1. This temperature range on request only.