Direct RDRAM RIMM Modules

HYR16xx30/HYR18xx20G
Rambus RIMM Modules
(with 128/144 Mb RDRAMs)

Perliminary Information

Rev. 0.9

Overview

The Direct Rambus™ RIMM™ module is a general purpose high-performance memory subsystem suitable for use in a broad range of applications including computer memory, personal computers, workstations, and other applications where high bandwidth and low latency are required.

The 128 MB Direct Rambus RIMM module consists of eight 128Mb/ 144Mb Direct Rambus DRAM (Direct RDRAM™) devices. These are extremely high-speed CMOS DRAMs organized as 8M words by 16 or 18 bits. The use of Rambus Signaling Level (RSL) technology permits 600MHz to 800MHz transfer rates while using conventional system and board design technologies. Direct RDRAM devices are capable of sustained data transfers at 1.25 ns per two bytes (10ns per sixteen bytes).

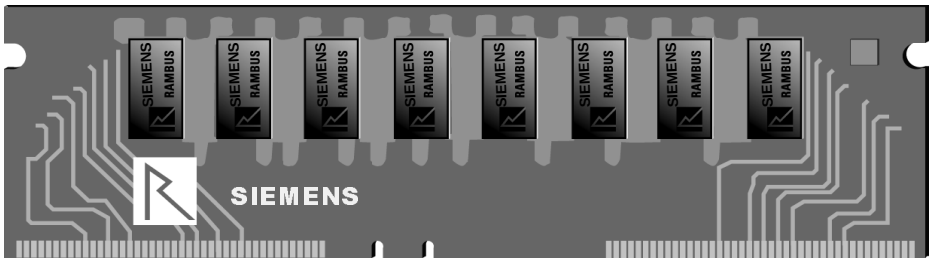
The RDRAM architecture enables the highest sustained bandwidth for multiple, simultaneous, randomly addressed, memory transactions. The separate control and data buses with independent row and column control yield over 95% bus efficiency. The RDRAM's 32-bank architecture supports up to four simultaneous transactions per device.

Form Factor

The Rambus RIMM modules are offered in a 184-pad 1mm edge connector pad pitch form factor suitable for either 184 or 168 contact RIMM connectors. The RIMM module is suitable for desktop and other system applications. Figure 1 shows an eight device Rambus RIMM module without heat spreader.

Features

- High speed 800, 711 & 600 MHz RDRAM storage
- 184 edge connector pads with 1mm pad spacing
- Maximum module PCB size: 133.5mm x 34.9mm x 1.37mm (5.21” x 1.36” x 0.05”)
- Each RDRAM has 32 banks, for a total of 256banks on each 128MB module
- Gold plated edge connector pad contacts
- Serial Presence Detect (SPD) support
- Operates from a 2.5 volt supply (±5%)
- Low power and powerdown self refresh modes
- Separate Row and Column buses for higher efficiency



Part Number Designators

Organization	Capacity	I/O Freq. MHz	Part Designator	# of RDRAMs	RDRAM density
64MB/72MB:					
32Mb x16	64MB	600	**HYR163230G-653**	4	128Mb
32Mb x16	64MB	711	**HYR163230G-745**	4	128Mb
32Mb x16	64MB	800	**HYR163230G-845**	4	128Mb
32Mb x16	64MB	800	**HYR163230G-840**	4	128Mb
32Mb x18	72MB	600	**HYR183220G-653**	4	144Mb
32Mb x18	72MB	711	**HYR183220G-745**	4	144Mb
32Mb x18	72MB	800	**HYR183220G-845**	4	144Mb
32Mb x18	72MB	800	**HYR183220G-840**	4	144Mb
96MB/108MB					
48Mb x16	96MB	600	**HYR164830G-653**	6	128Mb
48Mb x16	96MB	711	**HYR164830G-745**	6	128Mb
48Mb x16	96MB	800	**HYR164830G-845**	6	128Mb
48Mb x16	96MB	800	**HYR164830G-840**	6	128Mb
48Mb x18	108MB	600	**HYR184820G-653**	6	144Mb
48Mb x18	108MB	711	**HYR184820G-745**	6	144Mb
48Mb x18	108MB	800	**HYR184820G-845**	6	144Mb
48Mb x18	108MB	800	**HYR184820G-840**	6	144Mb
128MB/144MB:					
64Mb x16	128MB	600	**HYR166430G-653**	8	128Mb
64Mb x16	128MB	711	**HYR166430G-711**	8	128Mb
64Mb x16	128MB	800	**HYR166430G-845**	8	128Mb
64Mb x16	128MB	800	**HYR166430G-840**	8	128Mb
64Mb x18	144MB	600	**HYR186420G-653**	8	144Mb
64Mb x18	144MB	711	**HYR186420G-711**	8	144Mb
64Mb x18	144MB	800	**HYR186420G-845**	8	144Mb
64Mb x18	144MB	800	**HYR186420G-840**	8	144Mb
256MB/288MB:					
128Mb x16	256MB	600	**HYR1612830G-653**	16	128Mb
128Mb x16	256MB	711	**HYR1612830G-745**	16	128Mb
128Mb x16	256MB	800	**HYR1612830G-845**	16	128Mb
128Mb x16	256MB	800	**HYR1612830G-840**	16	128Mb
128Mb x18	288MB	600	**HYR1812820G-653**	16	144Mb
128Mb x18	288MB	711	**HYR1812820G-745**	16	144Mb
128Mb x18	288MB	800	**HYR1812820G-845**	16	144Mb
128Mb x18	288MB	800	**HYR1812820G-840**	16	144Mb

Table 1: Module Pad Number and Signal Names

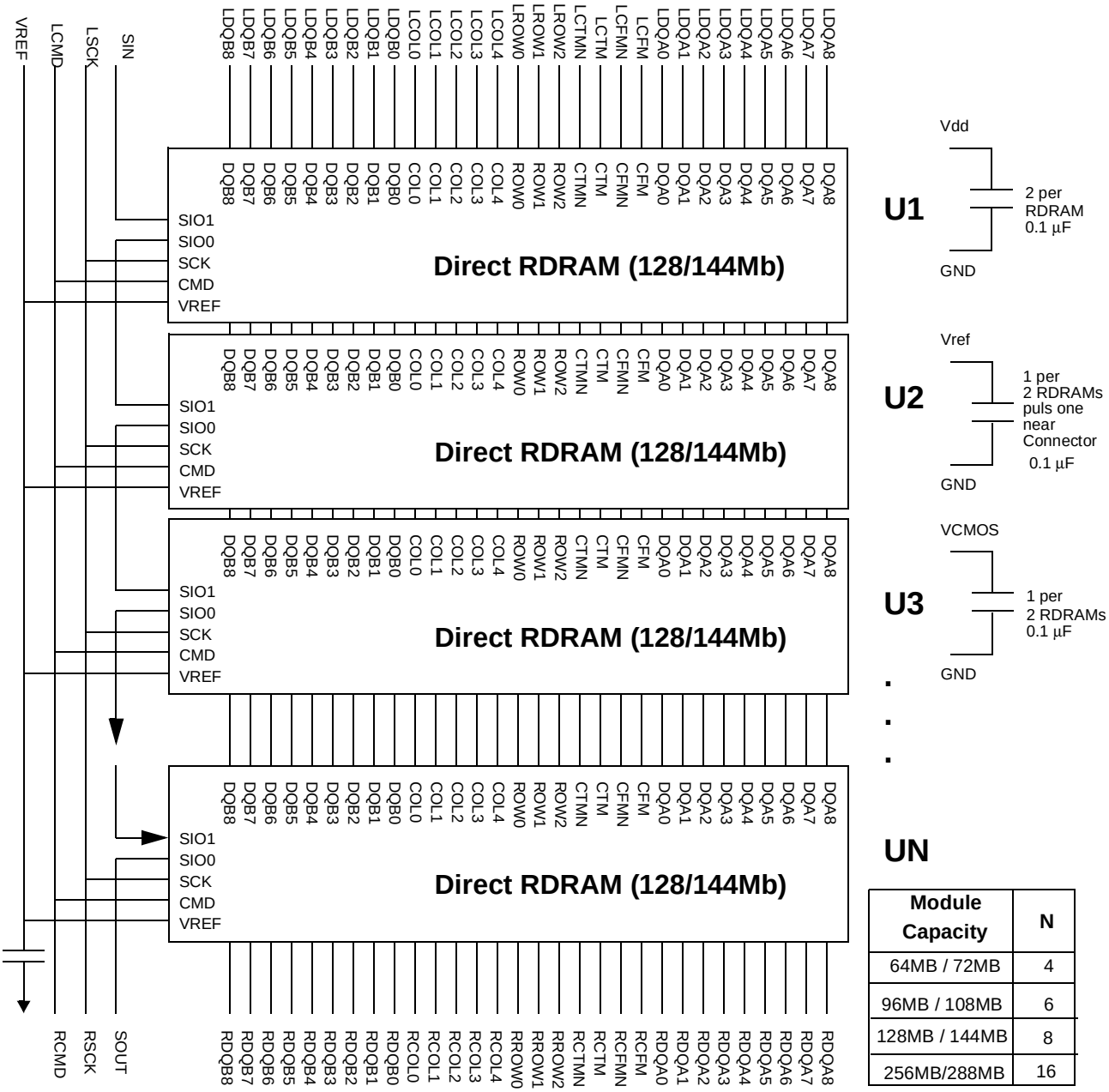
Pad	Signal Name	Pad	Signal Name
A1	Gnd	B1	Gnd
A2	LDQA8	B2	LDQA7
A3	Gnd	B3	Gnd
A4	LDQA6	B4	LDQA5
A5	Gnd	B5	Gnd
A6	LDQA4	B6	LDQA3
A7	Gnd	B7	Gnd
A8	LDQA2	B8	LDQA1
A9	Gnd	B9	Gnd
A10	LDQA0	B10	LCFM
A11	Gnd	B11	Gnd
A12	LCTMN	B12	LCFMN
A13	Gnd	B13	Gnd
A14	LCTM	B14	NC
A15	Gnd	B15	Gnd
A16	NC	B16	LROW2
A17	Gnd	B17	Gnd
A18	LROW1	B18	LROW0
A19	Gnd	B19	Gnd
A20	LCOL4	B20	LCOL3
A21	Gnd	B21	Gnd
A22	LCOL2	B22	LCOL1
A23	Gnd	B23	Gnd
A24	LCOL0	B24	LDQB0
A25	Gnd	B25	Gnd
A26	LDQB1	B26	LDQB2
A27	Gnd	B27	Gnd
A28	LDQB3	B28	LDQB4
A29	Gnd	B29	Gnd
A30	LDQB5	B30	LDQB6
A31	Gnd	B31	Gnd
A32	LDQB7	B32	LDQB8
A33	Gnd	B33	Gnd
A34	LSCK	B34	LCMD
A35	Vcmos	B35	Vcmos
A36	SOUT	B36	SIN
A37	Vcmos	B37	Vcmos
A38	NC	B38	NC
A39	Gnd	B39	Gnd
A40	NC	B40	NC
A41	Vdd	B41	Vdd
A42	Vdd	B42	Vdd
A43	NC	B43	NC
A44	NC	B44	NC
A45	NC	B45	NC
A46	NC	B46	NC
A47	NC	B47	NC
A48	NC	B48	NC
A49	NC	B49	NC
A50	NC	B50	NC
A51	Vref	B51	Vref
A52	Gnd	B52	Gnd
A53	SCL	B53	SA0
A54	Vdd	B54	Vdd
A55	SDA	B55	SA1
A56	SVdd	B56	SVdd
A57	SWP	B57	SA2
A58	Vdd	B58	Vdd
A59	RSCK	B59	RCMD
A60	Gnd	B60	Gnd
A61	RDQB7	B61	RDQB8
A62	Gnd	B62	Gnd
A63	RDQB5	B63	RDQB6
A64	Gnd	B64	Gnd
A65	RDQB3	B65	RDQB4
A66	Gnd	B66	Gnd
A67	RDQB1	B67	RDQB2
A68	Gnd	B68	Gnd
A69	RCOL0	B69	RDQB0
A70	Gnd	B70	Gnd
A71	RCOL2	B71	RCOL1
A72	Gnd	B72	Gnd
A73	RCOL4	B73	RCOL3
A74	Gnd	B74	Gnd
A75	RROW1	B75	RROW0
A76	Gnd	B76	Gnd
A77	NC	B77	RROW2
A78	Gnd	B78	Gnd
A79	RCTM	B79	NC
A80	Gnd	B80	Gnd
A81	RCTMN	B81	RCFMN
A82	Gnd	B82	Gnd
A83	RDQA0	B83	RCFM
A84	Gnd	B84	Gnd
A85	RDQA2	B85	RDQA1
A86	Gnd	B86	Gnd
A87	RDQA4	B87	RDQA3
A88	Gnd	B88	Gnd
A89	RDQA6	B89	RDQA5
A90	Gnd	B90	Gnd
A91	RDQA8	B91	RDQA7
A92	Gnd	B92	Gnd

Table 2: Module Connector Pad Description

Signal	Module Connector Pads	I/O	Type	Description
Gnd	A1, A3, A5, A7, A9, A11, A13, A15, A17, A19, A21, A23, A25, A27, A29, A31, A33, A39, A52, A60, A62, A64, A66, A68, A70, A72, A74, A76, A78, A80, A82, A84, A86, A88, A90, A92, B1, B3, B5, B7, B9, B11, B13, B15, B17, B19, B21, B23, B25, B27, B29, B31, B33, B39, B52, B60, B62, B64, B66, B68, B70, B72, B74, B76, B78, B80, B82, B84, B86, B88, B90, B92			Ground reference for RDRAM core and interface. 72 PCB connector pads.
LCFM	B10	**I**	**RSL**	Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.
LCFMN	B12	**I**	**RSL**	Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity.
LCMD	B34	**I**	**V_{CMOS}**	Serial Command used to read from and write to the control registers. Also used for power management.
LCOL4.. LCOL0	A20, B20, A22, B22, A24	**I**	**RSL**	Column bus. 5-bit bus containing control and address information for column accesses.
LCTM	A14	**I**	**RSL**	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.
LCTMN	A12	**I**	**RSL**	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity.
LDQA8.. LDQA0	A2, B2, A4, B4, A6, B6, A8, B8, A10	**I/O**	**RSL**	Data bus A. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. LDQA8 is non-functional on modules with x16 RDRAM devices
LDQB8.. LDQB0	B32, A32, B30, A30, B28, A28, B26, A26, B24	**I/O**	**RSL**	Data bus B. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. LDQB8 is non-functional on modules with x16 RDRAM devices.
LROW2.. LROW0	B16, A18, B18	**I**	**RSL**	Row bus. 3-bit bus containing control and address information for row accesses.
LSCK	A34	**I**	**V_{CMOS}**	Serial Clock input. Clock source used to read from and write to the RDRAM control registers.
NC	A16, B14, A38, B38, A40, B40, A77, B79			These pads are not connected. These 8 connector pads are reserved for future use.
NC	A43, B43, A44, B44, A45, B45, A46, B46, A47, B47, A48, B48, A49, B49, A50, B50			These pads are not connected. These 16 connector pads are reserved for future use. The 168 contact RIMM connector does not connect to these PCB pads
RCFM	B83	**I**	**RSL**	Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.
RCFMN	B81	**I**	**RSL**	Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity.

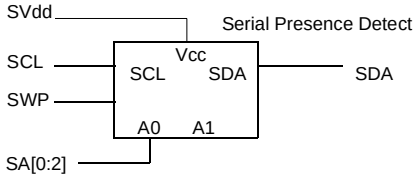
Signal	Module Connector Pads	I/O	Type	Description
RCMD	B59	I	V_{CMOS}	Serial Command Input used to read from and write to the control registers. Also used for power management.
RCOL4.. RCOL0	A73, B73, A71, B71, A69	I	RSL	Column bus. 5-bit bus containing control and address information for column accesses.
RCTM	A79	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.
RCTMN	A81	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity.
RDQA8.. RDQA0	A91, B91, A89, B89, A87, B87, A85, B85, A83	I/O	RSL	Data bus A. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. RDQA8 is non-functional on modules with x16 RDRAM devices.
RDQB8.. RDQB0	B61, A61, B63, A63, B65, A65, B67, A67, B69	I/O	RSL	Data bus B. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. RDQB8 is non-functional on modules with x16 RDRAM devices.
RROW2.. RROW0	B77, A75, B75	I	RSL	Row bus. 3-bit bus containing control and address information for row accesses.
RSCK	A59	I	V_{CMOS}	Serial Clock input. Clock source used to read from and write to the RDRAM control registers.
SA0	B53	I	SV_{DD}	Serial Presence Detect Address 0.
SA1	B55	I	SV_{DD}	Serial Presence Detect Address 1.
SA2	B57	I	SV_{DD}	Serial Presence Detect Address 2.
SCL	A53	I	SV_{DD}	Serial Presence Detect Clock.
SDA	A55	I/O	SV_{DD}	Serial Presence Detect Data (Open Collector I/O).
SIN	B36	I/O	V_{CMOS}	Serial I/O for reading from and writing to the control registers. Attaches to SIO0 of the first RDRAM on the module.
SOUT	A36	I/O	V_{CMOS}	Serial I/O for reading from and writing to the control registers. Attaches to SIO1 of the last RDRAM on the module.
SV_{DD}	A56, B56			SPD Voltage. Used for signals SCL, SDA, SWE, SA0, SA1 and SA2.
SWP	A57	I	SV_{DD}	Serial Presence Detect Write Protect (active high). When low, the SPD can be written as well as read.
V_{CMOS}	A35, B35, A37, B37			CMOS I/O Voltage. Used for signals CMD, SCK, SIN, SOUT.
Vdd	A41, A42, A54, A58, B41, B42, B54, B58			Supply voltage for the RDRAM core and interface logic.
Vref	A51, B51			Logic threshold reference voltage for RSL signals.

RIMM Module Functional Diagram



Module Capacity	N
64MB / 72MB	4
96MB / 108MB	6
128MB / 144MB	8
256MB/288MB	16

Note 1: Rambus Channel signals form a loop through the RIMM module, with the exception of the SIO chain.
Note 2: See Serial Presence Detection Specification for information on the SPD device and its contents.



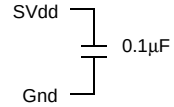


Table 3: Module Connector Pad Description

Signal	Module Connector Pads	I/O	Type	Description
Gnd	A1, A3, A5, A7, A9, A11, A13, A15, A17, A19, A21, A23, A25, A27, A29, A31, A33, A39, A52, A60, A62, A64, A66, A68, A70, A72, A74, A76, A78, A80, A82, A84, A86, A88, A90, A92, B1, B3, B5, B7, B9, B11, B13, B15, B17, B19, B21, B23, B25, B27, B29, B31, B33, B39, B52, B60, B62, B64, B66, B68, B70, B72, B74, B76, B78, B80, B82, B84, B86, B88, B90, B92			Ground reference for RDRAM core and interface. 72 PCB connector pads.
LCFM	B10	**I**	**RSL**	Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.
LCFMN	B12	**I**	**RSL**	Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity.
LCMD	B34	**I**	**V_{CMOS}**	Serial Command used to read from and write to the control registers. Also used for power management.
LCOL4.. LCOL0	A20, B20, A22, B22, A24	**I**	**RSL**	Column bus. 5-bit bus containing control and address information for column accesses.
LCTM	A14	**I**	**RSL**	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.
LCTMN	A12	**I**	**RSL**	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity.
LDQA8.. LDQA0	A2, B2, A4, B4, A6, B6, A8, B8, A10	**I/O**	**RSL**	Data bus A. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. LDQA8 is non-functional on modules with x16 RDRAM devices
LDQB8.. LDQB0	B32, A32, B30, A30, B28, A28, B26, A26, B24	**I/O**	**RSL**	Data bus B. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. LDQB8 is non-functional on modules with x16 RDRAM devices.
LROW2.. LROW0	B16, A18, B18	**I**	**RSL**	Row bus. 3-bit bus containing control and address information for row accesses.
LSCK	A34	**I**	**V_{CMOS}**	Serial Clock input. Clock source used to read from and write to the RDRAM control registers.
NC	A16, B14, A38, B38, A40, B40, A77, B79			These pads are not connected. These 8 connector pads are reserved for future use.
NC	A43, B43, A44, B44, A45, B45, A46, B46, A47, B47, A48, B48, A49, B49, A50, B50			These pads are not connected. These 16 connector pads are reserved for future use. The 168 contact RIMM connector does not connect to these PCB pads
RCFM	B83	**I**	**RSL**	Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.
RCFMN	B81	**I**	**RSL**	Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity.

Signal	Module Connector Pads	I/O	Type	Description
RCMD	B59	I	V_{CMOS}	Serial Command Input used to read from and write to the control registers. Also used for power management.
RCOL4.. RCOL0	A73, B73, A71, B71, A69	I	RSL	Column bus. 5-bit bus containing control and address information for column accesses.
RCTM	A79	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.
RCTMN	A81	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity.
RDQA8.. RDQA0	A91, B91, A89, B89, A87, B87, A85, B85, A83	I/O	RSL	Data bus A. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. RDQA8 is non-functional on modules with x16 RDRAM devices.
RDQB8.. RDQB0	B61, A61, B63, A63, B65, A65, B67, A67, B69	I/O	RSL	Data bus B. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. RDQB8 is non-functional on modules with x16 RDRAM devices.
RROW2.. RROW0	B77, A75, B75	I	RSL	Row bus. 3-bit bus containing control and address information for row accesses.
RSCK	A59	I	V_{CMOS}	Serial Clock input. Clock source used to read from and write to the RDRAM control registers.
SA0	B53	I	SV_{DD}	Serial Presence Detect Address 0.
SA1	B55	I	SV_{DD}	Serial Presence Detect Address 1.
SA2	B57	I	SV_{DD}	Serial Presence Detect Address 2.
SCL	A53	I	SV_{DD}	Serial Presence Detect Clock.
SDA	A55	I/O	SV_{DD}	Serial Presence Detect Data (Open Collector I/O).
SIN	B36	I/O	V_{CMOS}	Serial I/O for reading from and writing to the control registers. Attaches to SIO0 of the first RDRAM on the module.
SOUT	A36	I/O	V_{CMOS}	Serial I/O for reading from and writing to the control registers. Attaches to SIO1 of the last RDRAM on the module.
SV_{DD}	A56, B56			SPD Voltage. Used for signals SCL, SDA, SWE, SA0, SA1 and SA2.
SWP	A57	I	SV_{DD}	Serial Presence Detect Write Protect (active high). When low, the SPD can be written as well as read.
V_{CMOS}	A35, B35, A37, B37			CMOS I/O Voltage. Used for signals CMD, SCK, SIN, SOUT.
Vdd	A41, A42, A54, A58, B41, B42, B54, B58			Supply voltage for the RDRAM core and interface logic.
Vref	A51, B51			Logic threshold reference voltage for RSL signals.

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
$V_{I,ABS}$	Voltage applied to any RSL or CMOS signal pad with respect to Gnd	- 0.3	V_{DD} + 0.3	V
$V_{DD,ABS}$	Voltage on VDD with respect to Gnd	- 0.5	V_{DD} + 1.0	V
T_{STORE}	Storage temperature	- 50	100	°C

DC Recommended Electrical Conditions

Symbol	Parameter and Conditions	Min	Max	Unit
V_{DD}	Supply voltage	2.50 - 0.13	2.50 + 0.13	**V**
V_{CMOS}	CMOS I/O power supply at pad for 2.5V controllers: CMOS I/O power supply at pad for 1.8V controllers:	2.5 - 0.13 1.8 - 0.1	2.5 + 0.25 1.8 + 0.2	**V** **V**
V_{REF}	Reference voltage	1.4 - 0.2	1.4 + 0.2	**V**
V_{IL}	RSL input low voltage	V_{REF} - 0.5	V_{REF} - 0.2	**V**
V_{IH}	RSL input high voltage	V_{REF} + 0.2	V_{REF} + 0.5	**V**
$V_{IL,CMOS}$	CMOS input low voltage	- 0.3	$0.5V_{CMOS}$ - 0.25	**V**
$V_{IH,CMOS}$	CMOS input high voltage	$0.5V_{CMOS}$ + 0.25	V_{CMOS} + 0.7	**V**
$V_{OL,CMOS}$	CMOS output low voltage @ $I_{OL,CMOS}$ = 1mA		0.3	**V**
$V_{OH,CMOS}$	CMOS output high voltage @ $I_{OH,CMOS}$ = -0.25mA	V_{CMOS} - 0.3		**V**
I_{REF}	V_{REF} current @ $V_{REF,MAX}$	-10 x no. RDRAMs[a]	10 x no. RDRAMs[a]	**µA**
$I_{SCK,CMD}$	CMOS input leakage current @ ($0 \le V_{CMOS} \le V_{DD}$)	-10 x no. RDRAMs[a]	10 x no. RDRAMs[a]	**µA**
$I_{SIN,SOUT}$	CMOS input leakage current @ ($0 \le V_{CMOS} \le V_{DD}$)	-10.0	10.0	**µA**

a. The table below shows the number of 128Mb or 144Mb RDRAM devices contained in a RIMM module of listed storage capacity.

RIMM Module Capacity:	64/72MB	96/108MB	128/144MB	256/288MB
Number of 128Mb or 144Mb RDRAM devices:	4	6	8	16

AC Electrical Specifications

Symbol	Parameter and Conditions	Min	Typ	Max	Unit
Z	Module Impedance	25.2	28	30.8	Ω
T_{PD}	Propagation Delay, all RSL signals	-		See Table[a]	ns
ΔT_{PD}	Propagation delay variation of RSL signals with respect to an average clock delay [b]	-10		10	ps
$\Delta T_{PD\text{-}CMOS}$	Propagation delay variation of SCK and CMD signals with respect to an average clock delay [b]	-100		100	ps
V_α / V_{IN}	Attenuation Limit			See Table[a]	%
V_{XF} / V_{IN}	Forward crosstalk coefficient (300ps input rise time @ 20%-80%)			See Table[a]	%
V_{XB} / V_{IN}	Backward crosstalk coefficient (300ps input rise time @ 20%-80%)			See Table[a]	%

a. Table below lists parameters and specifications for different storage capacity RIMM modules that use 128Mb or 144Mb RDRAM devices.
b. Average clock delay is defined as the average delay from finger to finger of all RSL clock nets (CTM, CTMN, CFM, and CFMN).

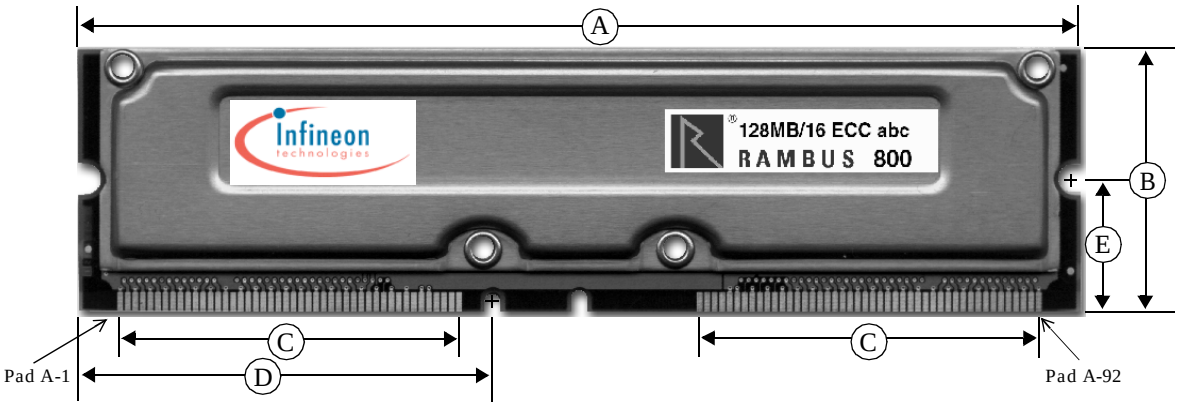
AC Electrical Specifications for RIMM Modules

Symbol	RIMM Module Capacity: No. of 128/144Mb RDRAMs:	64/72MB 4	96/108MB 6	128/144MB 8	256/288MB 16	Unit
	Parameter and Condition for -800 to-600 RIMM modules	**Max**	**Max**	**Max**	**Max**	
T_{PD}	Propagation Delay, all RSL signals -800	1.25	TBD	1.50	2.06	ns
	Propagation Delay, all RSL signals -600	1.25	TBD	1.60	2.10	ns
V_α / V_{IN}	Attenuation Limit -800	12	TBD	16	25	%
	Attenuation Limit -600	8	TBD	10	21	%
V_{XF} / V_{IN}	Forward crosstalk coefficient (300ps input rise time @ 20%-80%) -800	2	TBD	4	8	%
	Forward crosstalk coefficient (300ps input rise time @ 20%-80%) -600	2	TBD	4	8	%
V_{XB} / V_{IN}	Backward crosstalk coefficient (300ps input rise time @ 20%-80%) -800	1.5	TBD	2.0	2.5	%
	Backward crosstalk coefficient (300ps input rise time @ 20%-80%) -600	1.5	TBD	2.0	2.5	%
R_{DC}	DC Resistance Limit	0.6	TBD	0.8	1.2	Ω
	DC Resistance Limit	0.6	TBD	10.8	1.2	Ω

RIMM Module Current Profile

I_{DD}	RIMM Module Capacity: No. of 128/144Mb RDRAMs:	64/72MB 4	96/108MB 6	128/144MB 8	256/288MB 16	Unit
	RIMM module power conditions[a]	**Max**	**Max**	**Max**	**Max**	
I_{DD1}	One RDRAM in Read, balance in NAP mode	587	TBD	604	637	mA
I_{DD2}	One RDRAM in Read, balance in Standby mode, no commands	878	TBD	1282	2090	mA
I_{DD3}	One RDRAM in Read, balance in Active mode, no commands	1019	TBD	1611	2795	mA

a. Specifications in this table are maximum guidelines. Actual power will depend on individual memory controller and usage patterns.

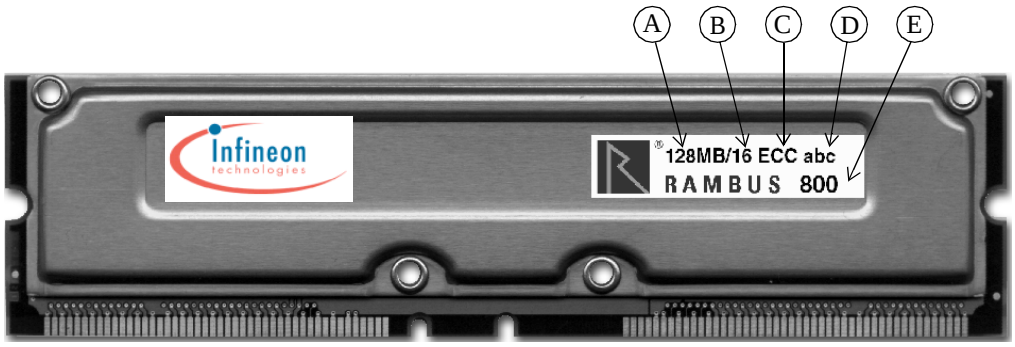


Dimension	Description	Min	Nom	Max	Unit
A	PCB length	133.20 5.244	133.35 5.250	133.50 5.256	mm in
B	PCB height			34.93 1.375	mm in
C	Center-center pad width from pad A1 to A46, A47 to A92, B1 to B46 or B47 to B92			45.00 1.770	mm in
D	Spacing from PCB left edge to connector key notch			55.25 2.175	mm in
E	Spacing from contact pad PCB edge to side edge retainer notch			17.78 0.700	mm in
F	PCB thickness	1.17 0.046	1.27 0.050	1.37 0.054	mm in
G	Heat spreader thickness from PCB surface (one side) to heat spreader top surface			3.00 0.118	mm in

Figure 1: RIMM Module PCB Physical Description

Standard RIMM Module Marking

The RIMM modules available from RIMM module manufacturers will be marked per Figure 2 below. This industry standard marking will help OEMs and users identify the Rambus RIMM modules when used in specific system applications. This will assist OEMs or users to specify and correctly verify if the correct RIMM modules are installed in their systems. In the diagram, a label is shown attached to the right-center side of the RIMM module's heat spreader. RIMM modules without heat spreaders will have a similar label attached to the lower right side of the RIMM module PCB. This label is in addition to any vendor specific label or marking. Information contained in this area is specific for the RIMM module and provides RDRAM information without requiring removal of the RIMM module's heat spreader.



	Label Field	Description	Marked Text	Unit
A	Module Memory Capacity	Number of 8-bit or 9-bit MBytes of RDRAM storage in RIMM module	128MB, 96MB, 64MB, 48MB, 32MB	MBytes
B	Number of RDRAMs	Number of RDRAM devices contained in the RIMM module	/16, /12, /8, /6, /4	RDRAM devices
C	ECC Support	Indicates whether the RIMM module supports 8-bit (no ECC) or 9-bit (ECC) Bytes	blank = 8-bit Byte ECC = 9-bit Byte	
D	Reserved	Reserved for future use	blank	
E	Memory Speed	Data transfer speed for RDRAM RIMM module	800, 711, 600	MHz

Figure 2: Standard RIMM Module Marking