Integrated Device Technology, Inc.

IDT79R4000 FLEXI-CACHE™ DEVELOPMENT TOOL

PRELIMINARY
IDT7MP6048
IDT7MP6068

FEATURES

- Hardware Development Tool for implementing various configurations of the secondary cache requirement for the IDT79R4000 CPU
- Configurable in various cache sizes, number of words per line size, and split vs. unified cache operation
- Move from prototype/development to production with no redesign by using pin-compatible "production grade" IDT79R4000 secondary cache modules
- Four identical 80-lead gold-plated SIMMs (Single In-Line Memory Modules) support each IDT79R4000 CPU
- Surface mounted plastic components on a multilayer epoxy laminate (FR-4) substrate
- Multiple ground pins and decoupling capacitors for maximum noise immunity
- TTL-compatible I/Os
- Single 5V (±10%) power supply

DESCRIPTION

The IDT7MP6048/7MP6068 is a Hardware Development Tool used for implementing various configurations of the secondary cache requirement for the IDT79R4000 CPU. By changing jumpers on the modules, the designer can easily change certain characteristics (cache size, number of words per line, and split vs. unified operation) of the secondary cache in the lab. By running benchmarks on the actual system using these various cache configurations, the secondary cache which best optimizes system performance can be determined. This development tool gives you cache performance benchmarks which are superior to benchmarks derived via simulation.

Move from development to production without changing the secondary cache footprint by choosing pin-compatible "production grade" IDT79R4000 secondary cache modules. These high-performance, high-density IDT modules are optimized to meet the customers' exact cache requirements required for volume production of the system (please consult the factory for more details).

The IDT7MP6048 is a 1 MB secondary cache module block (four identical modules builds a complete cache to support each IDT79R4000 CPU) constructed on a multilayer, epoxy laminate substrate (FR-4) using 11 64K x 4 Static RAMs and FBT logic drivers while the IDT7MP6068 is a 4MB secondary cache module block using eleven 256K x 4 Static RAMs and FBT logic drivers. The FBT drivers have BiCMOS I/Os and internal 25Ω series output resistors resulting in the fastest propagation times with minimal overshoots and ringing. Mul-

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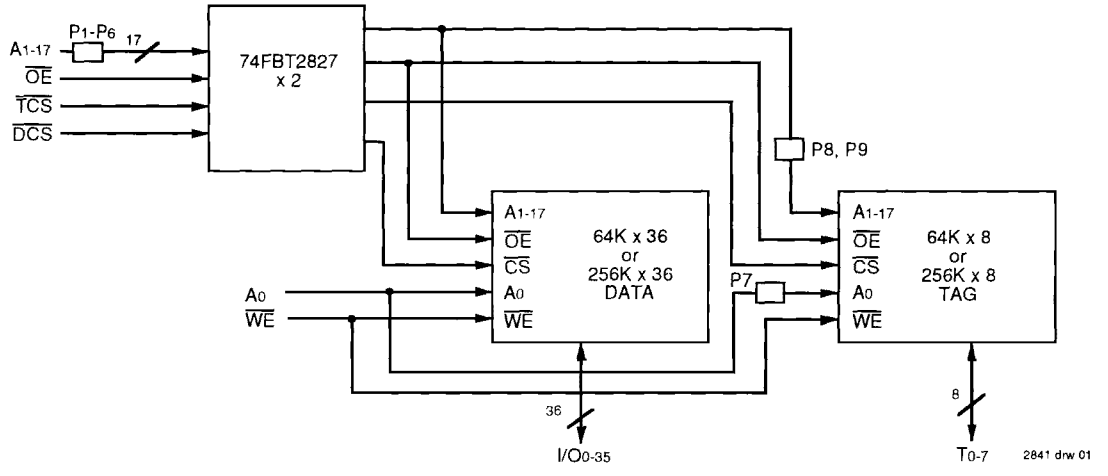
FUNCTIONAL BLOCK DIAGRAM[1]



NOTE:
1. The Data and Tag sizes shown on the block diagram are only for the case when the jumpers are in the default positions for the respective modules. These sizes will change according to the jumper connections (see Jumper Connections on page 2).

tiple GND pins and on-board decoupling capacitors provide maximum noise immunity for this performance critical part of the system. All inputs and outputs of the modules are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refresh for operation of the module.

CACHE CONFIGURATIONS[1]

Memory Size
4MB (7MP6068 default)
2MB
1MB (7MP6048 default)
512KB
256KB
128KB

Words per line
4 (default)
8
16
32

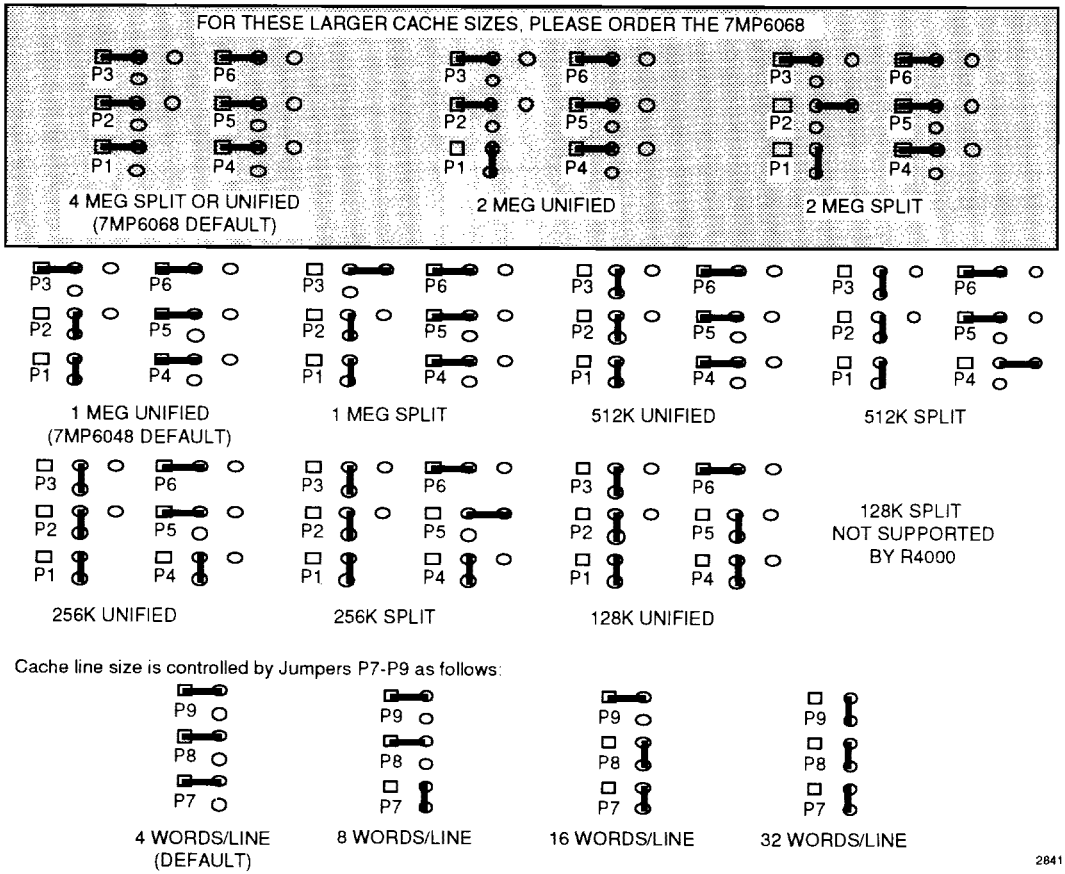
Cache Operation
unified cache (default)
split cache

NOTE: 2841 tbl 01

1. Please refer to the Jumper Connections for instructions on how to implement the Cache Configurations shown above.

JUMPER CONNECTIONS

Cache depth and Split vs. Unified Operation are controlled by Jumpers P1-P6 as follows:



Cache line size is controlled by Jumpers P7-P9 as follows:

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PIN CONFIGURATION[1]

V_{CC}	2	1	GND
I/O_1	4	3	I/O_0
I/O_3	6	5	I/O_2
I/O_5	8	7	I/O_4
GND	10	9	I/O_6
I/O_8	12	11	I/O_7
I/O_{10}	14	13	I/O_9
I/O_{12}	16	15	I/O_{11}
I/O_{14}	18	17	I/O_{13}
I/O_{15}	20	19	GND
I/O_{17}	22	21	I/O_{16}
I/O_{19}	24	23	I/O_{18}
I/O_{21}	26	25	I/O_{20}
GND	28	27	I/O_{22}
I/O_{23}	30	29	V_{CC}
I/O_{25}	32	31	I/O_{24}
I/O_{27}	34	33	I/O_{26}
I/O_{29}	36	35	I/O_{28}
I/O_{30}	38	37	GND
I/O_{32}	40	39	I/O_{31}
I/O_{34}	42	41	I/O_{33}
GND	44	43	I/O_{35}
A_0	46	45	$\overline{WE}$
A_2	48	47	A_1
A_4	50	49	A_3
A_6	52	51	A_5
V_{CC}	54	53	GND
$\overline{OE}$	56	55	$\overline{DCS}$
A_8	58	57	A_7
A_{10}	60	59	A_9
GND	62	61	A_{11}
A_{13}	64	63	A_{12}
A_{15}	66	65	A_{14}
A_{17}	68	67	A_{16}
T_0	70	69	$\overline{TCS}$
T_1	72	71	GND
T_3	74	73	T_2
T_5	76	75	T_4
T_7	78	77	T_6
GND	80	79	V_{CC}

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SIMM
TOP VIEW

NOTE:
1. For proper operation of the module, please refer to the Jumper Connections for proper connections of the module pins.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5V ± 10%

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PIN NAMES

I/O_{0-35}	Data Inputs/Outputs
T_{0-7}	Tag Inputs/Outputs
A_{0-17}	Address Inputs
$\overline{DCS}$	Data Chip Select
$\overline{TCS}$	Tag Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
GND	Ground

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CAPACITANCE

Symbol	Parameter[1]	Conditions	Max.	Unit
$C_{IN(D)}$	Input Capacitance (Data)	V_{IN} = 0V	10	pF
$C_{IN(A)}$	Input Capacitance (A_{1-15}, $\overline{OE}$, $\overline{TCS}$, $\overline{DCS}$)	V_{IN} = 0V	10	pF
$C_{IN(B)}$	Input Capacitance (A_0, $\overline{WE}$)	V_{IN} = 0V	100	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	10	pF

NOTE: 2841 tbl 04
1. This parameter is guaranteed by design, but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE: 2841 tbl 05
1. V_{IL} = –1.5V for pulse width less than 10ns.

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating[1]	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 2841 tbl 06
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI1}\|$	Input Leakage (except A_0, $\overline{WE}$)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LI2}\|$	Input Leakage (A_0, $\overline{WE}$)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	110	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
I_{CC}	Operating Current	$\overline{CS}$ = V_{IL}; V_{CC} = Max., Outputs Open	—	2200	mA
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4mA	2.4	—	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V

2841 tbl 07

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 – 4

2841 tbl 08

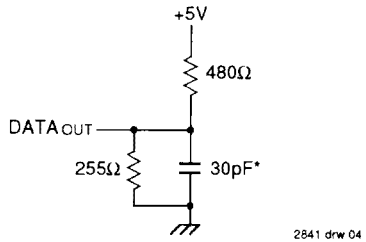


Figure 1. Output Load

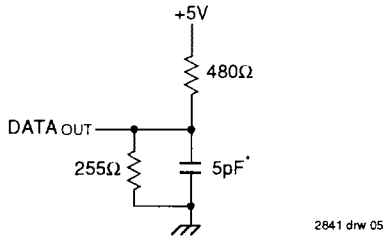


Figure 2. Output Load (for t_{OLZ} and t_{OHZ})

* Including scope and jig.

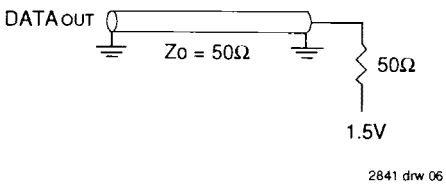


Figure 3. Alternate Output Load

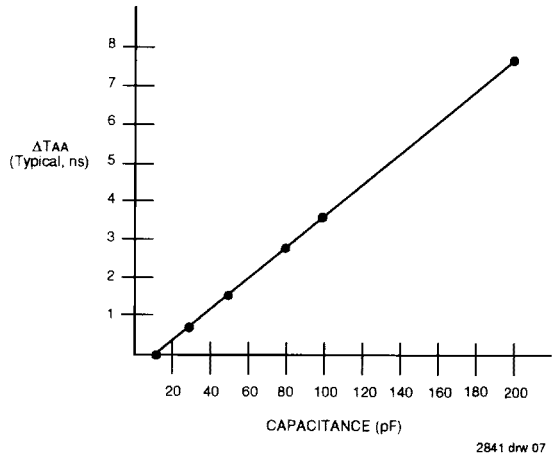


Figure 4. Alternate Lumped Capacitive Load, Typical Derating

AC ELECTRICAL CHARACTERISTICS

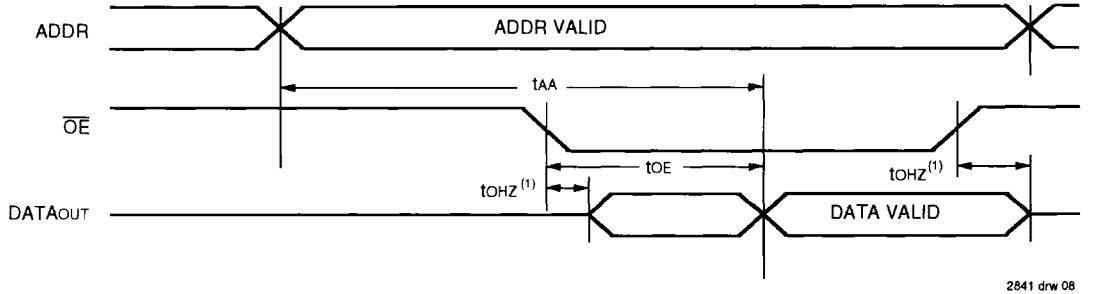
(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	7MP6048/6068SxxM												Unit
		-12		-15		-17		-20		-25		-30		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE														
t_{AA}	Address Access Time	—	12	—	15	—	17	—	20	—	25	—	30	ns
t_{A0A}	A_0 Access Time	—	10	—	12	—	14	—	16	—	21	—	26	ns
t_{OE}	Output Enable to Output Valid	—	12	—	15	—	17	—	20	—	25	—	30	ns
t_{OHZ}[1]	Output Disable to Output in High-Z	—	10	—	12	—	13	—	15	—	17	—	20	ns
t_{OLZ}[1]	Output Enable to Output in Low-Z	2	—	2	—	2	—	2	—	2	—	2	—	ns
WRITE CYCLE														
t_{AW}	Address Valid to End of Write	12	—	15	—	17	—	20	—	25	—	30	—	ns
t_{A0W}	A_0 Valid to End of Write	10	—	12	—	14	—	16	—	21	—	26	—	ns
t_{WP}	Write Pulse Width	7	—	10	—	12	—	15	—	20	—	25	—	ns
t_{DW}	Data Valid to End of Write	7	—	10	—	12	—	15	—	20	—	25	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	ns

NOTE:
1. This parameter is guaranteed by design but not tested.

2833 tbl 08

TIMING WAVEFORM OF READ CYCLE[1]



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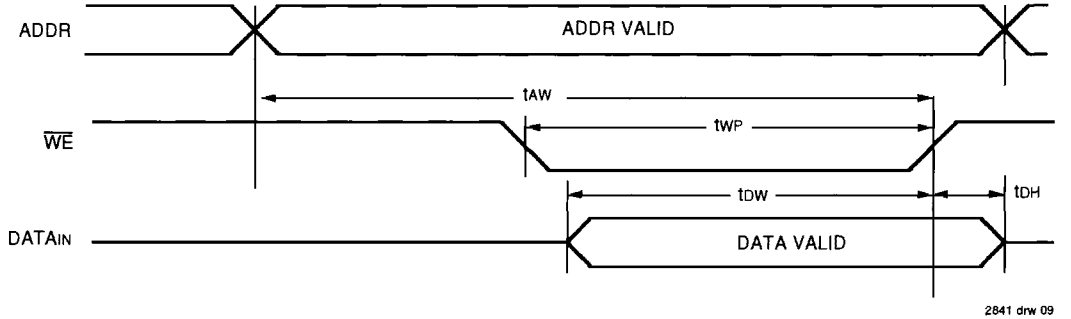
NOTE:
1. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE



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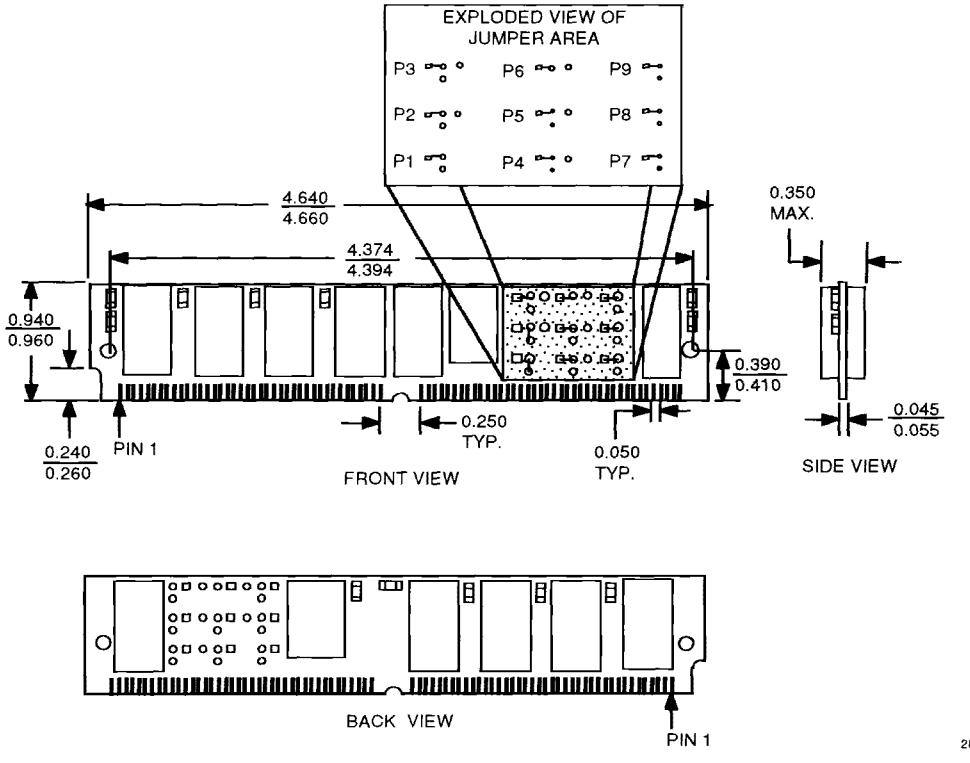
PACKAGE DIMENSIONS



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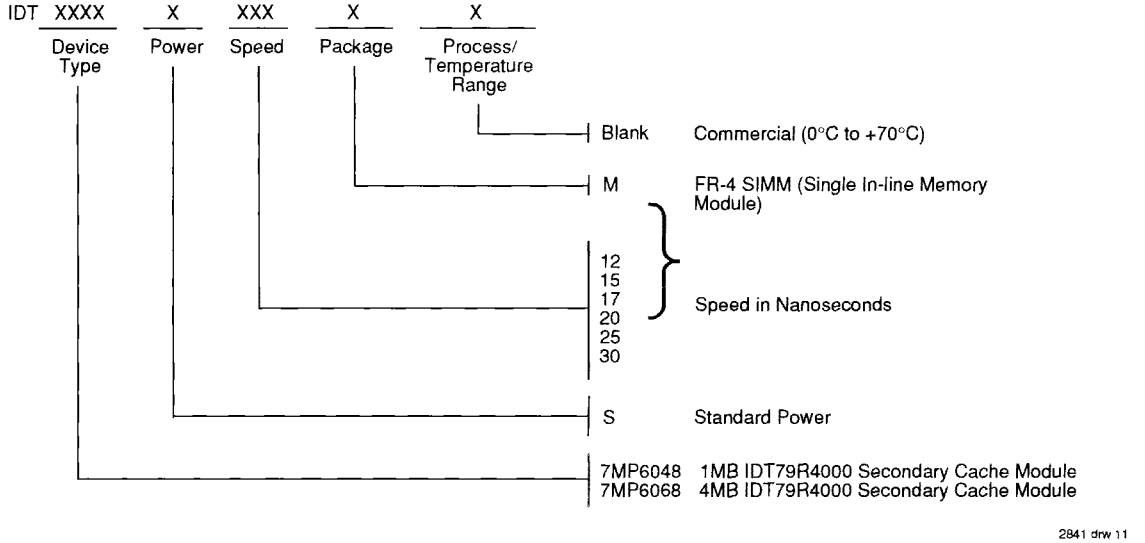
ORDERING INFORMATION



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