HY628100

128K×8-Bit CMOS SRAM

M271200A-MAY92

DESCRIPTION

The HY628100 is a high speed low power, 131,072 words by 8-bit CMOS static RAM fabricated using HYUNDAI's high performance twin tub CMOS process. This high reliability process coupled with innovative circuit design techniques, yields maximum access time of 70ns.

The HY628100 has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 2.0 volt.

Using CMOS technology, supply voltages from 2.0 to 5.5 volt have little effect on supply current in data retention mode. Reducing the supply voltage to minimize current drain is unnecessary with the HY628100 family.

FEATURES

- **High speed − 70/85/100/120 ns (max.)**
- **Low power consumption**
  - **250mW typical operating**
  - **10μW typical standby (L/LL-version)**
- **Battery back up (L/LL-version)**
  - **2 volt data retention**
- **Fully static operation**
  - **No clock or refresh required**
- **All inputs and outputs directly TTL compatible**
- **Tri-state output**
- **High reliability 32 pin 600 mil P-DIP and 525 mil SOP**

		HY628100-70	HY628100-85	HY628100-10	HY628100-12
Maximum Access Time (ns)		70	85	100	120
Maximum Average Operating Current (mA)		70	70	70	70
Maximum Standby Current (mA)		2.0	2.0	2.0	2.0
	L	0.1	0.1	0.1	0.1
	LL	0.05	0.05	0.05	0.05

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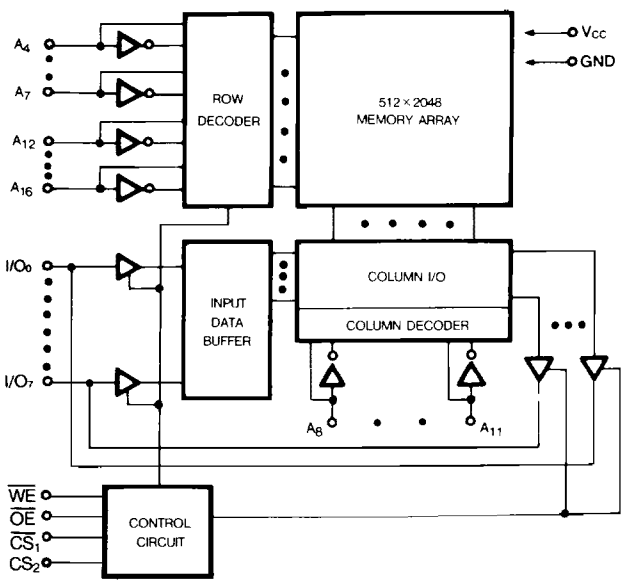
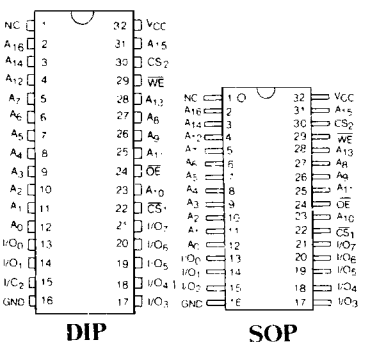
BLOCK DIAGRAM



PIN CONNECTIONS



DIP SOP

PIN NAMES

A_0-A_{16}	ADDRESS INPUT
I/O_0-I/O_7	DATA INPUT/OUTPUT
$\overline{CS}_1$	CHIP SELECT ONE
CS_2	CHIP SELECT TWO
$\overline{WE}$	WRITE ENABLE
$\overline{OE}$	OUTPUT ENABLE
V_{CC}	POWER
GND	GROUND

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}, V_{IN}, $V_{I/O}$	Power Supply, Input, Input/Output Voltage	−0.5[2] to 7.0	V
T_{BIAS}	Temperature Under Bias	−10 to 125	℃
T_{STG}	Storage Temperature	−65 to 150	℃
P_D	Power Dissipation	1.0	W
I_{OUT}	Data Output Current	50	mA

NOTES :
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating condition for extended may affect reliability.
2. −3.5V for 20ns pulse.

RECOMMENDED DC OPERATING CONDITIONS
(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	3.5	6.0	V
V_{IL}	Input Low Voltage	−0.5[1]	−	0.8	V

NOTE :
1. −3.5V for 20ns pulse

TRUTH TABLE

MODE	$\overline{CS_1}$	CS_2	$\overline{WE}$	$\overline{OE}$	I/O OPERATION
Standby	H	X	X	X	High-Z
	X	L	X	X	High-Z
Output Disabled	L	H	H	H	High-Z
Read	L	H	H	L	D_{OUT}
Write	L	H	L	X	D_{IN}

NOTE :
1. X : H or L

DC CHARACTERISTICS

(V_{CC}=5V± 10%, T_A=0°C to 70°C)

SYMBOL	PARAMETER	TEST CONDITIONS		HY628100 MIN.	HY628100 TYP.(1)	HY628100 MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{IN}=GND to V_{CC}		–	–	1	μA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=GND to V_{CC}		–	–	1	μA
I_{CC}	Operating Power Supply Current	$\overline{CS_1}$=V_{IL}, CS_2=V_{IH}, V_{IN}=V_{IH} or V_{IL}, $I_{I/O}$ =0mA		–	–	50	mA
I_{CC1}	Average Operating Current	Min cycle, Duty=100% $\overline{CS_1}$=V_{IL}, CS_2=V_{IH} V_{IN}=V_{IH} or V_{IL}, $I_{I/O}$ =0mA		–	50	70	mA
I_{CC2}		Cycle Time=1μs, Duty=100% $\overline{CS_1}$ ≤ 0.2V, CS_2 ≥ V_{CC}−0.2V V_{IN} ≤ 0.2V or ≥ V_{CC}−0.2V, $I_{I/O}$ =0mA		–	–	40	mA
I_{SB}	Standby Power Supply Current	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL}		–	–	3	mA
I_{SB1}		$\overline{CS_1}$ ≥ V_{CC}−0.2V, CS_2 ≤ 0.2V, V_{IN} ≤ 0.2V or ≥ V_{CC}−0.2V		–	–	2	mA
			L	–	2	100	μA
			LL	–	2	50	μA
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH}=−1.0mA		2.4	–	–	V

NOTE :
1. V_{CC}=5V, T_A=25°C

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AC CHARACTERISTICS

(V_{CC}=5V± 10%, T_A=0°C to 70°C)

READ CYCLE

SYMBOL	PARAMETER	HY628100-70 MIN.	HY628100-70 MAX.	HY628100-85 MIN.	HY628100-85 MAX.	HY628100-10 MIN.	HY628100-10 MAX.	HY628100-12 MIN.	HY628100-12 MAX.	UNIT
t_{RC}	Read Cycle Time	70	–	85	–	100	–	120	–	ns
t_{AA}	Address Access Time	–	70	–	85	–	100	–	120	ns
t_{ACS}	Chip Select Access Time	–	70	–	85	–	100	–	120	ns
t_{CLZ}	Chip Selection to Output in Low-Z	10	–	10	–	10	–	10	–	ns
t_{OE}	Output Enable to Output Valid	–	35	–	45	–	50	–	60	ns
t_{OLZ}	Output Enable to Output in Low-Z	5	–	5	–	5	–	5	–	ns
t_{CHZ}	Chip Deselection to Output in High-Z	–	25	–	30	–	35	–	40	ns
t_{OHZ}	Output Disable to Output in High-Z	–	25	–	30	–	35	–	40	ns
t_{OH}	Output Hold from Address Change	10	–	10	–	10	–	10	–	ns

WRITE CYCLE

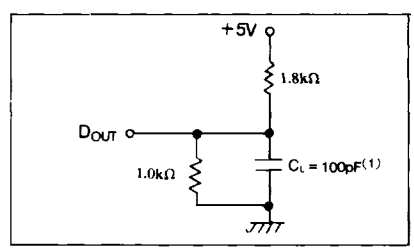
SYMBOL	PARAMETER	HY628100-70		HY628100-85		HY628100-10		HY628100-12		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	70	–	85	–	100	–	120	–	ns
t_{CW}	Chip Selection to End of Write	60	–	75	–	90	–	100	–	ns
t_{AW}	Address Valid to End of Write	60	–	75	–	90	–	100	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	55	–	65	–	75	–	85	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	ns
t_{OHZ}	Output Disable to Output in High-Z	–	30	–	30	–	35	–	40	ns
t_{WHZ}	Write to Output in High-Z	–	25	–	30	–	30	–	30	ns
t_{DW}	Data to Write Time Overlap	30	–	35	–	40	–	50	–	ns
t_{DH}	Data Hold from Write Time	0	–	0	–	0	–	0	–	ns
t_{OW}	Output Active from End of Write	5	–	5	–	5	–	5	–	ns

AC TEST CONDITIONS

(T_A=0°C to 70°C)

Input Pulse Level	0.8V to 2.4V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Level	1.5V

OUTPUT LOAD



NOTE :
1. Including scope and the Jig.

CAPACITANCE(1)

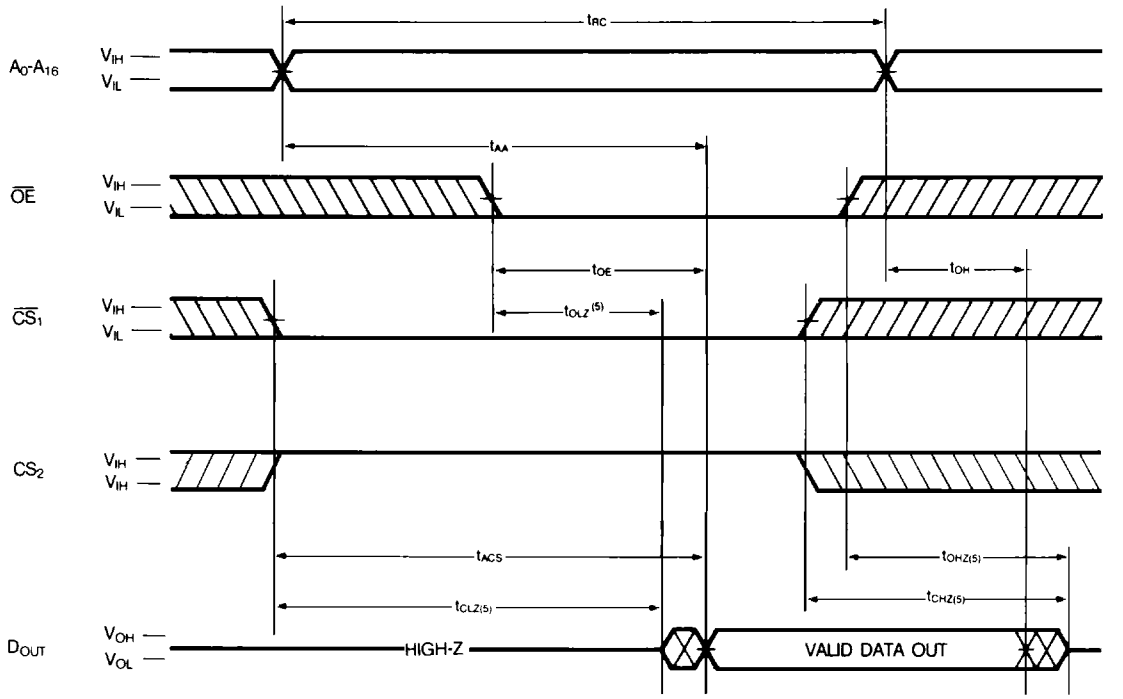
(T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	8	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$=0V	10	pF

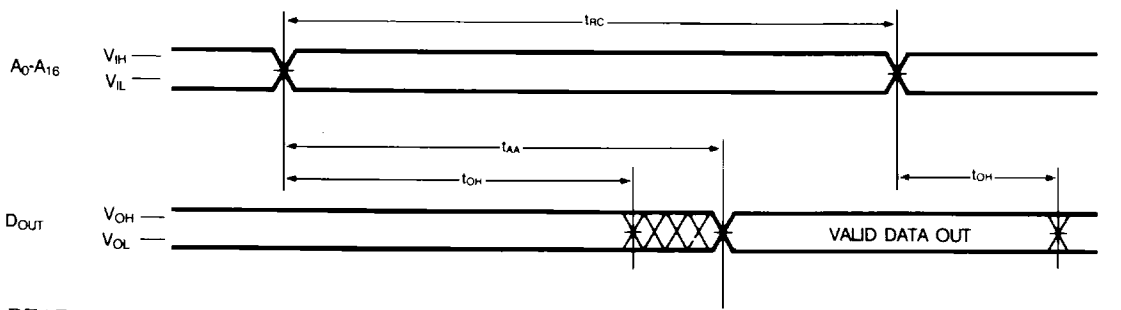
NOTE :
1. This parameter is sampled and not 100% tested.

TIMING DIAGRAMS

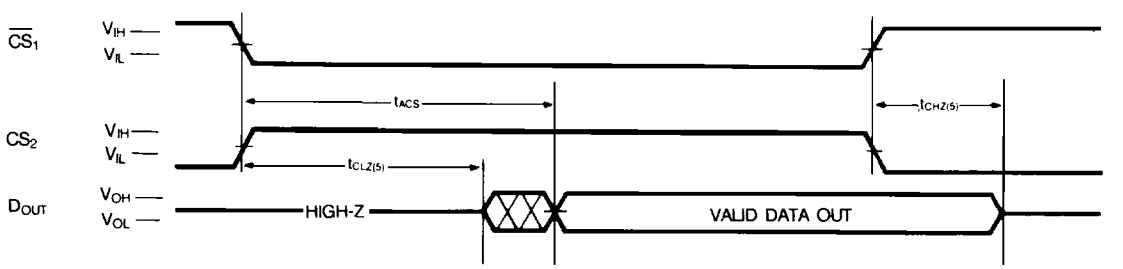
READ CYCLE 1[1]



READ CYCLE 2[1, 2, 4]



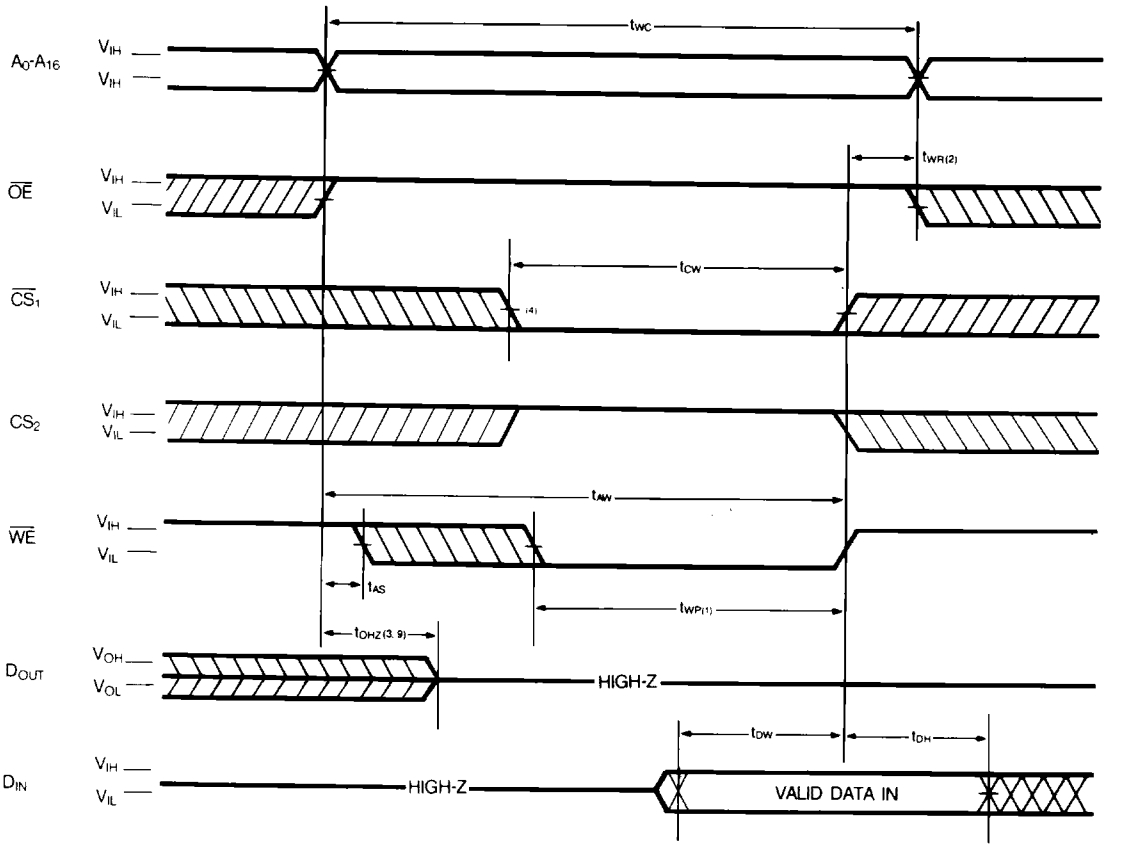
READ CYCLE 3[1, 3, 4]



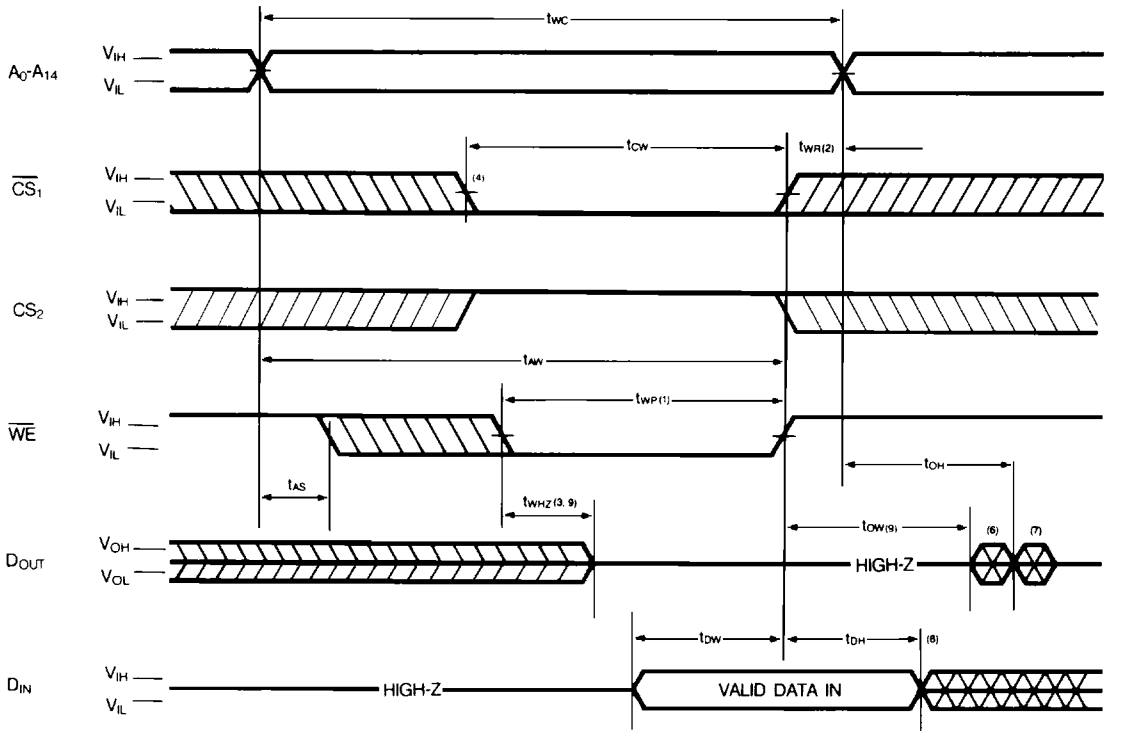
NOTES :

1. $\overline{WE}$ **is high for Read Cycle.**
2. Device is continuously selected, $\overline{CS_1}=V_{IL}$, $CS_2=V_{IH}$
3. Addresses are valid prior to or coincident with $\overline{CS_1}$ transition low, and CS_2 transition high.
4. $\overline{OE}=V_{IL}$
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

WRITE CYCLE 1



WRITE CYCLE 2[5]



NOTES :

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS_1}$, high CS_2 and low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS_1}$ or $\overline{WE}$ going high or CS_2 going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS_1}$ low transition and the CS_2 high transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
5. $\overline{OE}$ is continuously low ($\overline{OE}=V_{IL}$) for write cycle 2.
6. D_{OUT} is the same phase of write data of this write cycle.
7. D_{OUT} is the read data of next address.
8. If $\overline{CS_1}$ is low and CS_2 is high during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

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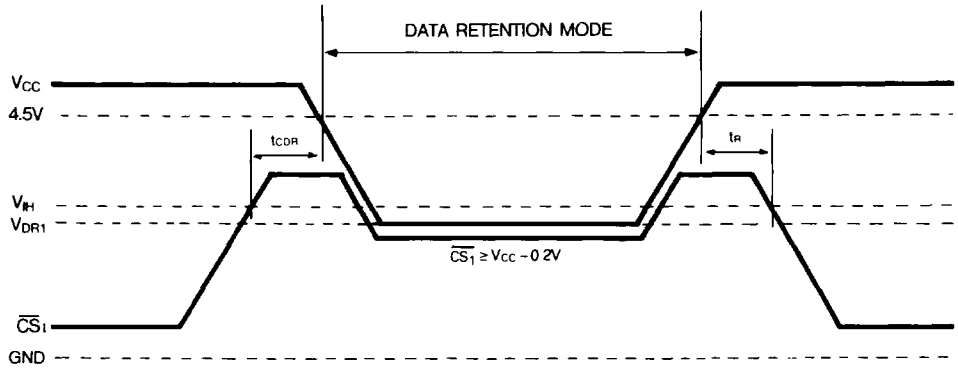
DATA RETENTION CHARACTERISTICS[1]

(V_A=0°C to 70°C)

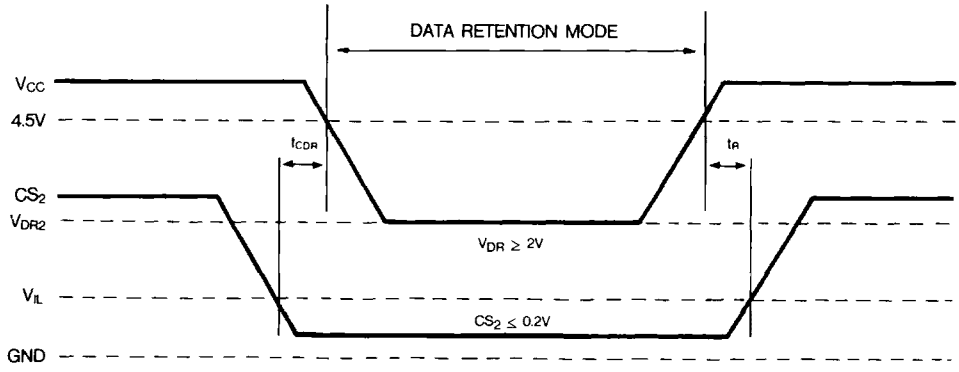
SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.[2]	MAX.	UNIT
V_{DR}	Data Retention Supply Voltage	V_{IN}=0 to V_{CC}, $\overline{CS_1} \geq V_{CC}-0.2V$, $CS_2 \geq V_{CC}-0.2V$ or $0V \leq CS_2 \leq 0.2V$		2.0	–	–	V
I_{CCDR}	Data Retention Current	V_{CC}=3.0V, V_{IN}=0 to V_{CC}, $\overline{CS_1} \geq V_{CC}-0.2V$, $CS_2 \geq V_{CC}-0.2V$ or $0V \leq CS_2 \leq 0.2V$	L	–	2	50	μA
			LL	–	2	30	μA
t_{CDR}	Chip Deselect to Data Retention Time	See Data Retention Timing Diagram		0	–	–	ns
t_R	Operating Recovery Time			t_{RC}[3]	–	–	ns

NOTES :
1. These characteristics are guaranteed for L and LL-version.
2. T_A=25°C
3. t_{RC}=Read Cycle Time

DATA RETENTION TIMING DIAGRAM 1 ($\overline{CS_1}$ Controlled)



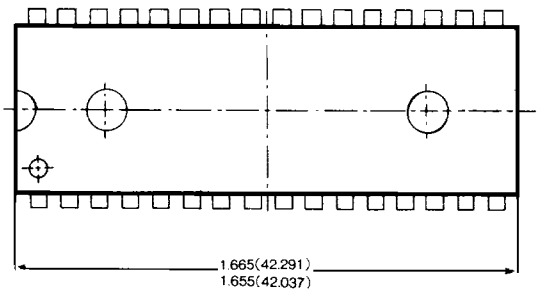
DATA RETENTION TIMING DIAGRAM 2 (CS_2 Controlled)

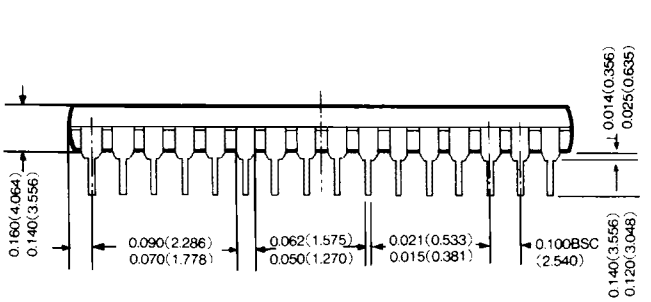


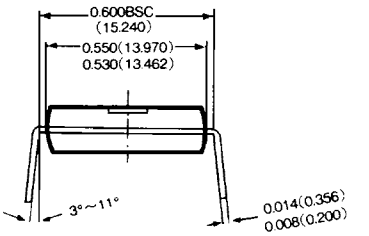
PACKAGE INFORMATION

- 32 PIN PLASTIC DUAL IN LINE PACKAGE−600 MIL

UNIT : INCH(mm) MAX/MIN







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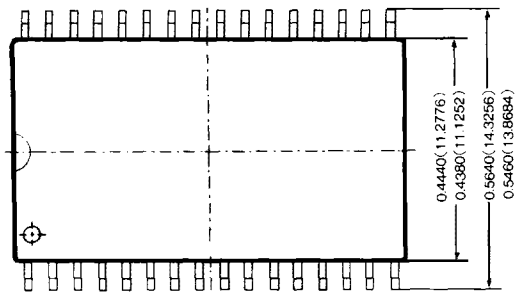
• 32 PIN SMALL OUTLINE PACKAGE−525 MIL



UNIT : INCH(mm) MAX/MIN