Low Noise Oscillator

- *Tight Frequency*
- *High Stability (Low Jitter)*
- *Standard Package Options*

Series CC155

RoHS COMPLIANT 2002 / 95 / EC

Part Numbering Example: CC155 C 1 L Z - A5 B6 - 155.52 TS

CC155	C	1	L	Z	A5	B6	155.52	TS
SERIES	OUTPUT	PACKAGE STYLE	VOLTAGE	ADDED FEATURES	OPERATING TEMP.	STABILITY	FREQUENCY	TRI-STATE
CC155	C = CMOS T = TTL	1 = Full Size 4 = Half Size 7 = 5X7 Ceramic 8 = PLASTIC SMD	Blank = 5V L = 3.3 V	Blank = Bulk T = Tube Z = Tape and Reel	Blank = 0°C +70°C A5 = -20°C +70°C A7 = -40°C +85°C	B6 = ±100 ppm BP = ±50 ppm BR = ±25 ppm	155.52 MHz	TS = Tri-State PD=PowerDwn

Specifications:

Frequency Range:	155.52	MHz
Available Stability Options:	±100	ppm
	±50	ppm
	±25	ppm
Input Voltage:	5.0	VDC
± 5%	3.3	VDC
Operating Temperature	0	+70°C
Range Options:	-20	+70°C
	-40	+85°C
Storage Temperature:	-55	+125
°C		
Aging (PPM/Year)	±5	
Ta=25C, Vdd=5/3.3V		
Output Level:	TTL/CMOS	
Packaging:	Tape & Reel	
Tube	(1K / Reel)	

Operating Conditions:

	min	max	
Vdd	3.0	5.5	V
Digital Supply Voltage			
C_{TTL}		15	pF
Max Cap Load (TTL)			
C_{CMOS}		15	pF
Max Cap Load (CMOS)			

Output Clock Switching Characteristics

	Test Conditions	Min	Typ	Max	Unit
Duty Cycle:					
TTL @ 1.4 V, 4.5–5.5 Vdd	C_L = 15 pF	40		60	%
CMOS @ Vdd/2, 4.5–5.5 Vdd	C_L = 15 pF	40		60	%
Output Clock Rise/Fall	C_L = 15				
	0.8V–2.0V, 4.5-5.5 Vdd			0.9	ns
	0.2–0.8Vdd, 3.0–3.6 Vdd			2.4	ns
Start Up Time	From power on			2	ms
Power Down Delay Time	PWR_DWN pin				
Synchronous	LOW to output Hi-Z		T/2	T+10	ns
Asynchronous			10	15	ns
Output Disable Time					
Synchronous	OE pin LOW to output Hi-Z		T/2	T+10	ns
Asynchronous	T = Freq oscillator period		10	15	ns
Output Enable Time				100	ns
Period Jitter: 1 σ Sigma	> 1,000,000 SAMPLES		8	12	ps
Peak to Peak	> JEDEC std JESD65		70	100	ps

Electrical Characteristics

Input Characteristics (Pin 1):					
V_{IL}, Low–Level Input Voltage	4.5–5.5V Vdd			0.8	V
TO DISABLE OUTPUT	3.0–3.6V Vdd			0.2Vdd	V
V_{IH}, High–Level Input Voltage	4.5–5.5V Vdd	2.0			V
TO ENABLE OUTPUT OR NO CONNECT	3.0–3.6V Vdd	0.7Vdd			V
I_{IL}, Input Low Current	V_{IN} = 0V			10	µA
I_{IH}, Input High Current	V_{IN} =Vdd			5	µA
Output Characteristics:	3.0V–3.6V Vdd, 8 mA I_{OL}			0.40	V
V_{OL}, Low–Level Output	4.5V–5.5V Vdd, 16 mA I_{OL}			0.40	V
V_{OHTTL}, Hi-level Output TTL	4.5V–5.5V Vdd, -16 mA I_{OL}	2.40			V
V_{OHCMOS},	4.5V–5.5V Vdd, -16 mA I_{OL}	Vdd-0.4			V
High-level CMOS Voltage	3.0V–3.6V Vdd, -8 mA I_{OL}	Vdd-0.4			V
Power Supply Current:	4.5–5.5 Vdd			45	mA
(unloaded)	3.0–3.6 Vdd			25	mA
Standby Current:			10	50	µA
Input Pull-Up Resistor	4.5–5.5 Vdd, V_{IN} = 0V	1.1	3.0	8.0	MΩ
	4.5–5.5 Vdd, V_{IN} = 0.7V	50	100	200	KΩ
CLKOUT Pull-Down Current	5.0 Vdd		20		µA
Output Enable /	Output is Tri-Stated				
Power Down Mode	Controlled by pin 1 input				

Cardinal Components, Inc., 155 Rt. 46 W, Wayne, NJ. 07470 TEL: (973)785-1333 FAX: (973)785-0053
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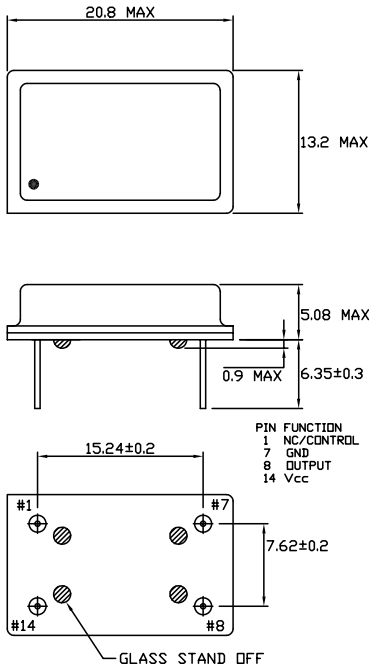
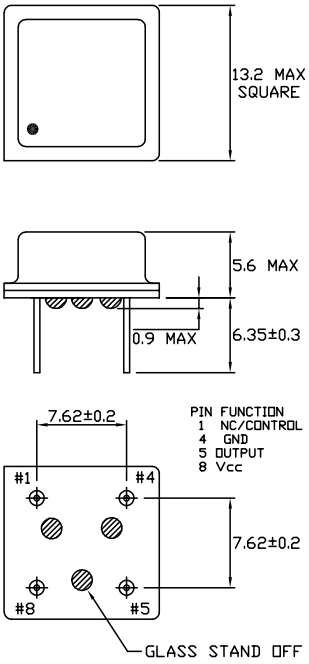
Note: Bypass Vdd to GND with a 0.01 µF Capacitor

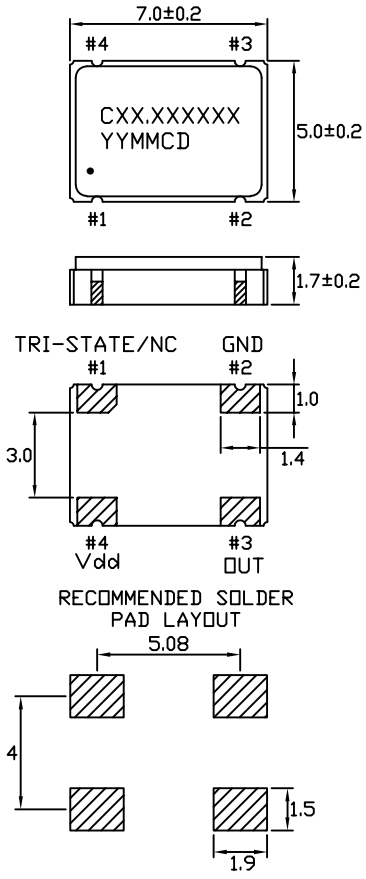
Style 1 Full Size 14 Pin Dip



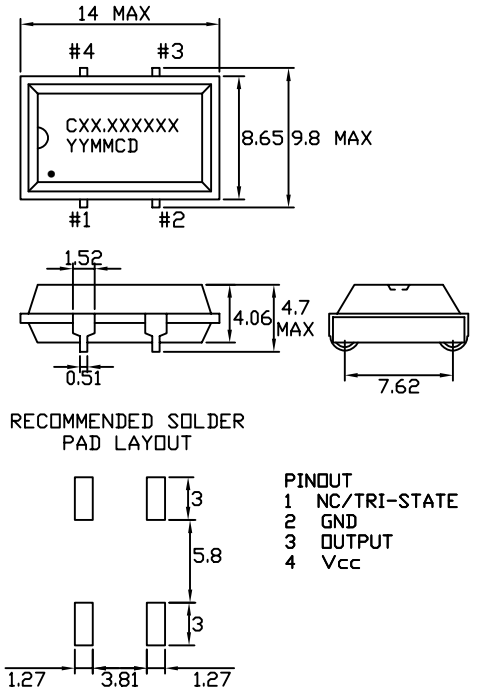
Style 4 Half Size 8 Pin



Style 7 5x7 Ceramic SMD



Style 8 Plastic SMD



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