AS8530

LIN Transceiver with Integrated Voltage Regulator and MCU Interface for Automotive Applications

1 General Description

The AS8530 is a general purpose companion IC for sensor and actuator LIN slaves offering LIN transceiver and low drop voltage regulator.

It also provides a 2-wire microcontroller interface through shared EN and TX pins to access a window watchdog with RC oscillator, control registers, backup registers and monitoring information.

The IC is fabricated in a high voltage CMOS technology which is able to withstand voltages up to 42V.

The product is available in ep-SOIC8 package.

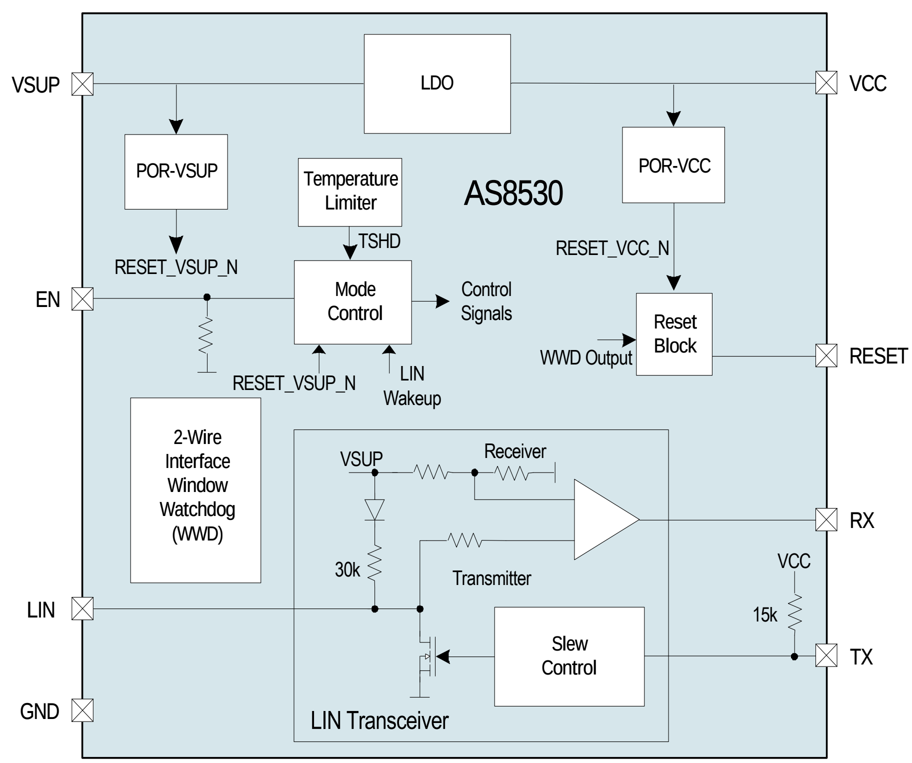
2 Key Features

- Operating voltage 6V to 18V
- Linear, low-drop voltage regulator: VCC = 5V ±5% or 3.3V ±5% as a factory programming option
- 50mA load current
- Operating modes: Normal and Standby or Normal and Sleep as a factory option
- Typically 45µA quiescent current in standby mode, Typically 35µA quiescent current in sleep mode
- Under voltage reset with factory options
- LIN bus transceiver l conforming to LIN 2.1, TX time out fail safe feature, over temperature warning and shut down
- Window watchdog if factory enabled
- Micro controller 2-wire interface through shared pins for watchdog trigger, monitoring, register read /write
- Chip ID for traceability and module ID
- 8 Backup registers to store data during VCC shut down
- ep-SOIC8 package
- -40ºC to +125ºC ambient operating temperature

3 Applications

The AS8530 is a System Basis Chip for automotive LIN networked sensor or actuator slaves.

Figure 1. AS8530 LIN Transceiver Block Diagram



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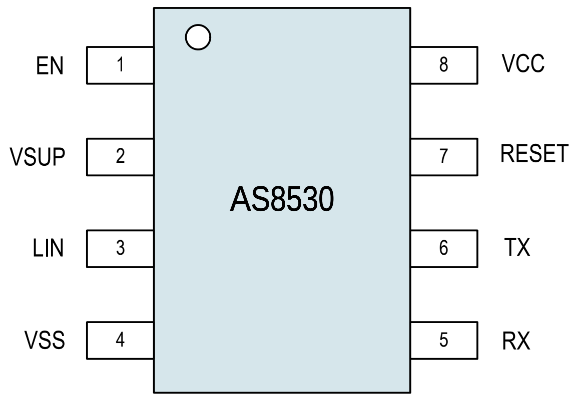
4 Pin Assignments

Figure 2. Pin Assignments (Top View)



4.1 Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Pin Name	Pin Type	Special Requirements	Description
1	EN	Digital input with pull-down	2kV ESD	Enable high-voltage compatible pin with pull down to VSS and ½ VCC trigger level, active high.
2	VSUP	Supply pad	Load dump (42V max), 4kV HBM ESD, Jump start (27V max)	Battery supply
3	LIN	Analog I/O	Conforms to LIN 2.1, 6kV HBM ESD	LIN Bus
4	VSS	Supply pad		
5	RX	Digital output with pull-up	2kV ESD	LIN transceiver receive signal, data out in test mode
6	TX	Digital input with pull-up		LIN transceiver transmit signal, clock in test mode
7	RESET	Digital output		Digital output referenced to VCC, active low
8	VCC	Supply pad		Regulated 5V / 3.3V supply for loads up to 50mA. OTP selectable

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 6 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter		Min	Max	Units	Comments
Electrical Parameters					
DC Supply Voltage	V_{SUP}	-0.3	42	V	Transient up to 500ms duration
	EN	-0.3	V_{SUP} + 0.3	V	
	V_{CC}	-0.3	7	V	
	LIN	-27	+40	V	
	RESET, RX, TX	-0.3	V_{CC} + 0.3	V	
Input current (latchup immunity) I_{scr}		-100	100	mA	Norm: JEDEC 78
Electrostatic Discharge					
Electrostatic Discharge (ESD) Norm: AEC-Q-100-002		±2		kV	For on board signals V_{CC}, TX, RX, Reset
		±4			For V_{SUP}
		±6			LIN to V_{SS}, HBM Model
Continuous Power Dissipation					
Total operating power dissipation (all supplies and outputs) P_t			0.25	W	epSOIC8 in still air, soldered on JEDEC standard board @125º ambient, static operation = no time limit
Temperature Ranges and Storage Conditions					
Storage temperature (T_{strg})		-55	+150	ºC	
Package body temperature (T_{body})			+260	ºC	*The reflow peak soldering temperature (body temperature) specified is in accordance with IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).
Humidity non-condensing		5	85	%	
Moisture Sensitive Level		3			Represents a maximum floor life time of 168h

6 Electrical Characteristics

6.1 Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{SUP}	Positive Supply Voltage	Normal operating condition	6		18	V
VSS	Negative Supply Voltage		0			V
T_{AMB}	Ambient temperature	Maximum junction temperature (T_J) 150ºC	-40		+125	ºC
I_{supp}	Supply Current				65	mA

6.2 Digital Inputs and Outputs

All pull-up, pull-downs have been implemented with active devices. RESET and RX have been measured with 100pF load.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
EN Input						
V_{IH}	High level input voltage	High Voltage Pin which can also be connected to VSUP	$0.8V_{CC}$			V
V_{IL}	Low level input voltage				$0.2V_{CC}$	V
I_{LEAK}	Input leakage current	EN = L	-1		+1	µA
I_{pd_en}	Pull down current	EN = V_{CC}	20		40	µA
TX						
V_{IH}	High level input voltage		$0.8V_{CC}$			V
V_{IL}	Low level input voltage				$0.2V_{CC}$	V
I_{LEAK}	Input leakage current	TX = V_{CC}	-1		+1	µA
I_{pu}	Pull up current	TX pulled to VSS	-30		-10	µA
RESET						
V_{OH}	High level output voltage	I_{OUT} = 1 mA, $V_{SUP} \geq 6V$	V_{CC} - 0.5			V
V_{OL}	Low level output voltage	$V_{SUP} \geq 6V$			VSS + 0.4	V
RX						
V_{OH}	High level output voltage		V_{CC} - 0.5			V
V_{OL}	Low level output voltage	I_{OUT} = 1 mA, $V_{SUP} \geq 6V$			VSS + 0.4	V

6.3 Detailed System and Block Specifications

6.3.1 Electrical System Specifications

Symbol	Parameter		Conditions	Min	Typ	Max	Units
IDD_{nom}[1]	Current consumption	Normal mode	No load on V_{CC}, LIN recessive, V_{SUP}= 12V		300		µA
			No load on V_{CC}, LIN dominant, V_{SUP} = 12V		700		µA
		Stand-by mode	Up to 125°C ambient (no load), V_{SUP}= 12V		45		µA
		Sleep mode	Up to 125°C ambient (no load), V_{SUP}=12V		35		µA

1. No external load on the LIN bus

6.4 Low Dropout Regulator

The LDO block is a linear voltage regulator, which provides a regulated (band-gap stabilized) output voltage (V_{CC}) from the battery supply voltage (V_{SUP}).

(6V < V_{SUP} < 18V for option 1, 6V <VSUP <18V option2; -40°C < T_J < 150°C; all voltages are with respect to ground (VSS); positive current flows into the pin), normal operating mode if not otherwise mentioned.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{CC}	Regulated supply voltage I_{LOAD} 0mA to 50mA	Option 1		4.75		5.25	V
		Option 2		3.135		3.465	
T_J	Junction Temperature			-40		150	ºC
V_{SUP}	Supply Voltage Range			6	12	18	V
V_{CC}	Output Voltage Range	Option 1	Load < 50mA	4.75	5.0	5.25	V
			50mA to 65mA	4.5		5.5	
			Standby mode @ ICC < 5mA	4.5		5.5	
			Load-dump condition, I_{LOAD} < 50mA			5.5	
		Option 2	Load < 50mA	3.135	3.3	3.465	
			50mA to 65mA	2.97	3.3	3.63	
			Standby mode @ ICC < 5mA	2.97		3.63	
			Load-dump condition, I_{LOAD} < 50mA			3.63	
ICC_SH	Output Short Circuit Current	Normal mode		50		250	mA
		Standby mode		5		250	
$dV_{CC}1$	Line Regulation	$\Delta V_{CC} / \Delta V_{SUP}$				8	mV/V
LOREG_SM	Load Regulation (Standby mode)	$\Delta V_{CC} / \Delta ICCn$ (for I_{LOAD} > 500µA)				10	mV/mA
LOREG_NM	Load Regulation (Normal mode)	$\Delta V_{CC} / \Delta ICCn$ (for I_{LOAD} > 500µA)				1	mV/mA
CL1	Output Capacitor (Electrolytic)			2.2		10	µF
ESR1				1		10	Ω
CL2	Output Capacitor (Ceramic)			100		220	nF
ESR2				0.02		1	Ω
CSUP1E	Input capacitor (Electrolytic)	For EMC suppression		10		100	µF
ESR1_CSUP				1		10	Ω
CSUP2C	Input capacitor (Ceramic)			100		220	nF
ESR2_CSUP				0.02		1	Ω

6.5 LIN Transceiver

6.5.1 DC Electrical Characteristics

(4.5V < V_{CC} < 5.5V; 6V < V_{SUP} < 18V; -40°C < T_J < 150°C, VBUS is the voltage on the LIN node. All voltages are with respect to ground (VSS); positive current flows into the pin.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Driver						
I_{bus_lim}		Current limitation in Dominant State [1] LIN = V_{SUP}_max	40	120	200	mA
LIN_V_{OL}		Output Voltage BUS (dominant state), I_{LIN} = 40mA (short-circuit condition tested at V_{OL} = 2.5V)			2	V
	Pull-up resistor	Normal mode (recessive BUS level on TX pin)	20	40	60	kΩ
$I_{bus\_leak\_rec}$		Driver OFF; V_{SUP} = 7.0V, 8V < VBUS < 18			20	µA
Receiver						
$I_{bus\_leak\_dom}$	Input Leakage current at receiver	Input Leakage current at receiver Driver OFF; Vbus = 0V; V_{SUP} = 12V; V_{CC} = 5V	-1			mA
$I_{bus\_no\_GND}$		VSS = V_{SUP}; V_{SUP} = 12V; 0V < VBUS < 18V, V_{CC} = 5V [2]	-1		1	mA
$I_{bus\_no\_bat}$		V_{SUP} = VSS; 0V < VBUS < 18V, V_{CC} = VSS [2]			100	µA
V_{bus_dom}					0.4	V_{SUP}
V_{bus_rec}			0.6			V_{SUP}
V_{bus_cnt}		$V_{bus\_cnt} = (V_{th\_dom} + V_{th\_rec})/2$ [3]	0.475		0.525	V_{SUP}
V_{hys}		$V_{hys} = (V_{th\_dom} – V_{th\_rec})$ [3]	0.05		0.175	V_{SUP}

1. This failure condition triggers thermal shut down when shut down temperature threshold is exceeded.
2. Not production tested.
3. Vth_dom: Receiver threshold of the recessive to dominant LIN bus edge
   Vth_rec : Receiver threshold of the dominant to recessive LIN bus edge

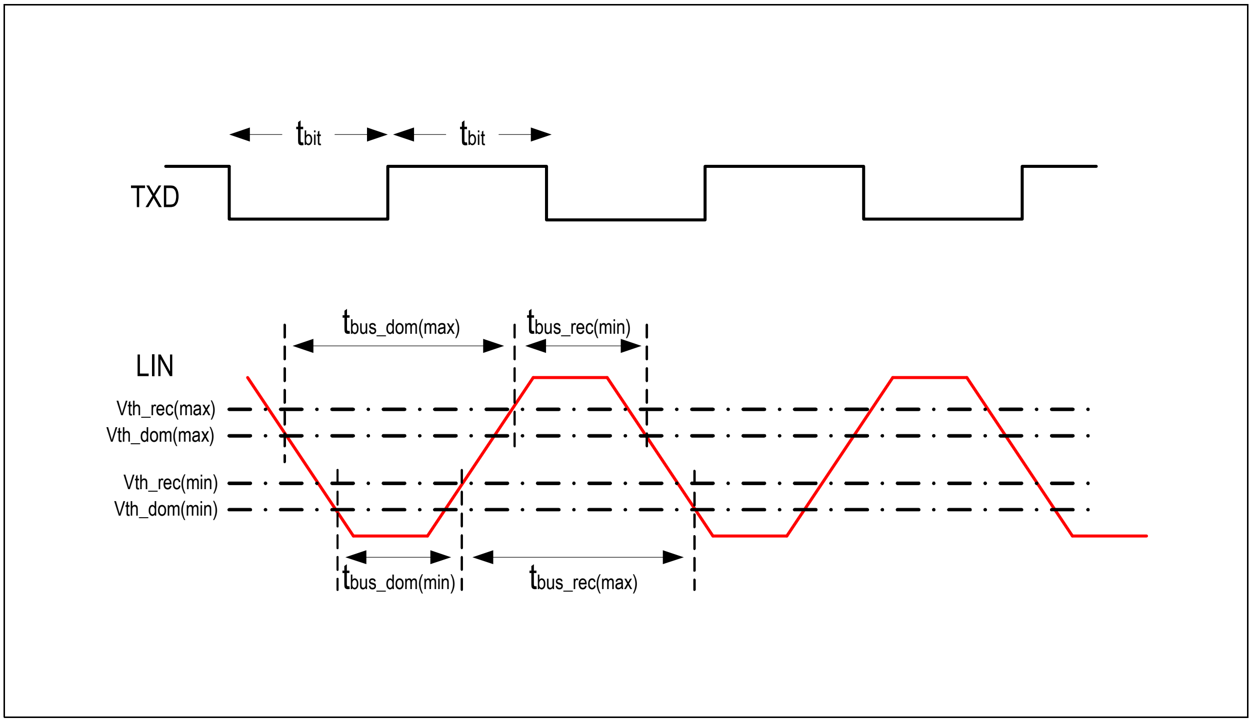
6.5.2 AC Electrical Characteristics

LIN Driver, Bus load conditions (C_{BUS} ; R_{BUS}): 1nF; 1kΩ / 6,8nF; 660Ω / 10nF; 500Ω

Symbol	Conditions	Min	Typ	Max	Units
D1 (worst case 20Kbps transmission)	V_{th_rec}(max) = 0.744 x VSUP; V_{th_dom}(max) = 0.581 x VSUP; VSUP = 6.0V to 18V; tbit = 50µs; D1 = tbus_rec(min) / (2 x tbit)	0.369			
D2 (worst case 20kbps transmission)	V_{th_rec} (min) = 0.422 x VSUP; V_{th_dom} (min) = 0.284 x VSUP; VSUP = 6V to 18V; tbit = 50µs; D2 = tbus_rec(max) / (2 x tbit)			0.581	
D3 (worst case 10.4kbps transmission)	V_{th_rec} (max) = 0.778 x VSUP; V_{th_dom} (max) = 0.616 x VSUP; VSUP = 6.0V to 18V; tbit = 96µs; D3 = tbus_rec(min) / (2 x tbit)	0.417			
D4 (worst case 10.4kbps transmission)	V_{th_rec} (min) = 0.389 x VSUP; V_{th_dom} (min) = 0.251 x VSUP; VSUP = 6V to18V; tbit = 96µs; D4 = tbus_rec(max) / (2 x tbit)			0.59	
t_{dLR}	V_{CC} = 5V; Propagation delay bus dominant to RX LOW			6	µs
t_{dHR}	V_{CC} = 5V; Propagation delay bus dominant to RX HIGH			6	µs
t_{RS}	Receiver Delay symmetry	-2		2	µs
t_{wake}	Wake-up delay time	30		150	µs
t_{sln}	Transition from standby mode to normal mode (clock frequency is 128kHz ± 25%)		4		Clock cycles
t_{nsl}	Transition from normal mode to standby mode (clock frequency is 128kHz ± 25%)		6		Clock cycles
t_{rec_deb}	Receiver De-bounce time	1		3	µs
C_{int}	Guaranteed by design		220	250	pF

Note: Sleep-mode to Normal mode transition is identical to the Power-ON sequence after the remote wakeup event on LIN bus. The transition time will include the t_{Res} (RESET time) and start-up time for the LDO.

Figure 3. LIN Timing



6.5.3 Temperature Limiter

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{sd}	Shut down temperature	Junction temperature	139		171	ºC
T_{ret}	Return temperature	During shut down, the sensor must be powered by VSUP. Thermal shut down disables LDO and sets all drivers to high impedance, the IC returns from shut down with POR.	121		149	ºC
T_{otset}	Over-temp warning flag set	The temperature beyond which the warning flag is set.	121		149	ºC
$T_{otclear}$	Over-temp warning flag clear	The return temperature when the warning flag is cleared	103		127	ºC

6.5.4 TX Timeout Watchdog

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{lin_wdog}	Time out duration (dominant state)		0.5	1	2	s

6.6 V_{CC} Undervoltage Reset and Window Watchdog

The values in this table are valid for normal and standby modes. All parameters are tested, unless mentioned otherwise.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Vuvr_off	VCC under-voltage threshold off (Default)	Rising edge of VCC	2.55		2.95	V
Vuvr_on	VCC under voltage threshold on (Default)	Falling edge of VCC	2.3		2.7	V
Vuvr1_off	VCC under voltage threshold off (Factory Option)	Rising edge of VCC [1]	3.0		3.4	V
Vuvr1_on	VCC under voltage threshold on (Factory Option)	Falling edge of VCC [1]	2.75		3.15	V
Vuvr2_off	VCC under voltage threshold off (Factory Option)	Rising edge of VCC [1]	3.5		3.9	V
Vuvr2_on	VCC under voltage threshold on (Factory Option)	Falling edge of VCC [1]	3.25		3.65	V
Vuvr3_off	VCC under-voltage threshold off (Factory Option)	Rising edge of VCC [1]	4.0		4.4	V
Vuvr3_on	VCC under voltage threshold on (Factory Option)	Falling edge of VCC [1]	3.75		4.15	V
Vhyst_vcc	Hysteresis of under-voltage threshold on/off VCC	Default and all other factory options	0.1	0.25	0.4	V
t_{rr}	Spike filter on VCC	To remove disturbance	4			µs
Vsuvr_off	VSUP under-voltage threshold off			3.85		V
Vsuvr_on	VSUP under-voltage threshold on	BOR level (considered to be the Master Reset for AS8530)		3.25		V
WD_TCL	WWD non-service time (if factory enabled)	RESET will be generated [1 2]	0-75	0 -100	0-125	ms
WD_TSV	WWD Service – time (if factory enabled)	RESET will not be generated [1]	75-150	100-200	125-250	ms
t_{Res}	Reset delay time	4ms, 16ms, 32ms (typ) are factory options (min = -25% and max = +50% of typical)	6	8	12	ms
T_{shd}	Temporary shutdown reset active time		0.1		1	s

1. These are factory options which could be made available on specific request.
2. -40%, -20%, +20%, +60%, and +100% timings are available as factory options.

6.7 Two Port Serial Interface

Symbol	Parameter	Conditions	Min	Typ	Max	Units
General						
BR_{2WIRE_SPI}	Bit rate				250	Kbps
T_{ENSCLK_H}	Clock high time		2			µs
T_{ENSCLK_L}	Clock low time		2			µs
Write timing						
t_{DI_SU}	Data in setup time		20			ns
t_{DI_HD}	Data in hold time		10			ns
Read timing						
t_{DO_S}	Data out setup time		130			ns
t_{DO_HD}	Data out hold time		135			ns
t_{DO_D}	Data out delay				80	ns
t_{DI_HZ}	Data in to high impedance delay	Time for the Microcontroller to release the TX bus			80	ns
Timing parameters when entering 2-Wire SP mode						
T_{tx_su}	TX setup time before EN goes Low		20			ns
T_{tx_hd}	TX hold time after EN goes High		20			ns
$T_{tx\_SP\_trigger}$	EN falling edge to TX falling edge	To enter into 2-Wire SP mode	2		10	µs
$T_{STNDY\_trigger}$	TX high time from EN falling edge	To enter into Sleep/Standby mode	5			cycles
T_{en_ENSCLK}	EN falling edge to start of 2-wire serial port clock		5			cycles

7 Detailed Description

The AS8530 chip consists of a low drop-out regulator and a LIN bus transceiver, which is a bi-directional bus interface for data transfer between LIN bus and the LIN protocol controller. Additionally integrated is a RESET unit with a power-on-reset delay and a programmable window watchdog. It also includes a watchdog time-out on LIN TX node to indicate if the microcontroller is stuck in a loop and to release unintentional LIN bus dominant state.

7.1 Voltage Regulator (LDO)

The voltage regulator has three operating modes. The features of the operating modes are given below:

- Normal mode: Stability to be better ±0.25V over input range and temperature for load current up to 50mA. The LDO Output provides a voltage of 5V or 3.3V as OTP option.
- Standby mode: The Standby mode is a low quiescent current mode used in car applications that are always switched on. The load current in standby mode is 5mA. Quiescent current (no load) is less than 45mA typically at room temperature.
- Sleep mode: Power down or temporary shutdown of the regulator can be set by a register bit. This bit can be written through 2-wire MCU interface.

The LDO takes the input from bandgap and scales it up to the required voltage. The LDO starts charging only after the POR-VSUP event occurs (RESET_VSUP_N switched from low to high). The LDO can be powered-down by a control signal (temporary shutdown register) for the temporary shutdown mode.

7.2 Temperature Limiter

Temperature limiter produces a power down when temperature exceeds 155ºC ±10%. It powers up and generates a reset when it returns to 135ºC ±10% junction temperature. During thermal shut down, temperature sensor is supplied by VSUP. During the temperature ramp-up phase, as soon as the temperature exceeds 135ºC ±10%, a warning signal is issued and is written into the diagnostic register, which can be read through the SP interface.

7.3 VSUP Undervoltage Reset

VSUP undervoltage reset generates a reset RESET_VSUP_N, switched from low to high when VSUP ramps up above VSUVR_OFF. This is used to enable proper initialization of mode control and diagnostic registers. If VSUP < VSUVR_ON, then RESET_VSUP_N switches from high level to low level (active). This is considered to be the master reset and will have the highest priority over all other signals. As soon as VSUP < VSUVR_ON, the LDO, LIN Transceiver is completely shut off and system comes to a complete stop. AS8530 enters into the normal operating mode only after VSUP > VSUVR_OFF.

7.3.1 VSUP Undervoltage in Normal Mode

Supply Voltages below VSUVR_OFF and above VSUVR_ON do not influence the voltage regulator. The output voltage VCC follows VSUP.

7.3.2 VSUP Undervoltage in Standby Mode / Sleep Mode

No exit from the sleep mode or standby mode take place if the VSUP voltage drops down to VSUVR_OFF. If VSUP goes below VSUVR_ON, RESET_VSUP_N is active and resets the mode control and diagnostic register. The voltage regulator, LIN Transceiver modules are turned off. If VSUP rises again above VSUVR_OFF, RESET_VSUP_N is switched from low to high. The system enters normal mode where LIN Transceiver and LDO are switched on.

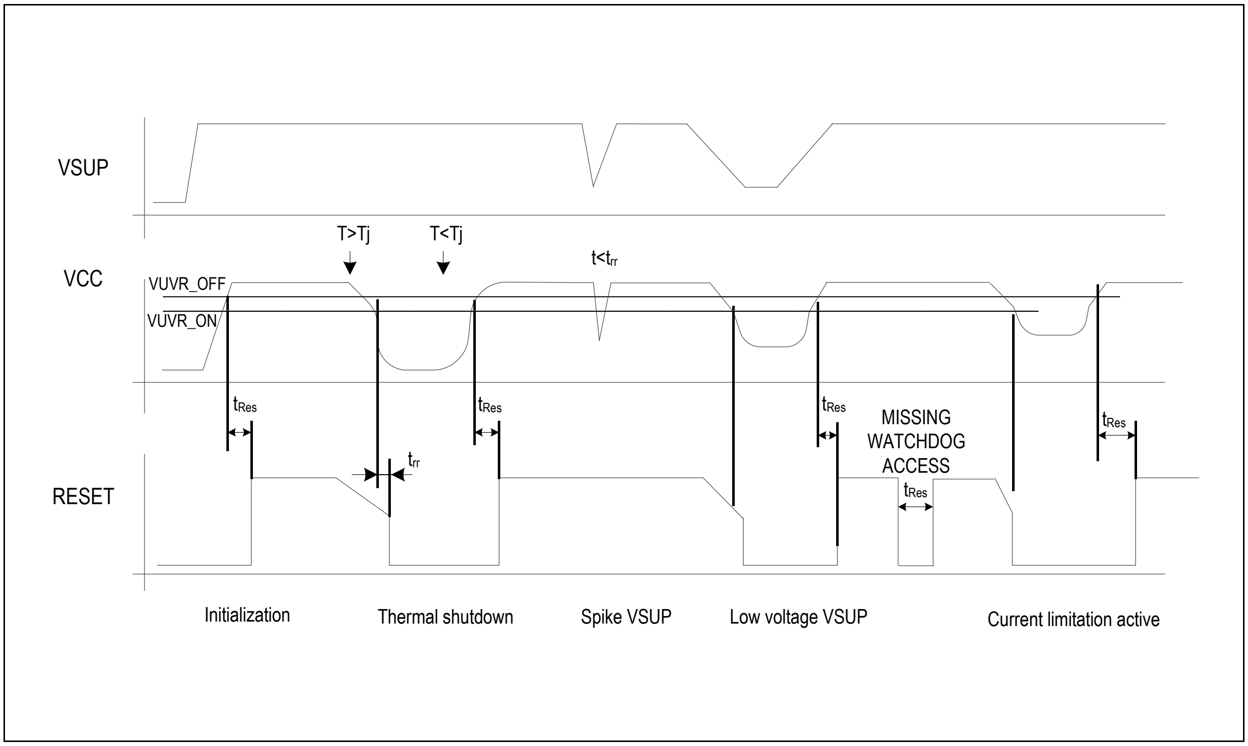
7.3.3 VSUP Undervoltage in Low Slew Mode

The behavior of AS8530 at low VSUP voltages is equal to the sleep mode. The low slew mode (set by control register through serial interface as an option) will be cancelled, if VSUP drops below VSUVR_ON in this mode. The AS8530 enters the normal mode, if VSUP rises again above VSUVR_OFF.

7.4 RESET

Reset generates an external RESET signal to reset the microcontroller and all other external circuits. The reset functionality is illustrated in Figure 4. Reset consists of a digital buffer at the output. RESET signal can be affected by RESET_VCC_N (which is the under-voltage reset on V_{CC}) and Window watchdog output. All those conditions which cause a drop in the V_{CC} voltage will be detected from the low voltage reset unit, which in-turn generates a reset signal. States like Temporary shut-down, Over-temperature monitor will influence the RESET output through RESET_VCC_N signal only.

Figure 4. Reset Functionality



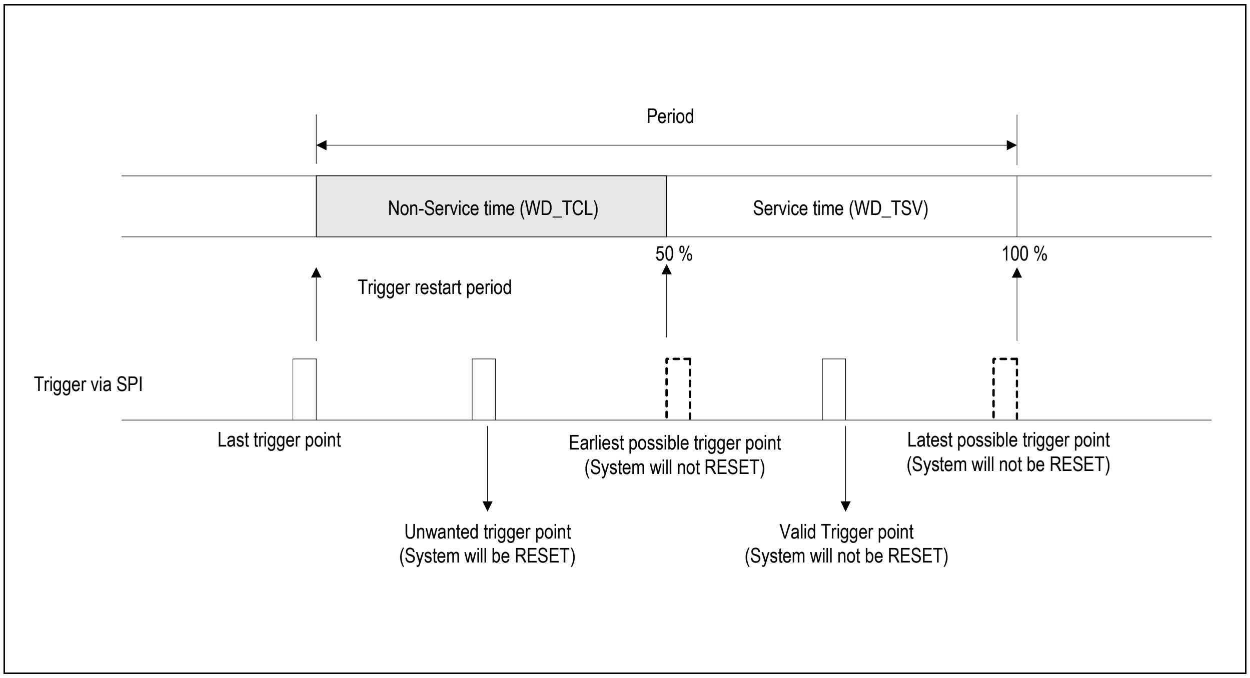
7.5 V_{CC} Undervoltage Reset

The POR-VCC generates RESET_VCC_N signal as output which determines under-voltage reset of the output of the LDO. The rising edge of the V_{CC} gives an under-voltage reset “off” and the falling edge of the V_{CC} gives an under-voltage reset “on”. This under-voltage signal is used to control the RESET output. When V_{CC} rises up Vuvr_off for a period greater than reset duration (tRes) then RESET_VCC_N switches from low level to high level and pin RESET is inactive (high). If V_{CC} falls below Vuvr_on for a period greater than a predetermined delay (trr) then RESET_VCC_N switches from high level to low level and pin RESET is active (low). The RESET_VCC_N signal is used to initializes Window watchdog timer, TX time-out, Test control circuits, 2-wire SP, and logic associated with SP (everything other than the SP control registers). V_{CC} under-voltage reset threshold voltage level adjustment can be made by 2 bit OTP as explained in OTP interface.

7.6 Window Watchdog (WWD)

To keep the external microcontroller always in proper function state, a window watchdog circuit is implemented. The WWD trigger is generated by external MCU through SP interface. If the window is missed, a reset on the RESET pin with certain reset time (t_{Res}) is generated. The WWD function can be enabled or disabled by factory setting. The watchdog is started after the ASSP exits reset. Under normal working conditions, microcontroller gives a WWD trigger every time in the window period of WD_TSV (service time). If the trigger does not occur during WD_TSV or occurs too early during WD_TCL (non-service time), then RESET output is pulled low (active), which will reset the micro-controller. WWD circuit is turned on after the RESET pin goes back to high (inactive). If V_{CC} < Vuvr_on, WWD circuit is switched off. When the WWD function is enabled, there is a 3-bit factory programming available to set the trigger window.

Figure 5. Window Watchdog Trigger



7.7 LIN Transceiver

The transceiver provides short circuit limitation, hardware watchdog and over temperature shut down features. The TX watchdog timer is active when TX is pulled low (active). As soon as the TX watchdog timeout occurs, the LIN bus is released from dominant state to recessive state. The LIN transceiver has a pull-up resistor (for the slave node; extra resistor externally for the master node) to the V_{SUP}. A diode protection is available to protect it from back supply from bus line.

The LIN transmitter has the basic functionality of relaying the data from the micro-controller on to the LIN. The data on the LIN needs to have controlled slew to have reduced EMI. The receiver relays the data from the LIN to the micro-controller. This transmitter has optimized EMC performance across different loading conditions conforming to the LIN 2.1 standards. The wake-up detects a wake up event on the LIN.

7.8 Operating Modes and States

The AS8530 provides four main operating modes “normal”, “sleep/stand-by” (programmed by OTP), “temporary shutdown” and “thermal shutdown”. The LIN transceiver can be programmed to operate with lower slew in the normal mode. Refer to Table 3 for a detailed description on transition for each mode.

7.8.1 Normal Mode

This is the mode after the power-up. In normal mode, LDO, LIN Transceiver, Window Watchdog, Resistive divider and the line drivers are all turned on. All the blocks are completely functional. LDO is now capable of delivering maximum load current possible as per the device specifications. The LIN Transceiver is capable of sending the TX data from microcontroller to the LIN bus at a maximum rate of 20Kbps. EN signal is set to high and LIN, TX, RX pins can be driven into dominant (low) or recessive (high) states. If the junction temperature increases more than T_{otset}, a warning flag is set in the diagnostic register, which can be read through the 2-wire interface.

7.8.2 Standby Mode

Standby mode is a functional low-power mode where LIN Transceiver is disabled. The LIN wake-up circuit and over-temperature monitor circuit is enabled. Window watchdog, TX timeout watchdog, Resistive divider, relay driver circuits are disabled. EN pin held low in this mode. TX pin is in recessive state (high). CS is pulled to V_{CC} while SDI and SCLK outputs are pulled to VSS.

7.8.3 Sleep Mode

As a factory programming option on request the AS8530 offers as a replacement to the standby mode with sleep mode. Sleep mode is the most current saving mode. If EN is held low, the LDO, LIN Transceiver and the reset and window watchdog unit will be switched off. V_{CC} is pulled down to zero. The LIN wake-up circuit, oscillator and over-temperature monitor circuit is active. LIN bus is in recessive state (high). Only wake-up possible is through remote wake-up, through LIN pin, pulling it to dominant state for 100µs typical (low), can change the state of the system.

7.8.4 Temporary Shutdown Mode

In this mode, the VCC is pulled down and the LDO is powered down. This mode is introduced to interface with other components which do not have a pin for the reset functionality. This provides an alternative way to reset those components interfacing with AS8530. This mode is default disabled but can be enabled by an OTP option. In this mode, all internal modules supplied by the LDO are disabled. Only the oscillator, control registers are enabled. The VCC output can be temporarily switched off and pulled to VSS. EN signal, RX, TX is pulled low and LIN Transceiver along with the LIN wake-up circuit is powered down. No remote wake-up functionality is possible. LIN bus enters into recessive state. The system goes out of this mode to normal mode after the time-out of an internal counter delay (T_{shd}). Normal mode to temporary shutdown transition will be controller by register bit in configuration register.

7.8.5 Thermal Shutdown State

If the junction temperature T_J is higher than T_{sd}, the AS8530 will be switched into the thermal shutdown mode. The transceiver is completely disabled. No wake-up functionality is available. Window watchdog, TX timeout watchdog, and LDO are completely turned off. Only the over-temperature monitor would be working. As soon as the temperature returns back to T_{ret}, the system enters normal mode. For more information on transition, see Table 3.

Table 3. Transition Table

Transition		Interface				Reg.	Flags				Comments
From mode	To mode	LIN	RX	TX	EN	0x05 D0	rwake	Uvbat	OT	Uvcc	
Normal Mode	Stand-By	X-RS	X-H[2]	H[3]	H-L[3]	L	X	X	inactive	inactive	TX is high for $T_{STNDY\_triggerr}$
	Sleep[1]	X-RS	X-H[2]	H[3]	H-L[3]	L	X	X	inactive	set	TX is high for $T_{STNDY\_triggerr}$[1]
	Temporary Shutdown	X-RS	X-H[2]	X	H[3]	H	X	X	inactive	set	The Control Bit is set through the 2-Wire SP interface
	Over-Temperature	X-RS	X-H[2]	X	X	L	X	X	set	set	
Stand-By Mode	Normal (LW)	X	H-X[2]	X	L-H[3]	L	X	X	inactive	inactive	
	Normal (RW)	X	H-X[2]	H	X	L	set	X	inactive	inactive	Remote Wake up Event occurred on LIN
	Temporary Shutdown	RS	H[2]	H	L	H[3]	X	X	inactive	set	The Control Bit is set through the 2-Wire SP interface
	Over-Temperature	RS	H[2]	H	L	L	X	X	set	set	
Temporary Shutdown Mode	Normal	RS-X	H-X[2]	X	X	L	X	X	inactive	clear	Internal 128ms timer expired
Sleep Mode[3]	Normal	RS-X	H-X[2]	X	X	L	set	X	inactive	clear	Remote Wake up Event occurred on LIN
	Over-Temperature	RS	H[2]	X	X	L	X	X	set	hold	Temperature monitor output asserted (covered by scan)
All States	Power Off	X	X	X	X	X	X	L-H[3]	X	X	

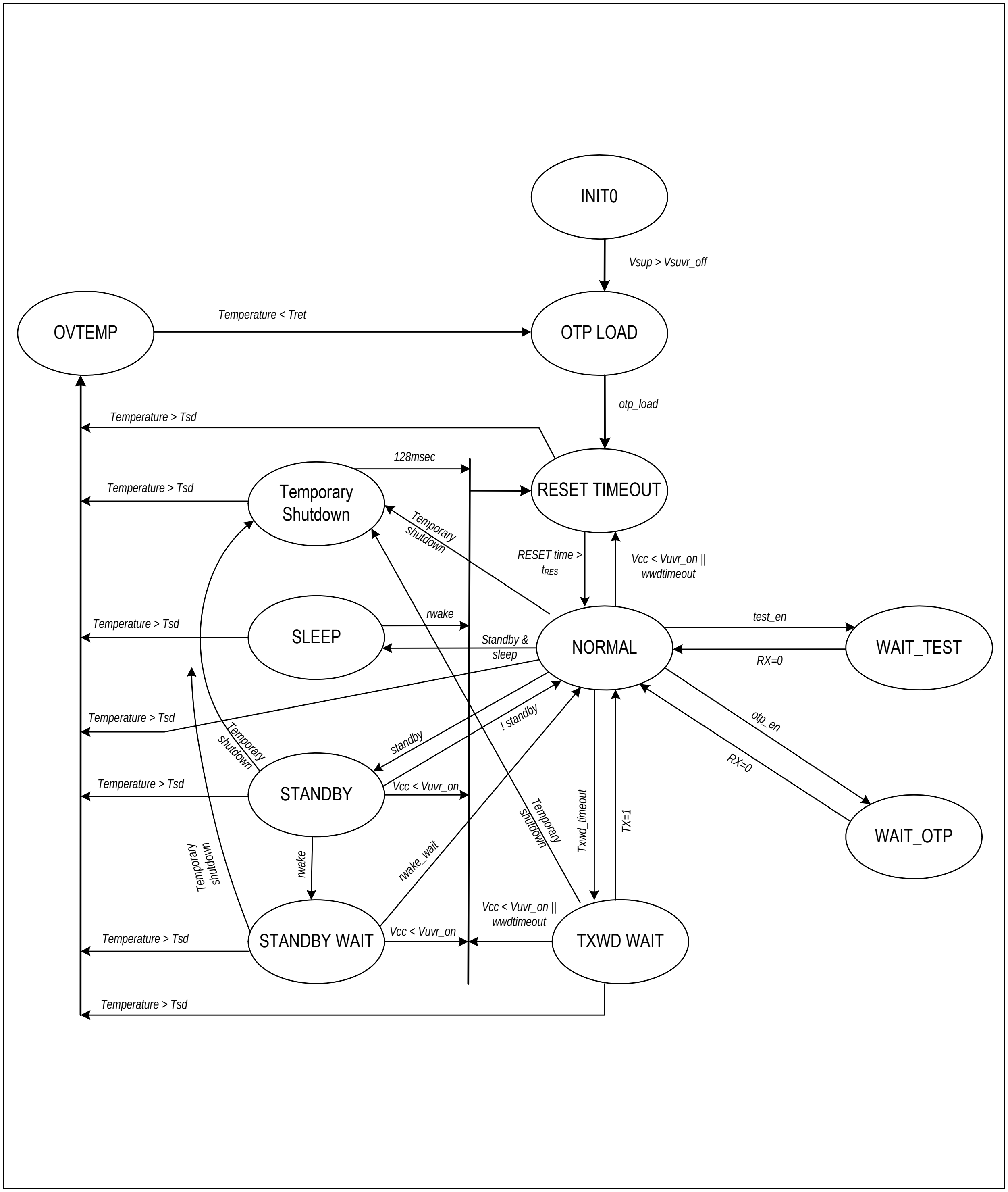
1. Chosen by factory programming option
2. Effect of Transition
3. Cause for Transition

Note: L = low state, H = high state, OT = Over-temperature Reset, Uvcc = Undervoltage VCC, Uvbat = Undervoltage VBAT, rwake =remote wake, X = do not care.

7.9 State Diagram

The complete functional state machine for AS8530 is illustrated in Figure 6. Some soft-states in the FSM like “TXWD Wait”, “Standby Wait” and other “wait” states have been included for the sake of completeness.

Figure 6. Finite State Machine Model for the AS8530 System



8 Application Information

8.1 Initialization

When the power supply is switched on, if VSUP > VSUVR_OFF, RESET_VSUP_N becomes inactive (high). After this, the voltage regulator starts with a default LDO output setting of 3.3V and Vuvr_off setting of 2.75V. If VCC > Vuvr_off (2.75V), active-low PORN_2_OTP is generated. The rising edge of PORN_2_OTP loads contents of fuse onto the OTP latch after load access time T_{Load}. LOAD_OTP_IN_PREREG signal loads contents of OTP latch onto the pre-regulator domain register. This register gives actual settings of LDO, Vuvr_off and Reset Timeout period T_{Res}. This is done because the OTP block is powered by the VCC. If VCC > Vuvr_off (phase 2), Reset timeout is restarted. RESET signal is de-asserted after Reset Timeout period T_{Res} (phase 2) and then device enters into normal mode. The circuit initializes correctly also for very slow ramp on VSUP (of the order of 0.5V/min).

Figure 7. Initialization Sequence for AS8530

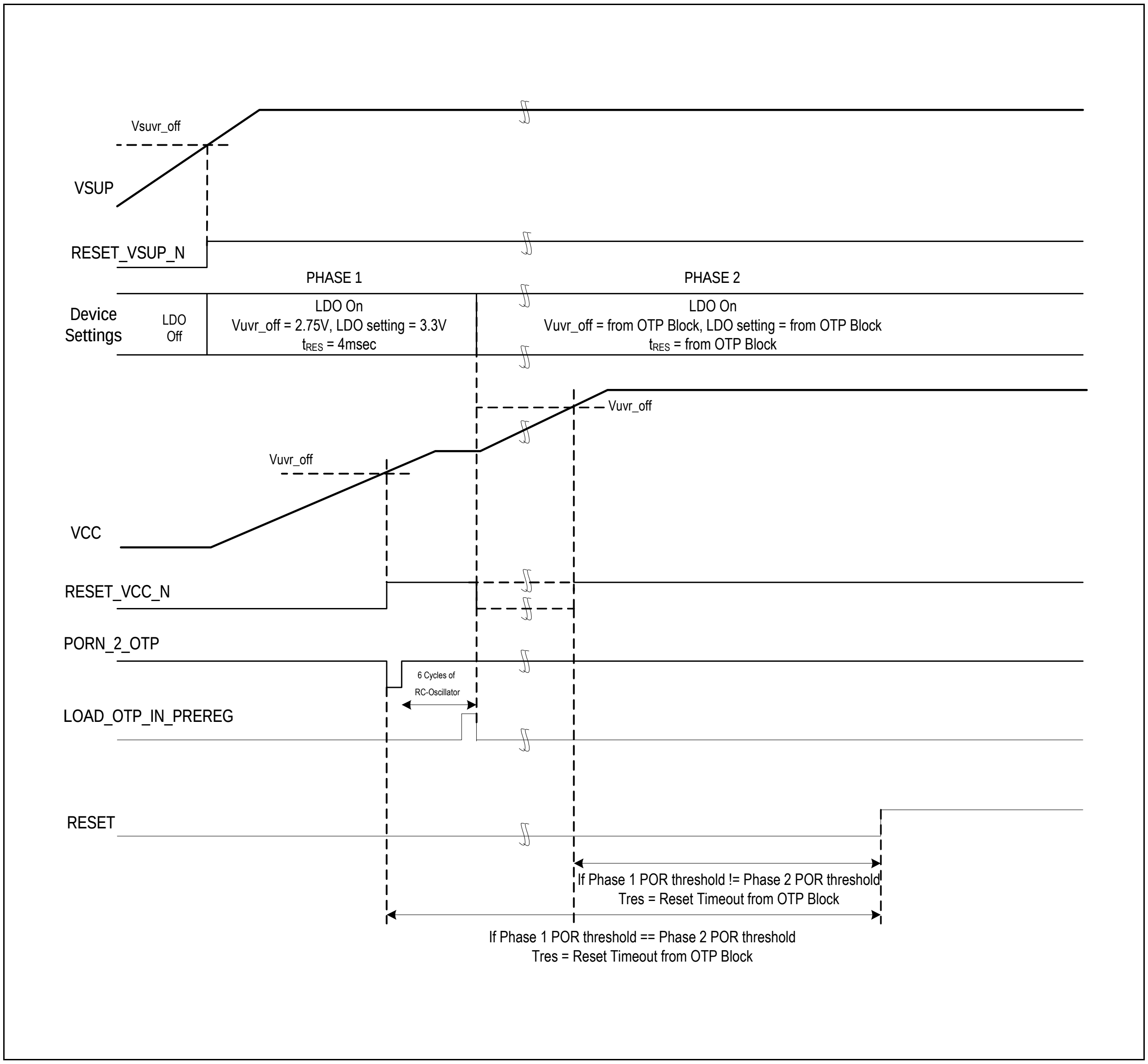


Table 4. VSUP>Vsuvr_on and VCC<Vuvr_on

Block	Output Signal
TRANSCEIVER = Enabled (disabled only during initial VSUP ramp-up)	LIN = high-z, RX = follows V
LDO = Enabled (disabled only during initial ramp-up)	VCC = low
RELAY DRIVER = Enabled	LDRIVE1 = high, LDRIVE2 = high
RESET = Enabled	RESET = high-z
RESISTIVE DIVIDER = Enabled	VBAT= high, VBAT_DIV = enabled

Table 5. VSUP<Vsuvr_on

Block	Output Signal
TRANSCEIVER = Disabled	LIN = high-z, RX = high-z
LDO = Disabled	VCC = low
RELAY DRIVER = Disabled	LDRIVE1 = high, LDRIVE2 = high
RESET = Disabled	RESET = high-z
RESISTIVE DIVIDER = Disabled	VBAT = high, VBAT_DIV = low

8.2 Wake-Up

If the regulator is put into sleep/standby mode, it can be woken up with the BUS interface. A transition on the BUS (high to low) with a minimum predefined low time (t_{wake}) puts the regulator into normal mode.

8.3 Over-Temperature Shutdown

If the junction temperature increases beyond T_{sd} the over-temperature recognition will be activated and the regulator voltage will be switched off. The VCC voltage drops down, the reset state is entered and the bus transceiver is switched off (recessive state). After TJ falls below T_{ret}, the AS8530 will be initialized again. This initialization starts independently from the voltage levels on EN and BUS. Within the thermal shutdown mode, the transceiver cannot switch to the normal mode either with local or with remote wake-up. The operation of the AS8530 is possible between TJ (125ºC) and the switch off temperature T_{sd}, but small parameter differences can appear. After over-temperature switch-off, the IC initializes as explained in Initialization on page 18. The low slew mode for LIN Transceiver has to be selected again on re-initialization, if necessary.

8.4 LIN BUS Transceiver

The AS8530 has an integrated bi-directional bus interface device for data transfer between LIN bus and the LIN protocol controller. The transceiver consists of a driver with slew rate control, wave shaping and current limitation and a receiver with high voltage comparator followed by a de-bouncing unit.

8.4.1 Transmit Mode

During transmission the data at the pin TX will be transferred to the BUS driver to generate a bus signal. To minimize the electromagnetic emission of the bus line, the BUS driver has an integrated slew rate control and wave shaping unit.

Transmitting will be interrupted in the following cases:

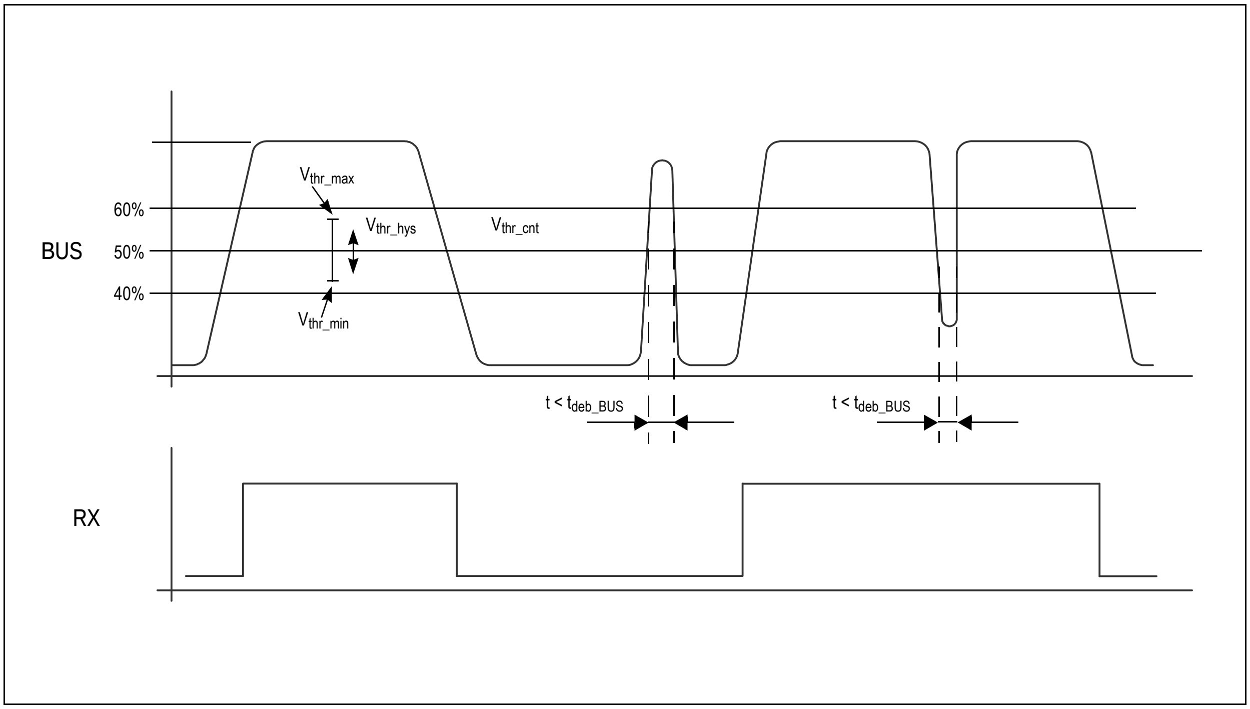
- Sleep mode
- Thermal Shutdown active
- Master Reset (VSUP < Vsuvr_on)

The recessive BUS level is generated from the integrated 30k pull up resistor in serial with an active diode This diode prevents the reverse current of VBUS during differential voltage between VSUP and BUS (VBUS>VSUP). No additional termination resistor is necessary to use the AS8530 in LIN slave nodes. If this IC is used for LIN master nodes it is necessary that the BUS pin is terminated via an external 1kΩ resistor in series with a diode to VBAT.

8.4.2 Receive Mode

The data signals from the BUS pin will be transferred continuously to the pin RX. Short spikes on the bus signal are suppressed by the implemented de-bouncing circuit. Including all tolerances the LIN specific receive threshold values of 0.4*VSUP and 0.6*VSUP will be securely observed.

Figure 8. Receive Mode Impulse Diagram

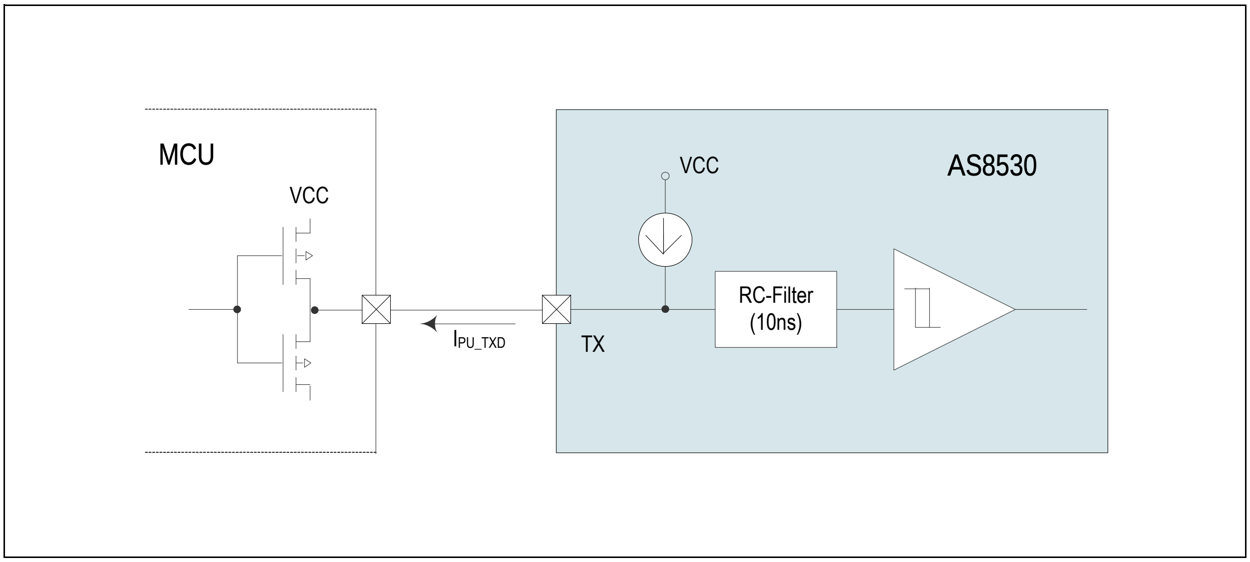


8.5 RX and TX Interface

Input TX.

The 5V input TX controls directly the BUS level. LIN Transmitter acts like a slew-controlled level shifter. A dominant state (low) on TX leads to the LIN bus being pulled low (dominant state) too. The TX pin has an internal active pull up connected to VCC. This guarantees that an open TX pin generates a recessive BUS level.

Figure 9. TX Input Circuitry



Output RX.

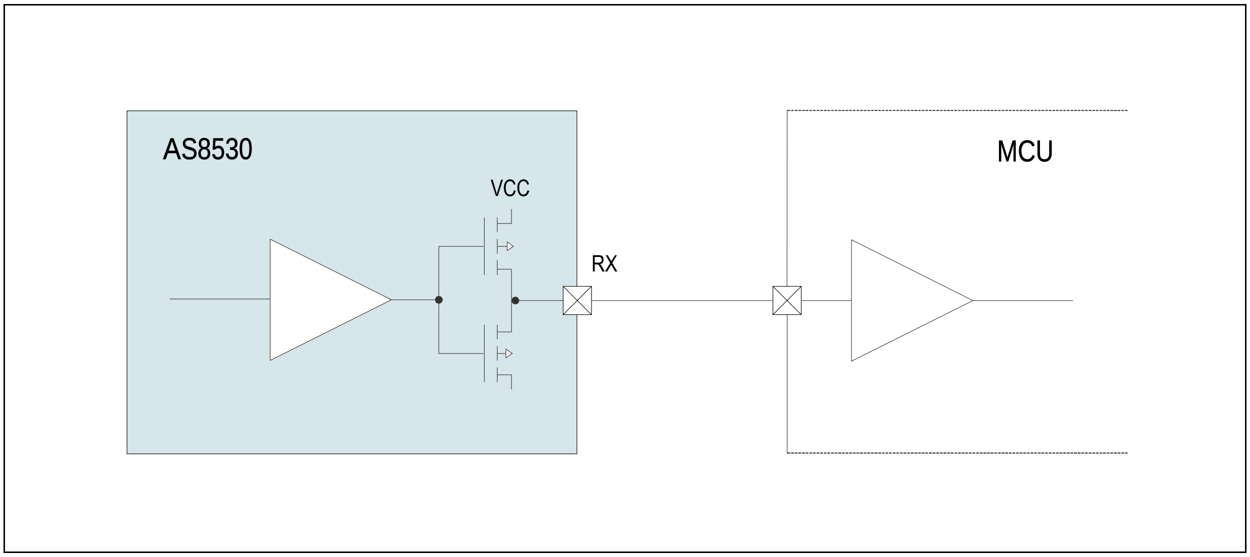
The received BUS signal will be output to the RX pin:

BUS < Vthr_cnt – 0.5 * Vthr_hys → RX = low

BUS > Vthr_cnt + 0.5 * Vthr_hys → RX = high

This output is a push-pull driver between VCC and GND with an output current of 1mA.

Figure 10. RX Output Circuitry

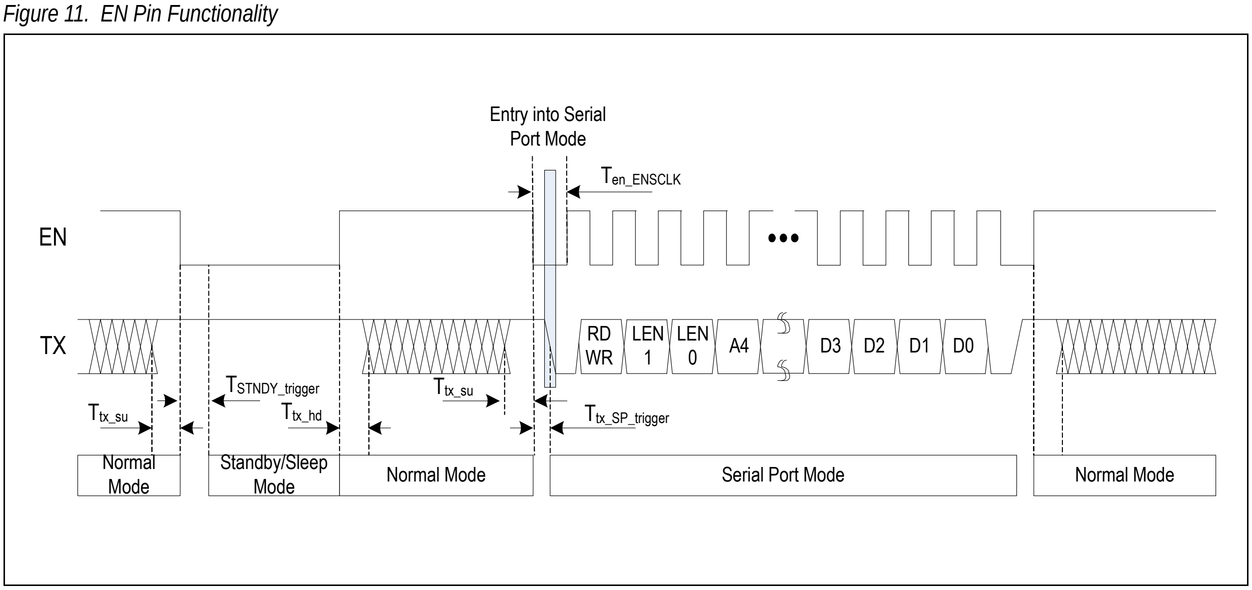


8.6 MODE Input EN

The AS8530 is switched from normal mode to the standby/sleep mode with a falling edge on EN and keeping TX high for $T_{STNDY\_trigger}$ time. Device is switched from standby mode to normal mode with a rising edge at the EN pin. The mode change for AS8530 with a falling edge at EN can be done independently from the state of the bus transceiver. Device enters into Serial port mode by forcing EN low and driving TX high to low within $T_{tx\_SP\_trigger}$ time after EN forced to low.

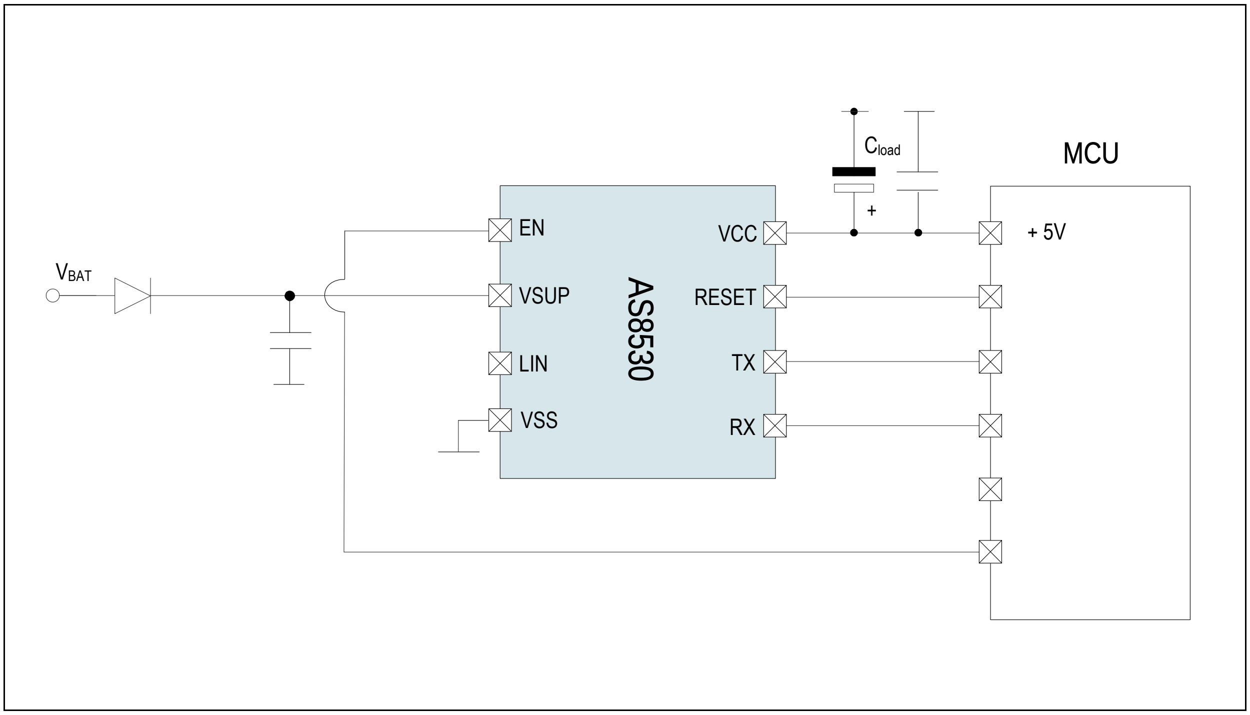
This ensures the direct control of device to enter into Standby/Sleep mode by microcontroller using EN pin.

Figure 11. EN Pin Functionality



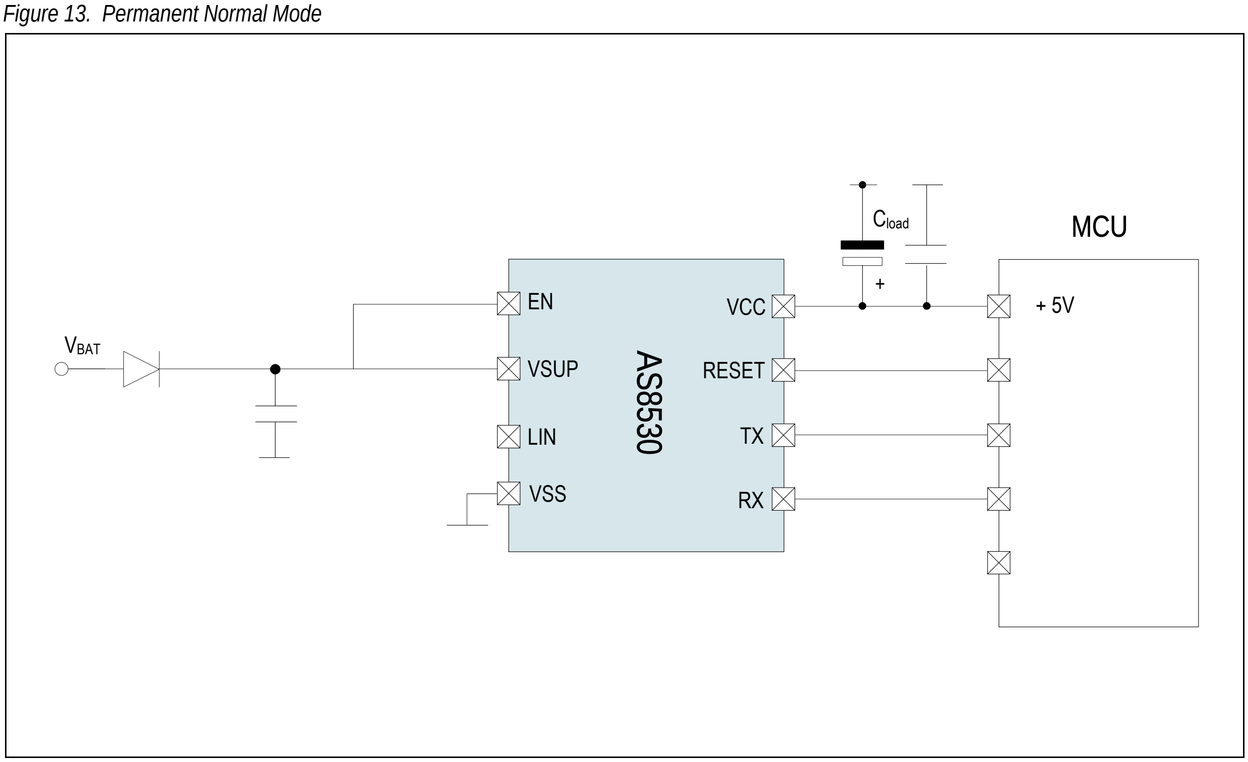
The EN input has an internal active pull down to secure that if this pin is not connected, a low level will be generated.

Figure 12. Enable Controlled via. MCU



If the application doesn't need the wake up capability of the AS8530, a direct connection EN to VCC is possible. In this case the AS8530 operates in permanent normal mode. Also possible is the external (outside of the module) control of the EN line via. VSUP signal as shown below.

Figure 13. Permanent Normal Mode



8.7 Serial Port Interface

The interface is essentially used to trigger the window watchdog, to access test mode and read out diagnostic information for the AS8530. The description of this interface and the protocol is explained below. Information on block status and errors can be displayed by diagnosis registers.

8.7.1 Device Configuration using 2-Wire Serial Port

The AS8530 device configuration register is programmed via a 2-wire Serial Programming Interface. EN/SCL is used as Serial Clock and TX/SDA_IO is used as Serial Data. EN is used as clock input to access serial port registers in serial port mode. Also EN is used to control transition from normal mode to standby/sleep mode. The TX input of the device will be multiplexed as following:

- LIN TX for transmitting data from microcontroller on LIN bus
- SDA_IO for Serial data input/output, this will be used for serially accessing data from configuration and status register

SP Frame. A frame is formed by first byte for command and address/configuration and following bit stream that can be formed by an integer number of bytes. Command is coded RD/WR on the first bits, length of the transfer is indicated by LEN1, LEN2 bits while address is given on LSB 5 bits.

Table 6. Command Bits

Command Bits			Register Address or Transmission Configuration				
RD/WR	LEN1	LEN2	A4	A3	A2	A1	A0

RD/WR	Command	<A4:A0>	Description
0	WRITE	ADDRESS	Writes data byte on the given starting address.
1	READ	ADDRESS	Read data byte from the given starting address.

Table 7. Transfer Length

LEN1	LEN2	Length	Description
0	0	1	Transfer consists of single Data phase. After completion of single Data phase device comes out of Serial port interface.
0	1	2	Transfer consist of two Data phase.
1	0	4	Transfer consist of four Data phase.
1	1	8	Transfer consist of eight Data phase.

Write Command. For Write command RD/WR = 0

After the command code, length of the transfer is send in next two bits, the address of register to be written has to be provided from the MSB to the LSB. Then one, two, four, or eight data bytes can be transferred from the MSB to the LSB. For each data byte following the first one, used address is the incremented value of the previously written address. Each bit of the frame has to be driven by the 2-Wire SP master on the SP clock (EN pin) positive edge and the 2-Wire SP slave (device) samples this bit on the next SP clock (EN pin) negative edge. In the following figures two examples of write command (without and with address self-increment).

Figure 14. Protocol for Serial Data Write with Length = 1

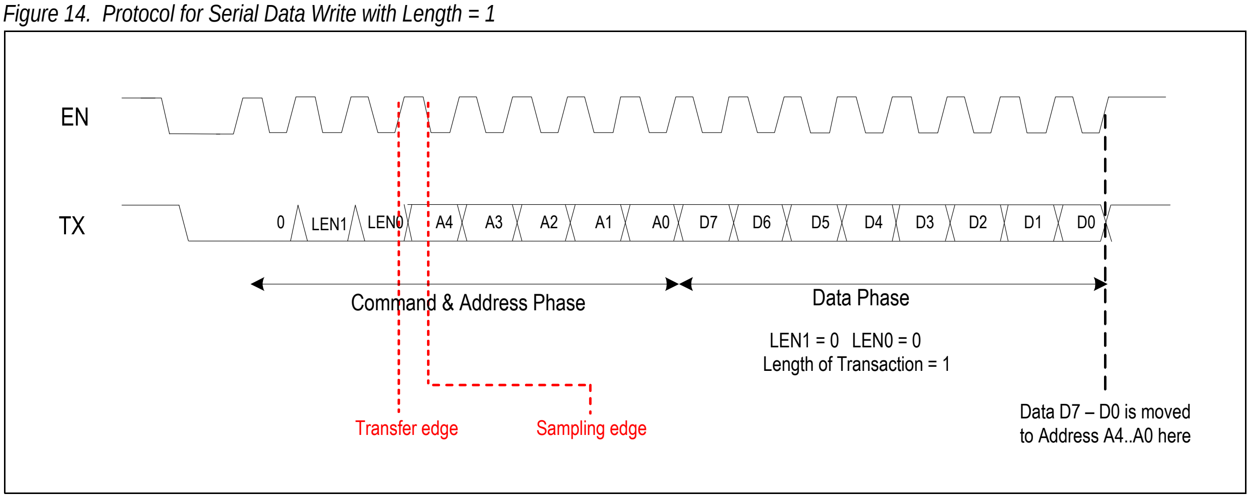
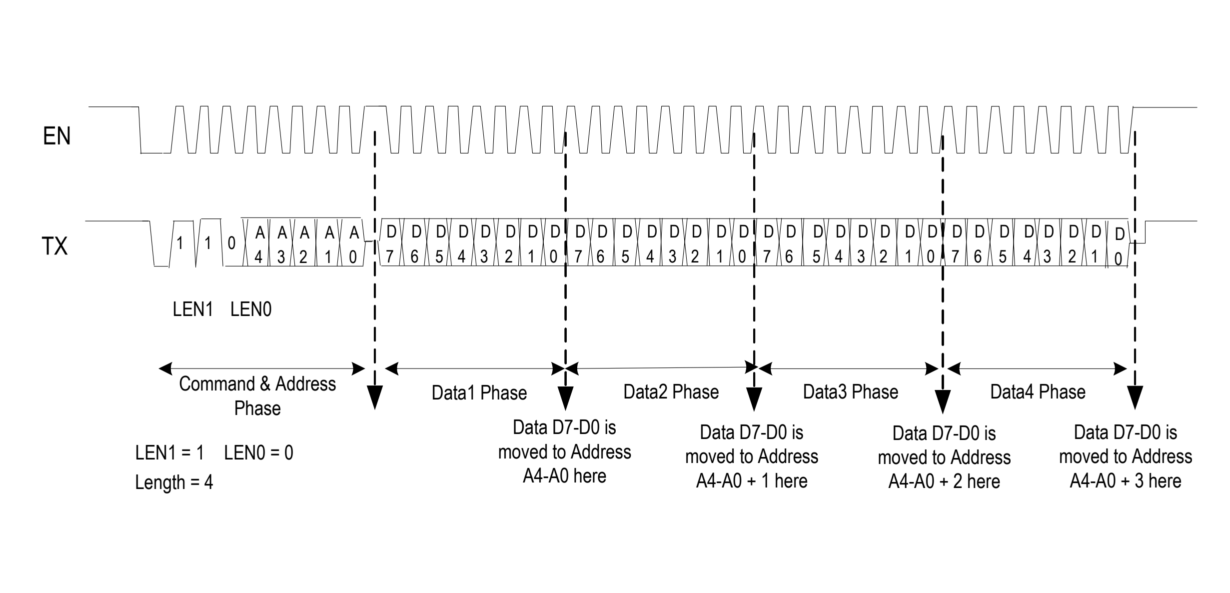


Figure 15. Protocol for Serial Data Write with Length = 4



Read Command. For Read command RD/WR=1.

After the command code, length of the transfer is send in next two bits, the address of register to be read has to be provided from the MSB to the LSB. Then one, two, four or eight data bytes can be transferred from the SPI slave to the master, always from the MSB to the LSB.

Each bit of the command and address sections of the frame have to be driven by the 2-Wire SP master on the SP clock (EN pin) positive edge and the 2-Wire SP slave (device) samples this bit on the next SP clock (EN pin) negative edge. Each bit of the data phase of the frame has to be driven by the 2-Wire SP slave (device) on the SP clock (EN pin) positive edge and the 2-Wire SP master samples this bit on the next SP clock (EN pin) negative edge. The following figures illustrate two examples of read command (without and with address self-increment.)

Figure 16. Protocol for Serial Data Read with Length = 1

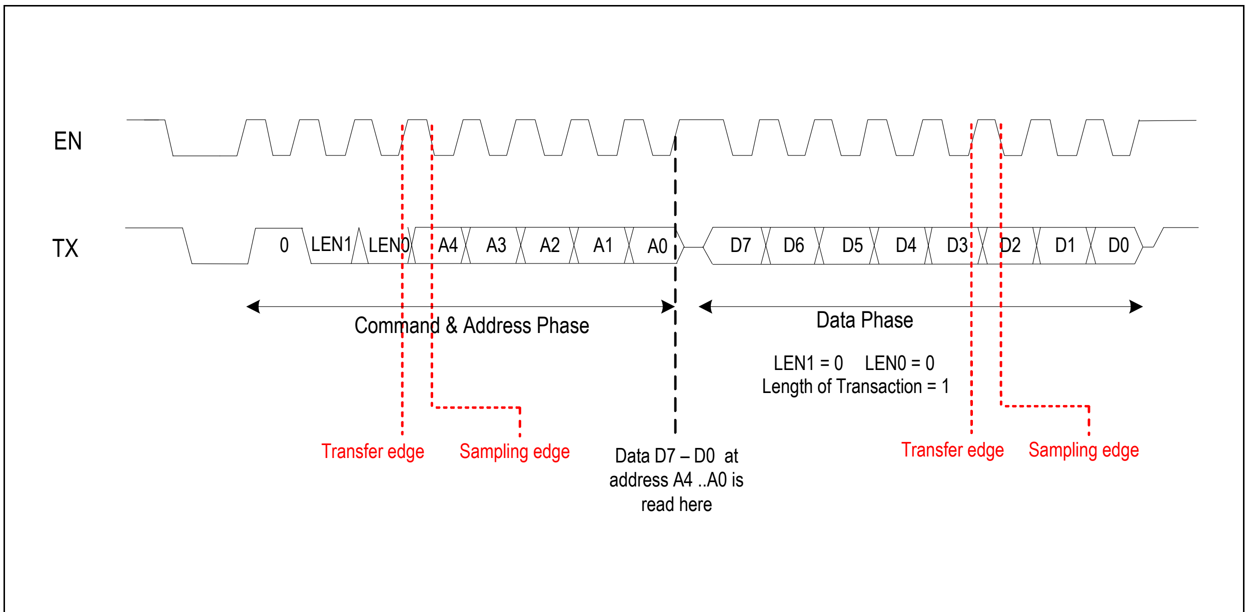
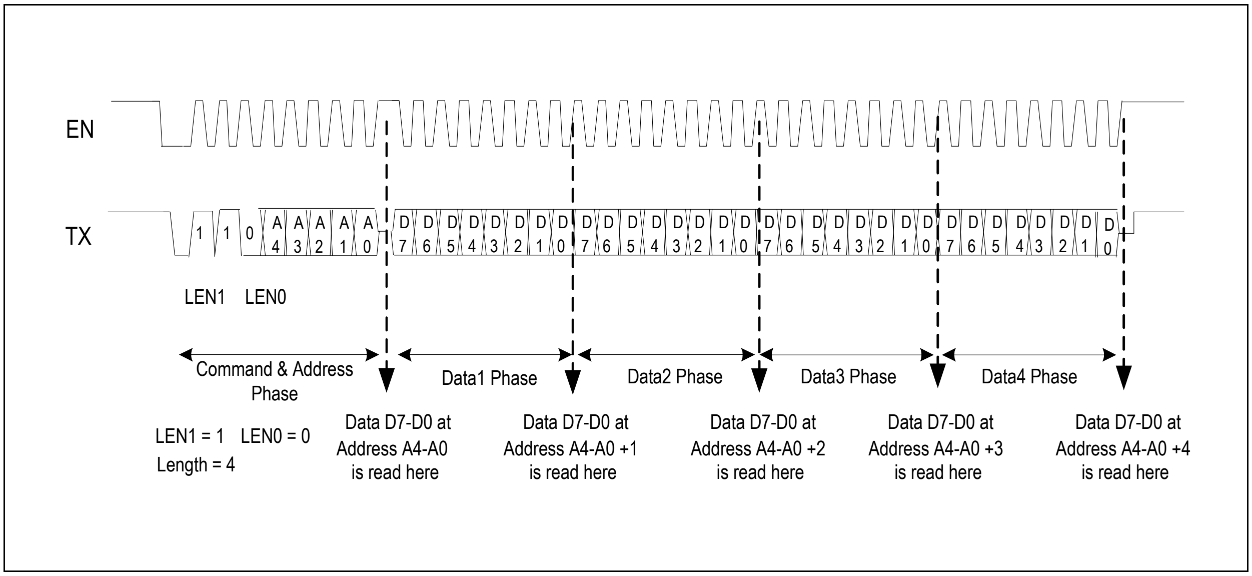


Figure 17. Protocol for Serial Data Read with Length = 4



Timing. The following figures illustrate timing waveforms and parameters.

Figure 18. Timing for Writing

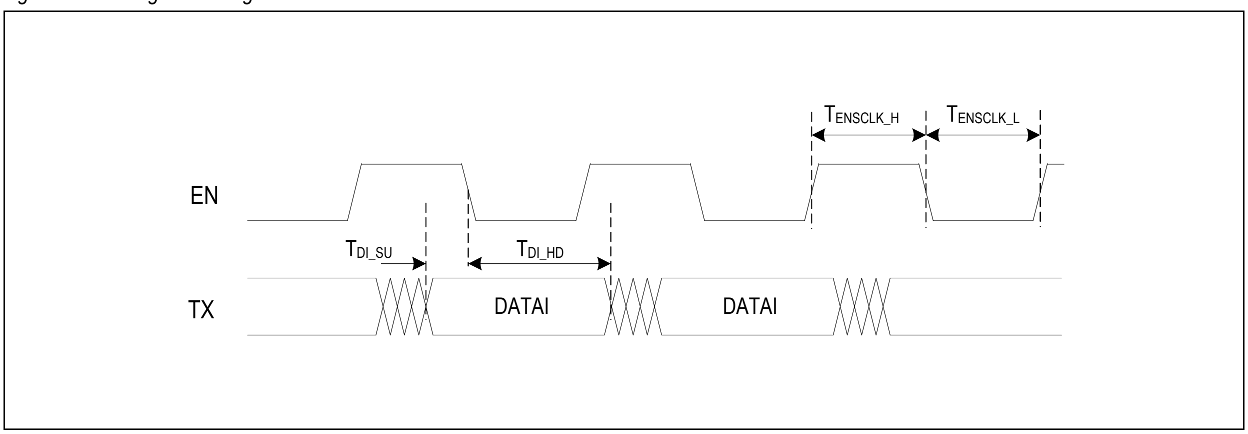
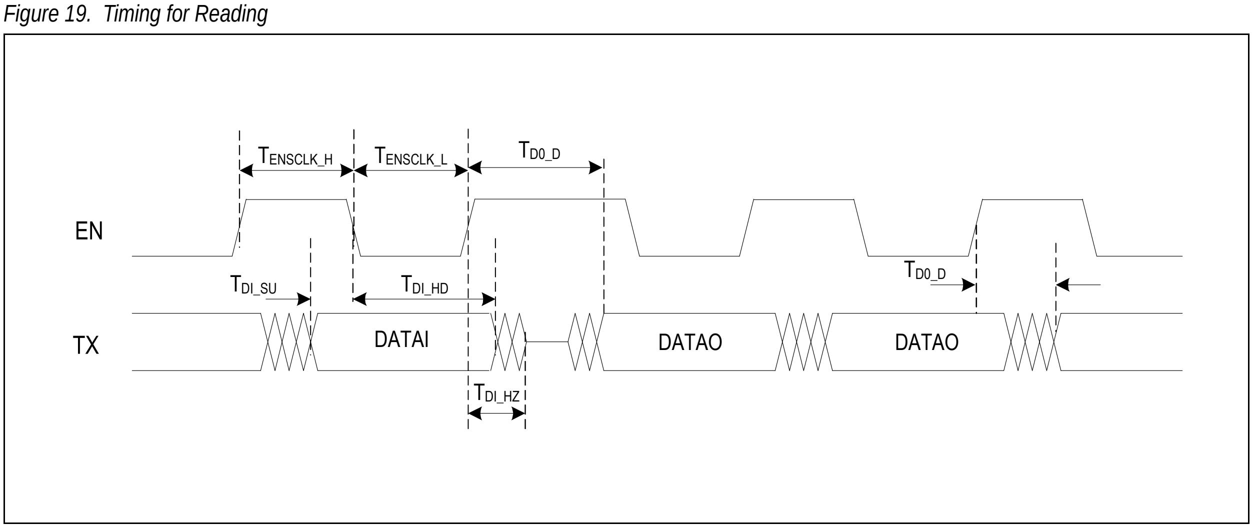


Figure 19. Timing for Reading



8.8 Control and Diagnosis Registers

The serial interface can be used as interface between the ASSP AS8530 and an external micro-controller. The interface is a slave and only the micro-controller can start the communication. This interface will be used for device configuration, entering into test mode and carrying out diagnostic options. Refer to Table 8 for details on the configuration registers.

8.8.1 Definition of Control and Status Registers

A total of 32 control, diagnosis and test registers, each of 8-bit can be accessed using the 2-wire serial interface. Table 8 provides a description of all control and status registers.

Table 8. Configuration Registers

Address	Register Name	POR Value	RD / WR	Description	
Control and Configuration Register					
0 x 03	Device Configuration Register	On POR_VCC 0000_1111	RD / WR	D0 Reserved	
				D1 Reserved	
				D2 Reserved	
				D3 Enable / Disable LIN Transceiver	
				0	Disabled
				1	Enabled
				D7…D4 Reserved	
0 x 04	Device Control Register	On POR_VSUP 0000_0001	RD / WR	D7... D1 Reserved	
0 x 05	Temporary Shutdown Register	On POR_VCC 0000_0000	RD / WR	D0 Temporary shutdown control bit	
				0	No Temporary shutdown
				1	Enter into Temporary shutdown
				D7…D1 Reserved	
0 x 06	Window Watch Dog Trigger Register	On POR_VCC 0000_0000	WR	D0 Window Watch Dog Trigger	
				This bit will be set by MCU to indicate trigger event. If this trigger occurs outside the Window of Watch dog counter, then RESET signal is asserted. Also on this trigger WWD counter is restarted and this bit will be cleared internally within 2 cycles of 128KHz clock.	
				D7 … D1 Reserved	
0 x 07	Low Side Driver Data Register	On POR_VCC 0000_0000	RD / WR	D7 … D0 Reserved	

Table 8. Configuration Registers

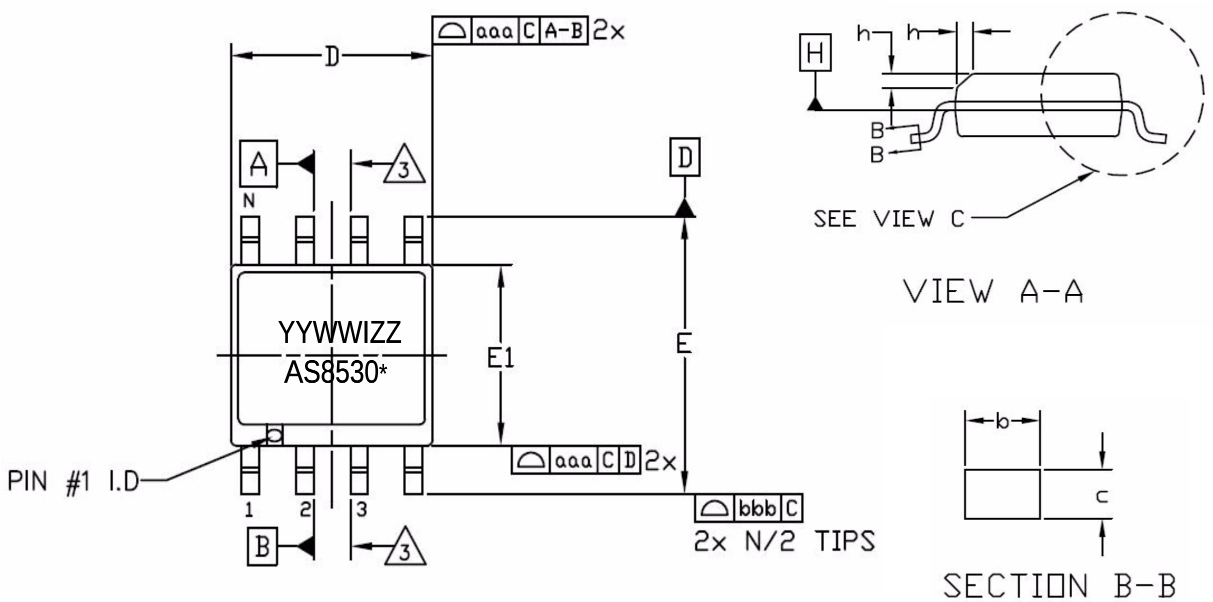
Address	Register Name	POR Value	RD / WR	Description
Diagnosis Register				
0 x 08	Diagnostic Register 1	On POR_VSUP 0000_0011	RD	D7..D0 = DR[7:0] 8 LSB bits of the 24 bit Diagnostic Register
				D0 PORVSUP (set when VSUP < Vsuvr_on, cleared after µC read)
				D1 UVVCC Under voltage VCC (set when VCC < Vuvr_on, cleared after µC read)
				D2 OTEMP160 Over-temperature Reset. (set when temp > T_{sd}, cleared after µC read)
				D3 OTEMP140 Over-temperature warning (set when temp > T_{otset}, cleared after µC read)
				D4 OVVBAT Overvoltage VBAT. (set when VSUP > Vovthh, cleared after µC read)
				D5 Reserved
				D6 RWAKE Remote Wakeup (set on Remote Wakeup event on LIN Bus, cleared after µC read)
				D7 WWDT Window watchdog timeout. (set on failure of Window watchdog timeout, cleared after µC read)
0 x 09	Diagnostic Register 2	On POR_VSUP 0000_0000	RD	D7..D0 = DR[15:8] next 8 LSB bits of the 24 bit Diagnostic Register.
				D0 TXTIMEOUT Tx timeout of 1sec. (set on TX low > 1sec, cleared after µC read)
				D1 TEMPSHUT this bit is set on entering into temporary shutdown state and cleared after µC read.
				D7 D2 Reserved

Note: When the device is powered ON @ ambient temperature of 125ºC, the status of the OVTEMP140 can be HIGH indicating an over temperature warning. This is because 125ºC is within the limits for the OVTEMP140.

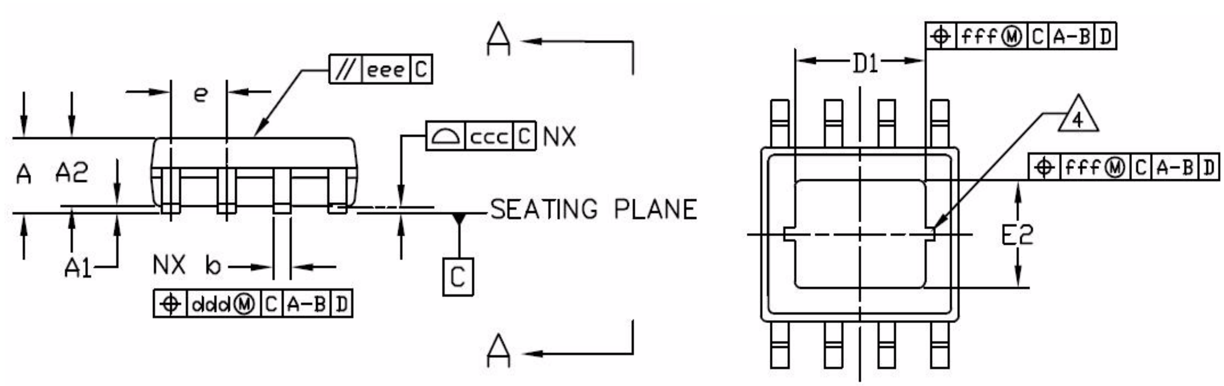
9 Package Drawings and Markings

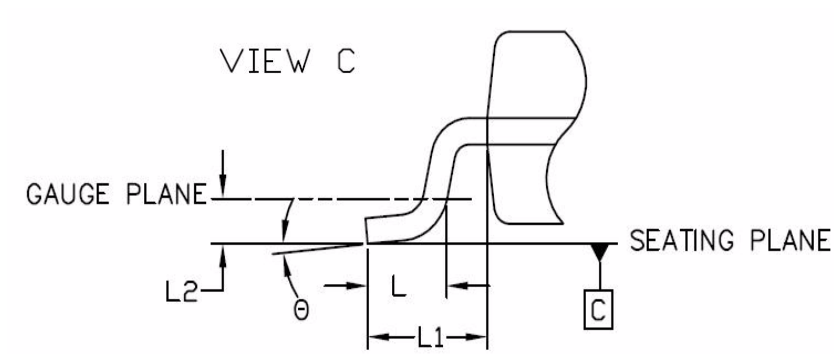
The device is available in a ep-SOIC8 package.

Figure 20. Drawings and Dimensions



* The device marking for the VCC=5V option will change to AS8530A.





Symbol	Min	Nom	Max
A	-	-	1.70
A1	0.00	-	0.15
A2	1.25	-	-
b	0.31	-	0.51
c	0.17	-	0.25
D	-	4.90 BSC	-
D1	2.24	3.10	3.20
E	-	6.00 BSC	-
E1	-	3.90 BSC	-
E2	1.55	2.41	2.51
e	-	1.27 BSC	-
L	0.41	0.64	0.89

Symbol	Min	Nom	Max
L1	-	1.04 REF	-
L2	-	0.25 BSC	-
h	0.25	-	0.50
θ	0º	-	8º
aaa	-	0.10	-
bbb	-	0.20	-
ccc	-	0.10	-
ddd	-	0.25	-
eee	-	0.10	-
fff	-	0.15	-
N	8		

Notes:

1. Dimensions and tolerancing conform to *ASME Y14.5M -1994*.
2. All dimensions are in miilimeters. Angles are in degrees.
3. Datums A and B to be determined at datum H.
4. Extrusion of exposed area in bottom side is 0.20mm typical.

Marking: YYWWIZZ.

YY	WW	I	ZZ
Last two digits of the manufacturing year	Manufacturing Week	Plant Identifier	Traceability Code

Revision History

Revision	Date	Owner	Description
1.0	26 Nov, 2010	mbl	Initial release
	29 Nov, 2010	kpt	Marking details updated under Ordering Information.
1.1	03 Jun, 2011	mbl	Updated Package Drawings and Markings, Ordering Information.
	Dec 31, 2012	sju	Updated ordering table.

Note: Typos may not be explicitly mentioned under revision history.

10 Ordering Information

The devices are available as the standard products shown in Table 9.

Table 9. Ordering Information[1]

Ordering Code	Description	Delivery Form	Package
AS8530-ASOP	LIN Transceiver with Integrated Voltage Regulator and MCU Interface (3.3V Version)[2]	Tape and Reel (2500 pcs)	SOIC-8
AS8530-ASOM		Tape and Reel (500 pcs)	SOIC-8

1. For both product versions, the RESET delay time t_{Res} as well as undervoltage threshold are set to default value and window watchdog is disabled. On special request, optional factory settings can be made available on specific vendor addendum.
2. Also available as 5V version.

Note: All products are RoHS compliant and ams green.
Buy our products or get free samples online at www.ams.com/ICdirect

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