Am2864A

8192 x 8 Electrically Erasable PROM

DISTINCTIVE CHARACTERISTICS

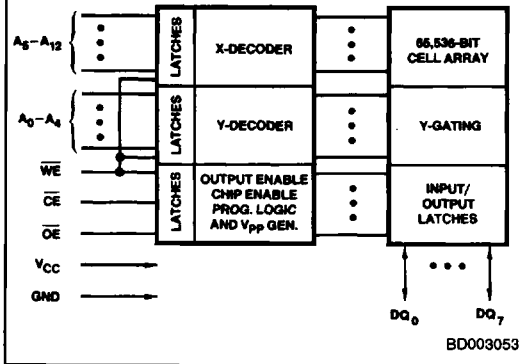
- 5-V only operation
- Military temperature range available
- Self-timed Write Cycle with on-chip latches
- $\overline{\text{Data}}$ Polling for end-of-write indication
- Data protection features to prevent writes from occurring during V_{CC} power-up/down
- 32-byte page write mode
- Minimum endurance of 10,000 write cycles per byte with a 10-year retention. For detailed information, see the Am9864 Reliability Report (PID #06891A).

GENERAL DESCRIPTION

The Am2864A is a 65,536-bit Electrically Erasable Programmable Read-Only Memory (EEPROM), organized as 8192 words by 8 bits per word. It operates from a single 5-volt supply and has a fully self timed write cycle with address, data and control lines latched during the write operation. The 32-byte page write mode allows programming in as little as 2.8 seconds. The Am2864A is fabricated on AMD's highly manufacturable N-Channel Silicon gate process, and uses AMD's proprietary EEPROM technology to achieve the electrically alterable nonvolatile storage. This technology employs the industry-accepted accepted Fowler-Nordheim tunneling across a thin oxide.

The Am2864A provides on-chip the logic necessary to interface with most microprocessors. The latched inputs and self-timed write cycle free the microprocessor to perform other tasks during a write. A transparent automatic erase before write enhances system performance.

BLOCK DIAGRAM



BD003053

MODE SELECT TABLE

Inputs			Outputs		
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	A_9	Mode
L	L	H	Data Out	X	Read
L	H	⊓	Data In	X	Write
H	X	X	Hi-Z	X	Standby
L	H	H	Hi-Z	X	Read Inhibit
X	L	X	–	X	Write Inhibit
L	L	H	Code	V_H	Auto Select
L	L	H	$\overline{D_{IN}}$	X	$\overline{\text{Data}}$ Polling

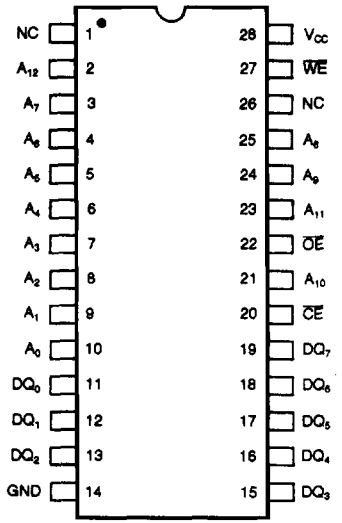
V_H = 12.0 V ± .5 V
H = HIGH
L = LOW
X = Don't Care
⊓ = Pulse

PRODUCT SELECTOR GUIDE

Part Number	Am2864A-2	Am2864A-20	Am2864A	Am2864A-25	Am2864A-3	Am2864A-30	Am2864A-355	Am2864A-35
Maximum Access Time	200 ns		250 ns		300 ns		350 ns	
V_{CC} Supply Tolerance	±5%	±10%	±5%	±10%	±5%	±10%	±5%	±10%

Publication # 08085 Rev. A Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View



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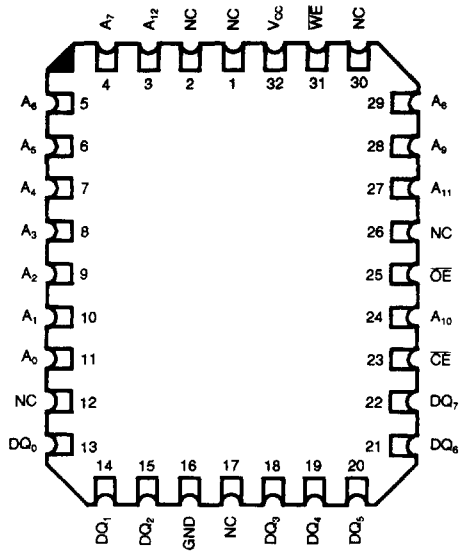

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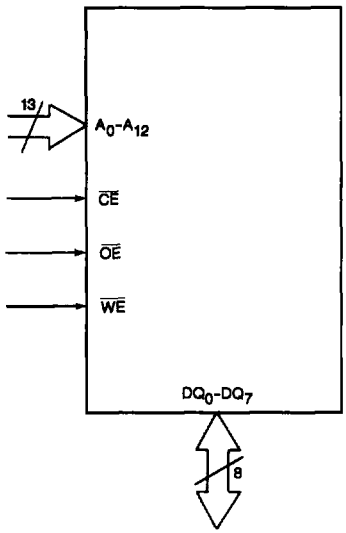
Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



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VCC = Power Supply
GND = Ground

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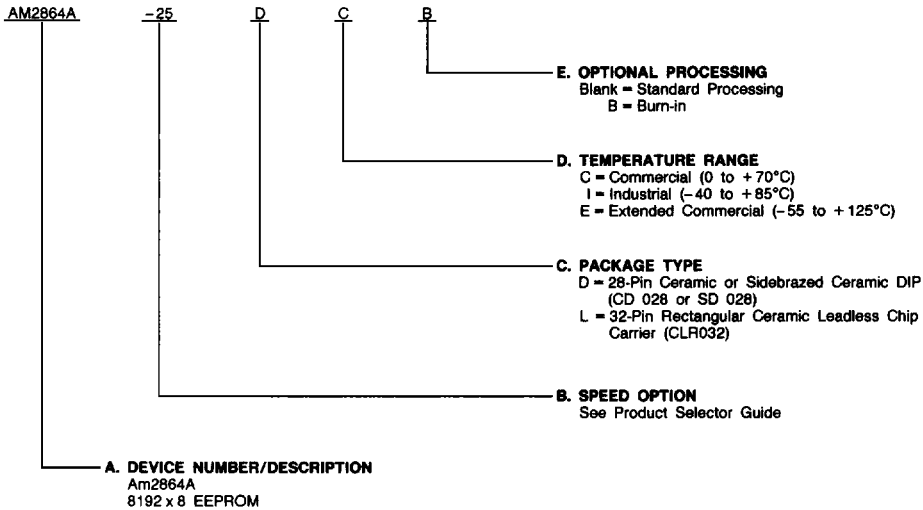
ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM2864A-2	DC, DCB, DI, DIB, DE, DEB, LC, LCB, LI, LIB, LE, LEB
AM2864A-20	
AM2864A	
AM2864A-25	
AM2864A-3	
AM2864A-30	
AM2864A-355	
AM2864A-35	

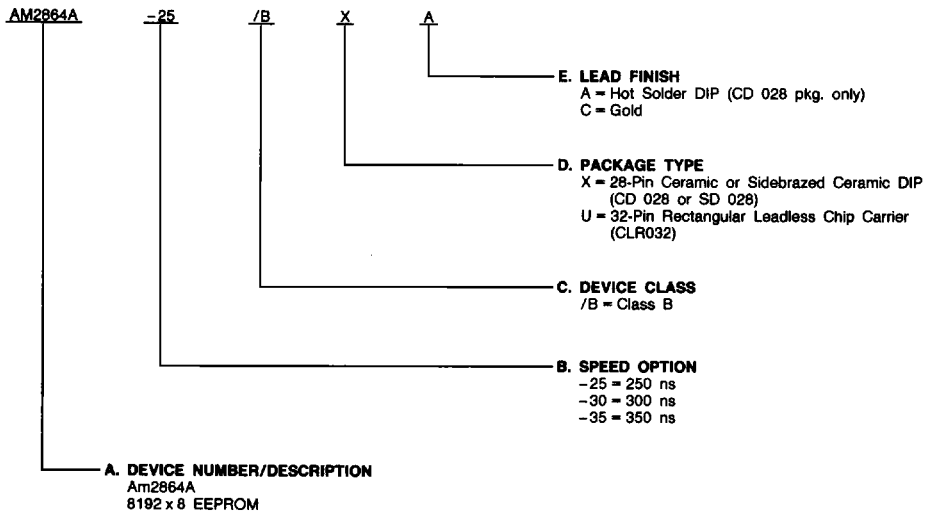
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM2864A-25	/BXA, /BXC, /BUC
AM2864A-30	
AM2864A-35	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

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FUNCTIONAL DESCRIPTION

Read Mode

The Am2864A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least t_{ACC}-t_{OE}.

Standby Mode

The Am2864A has a standby mode which reduces the active power dissipation by 60%, from 525 mW to 210 mW (V_{CC} ±5% values for 0 to 70°C). The Am2864A is placed in the standby mode by applying a TTL HIGH signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Data Protection

The Am2864A incorporates several features that prevent unwanted write cycles during V_{CC} power-up and power-down. These features protect the integrity of the stored data.

To avoid the initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than 3.3 volts (typical 3.8 V). It is the users's responsibility to insure that the control levels are logically correct when V_{CC} is above 3.3 volts.

There is a $\overline{WE}$ lockout circuit that prevents $\overline{WE}$ pulses of less than 20 ns duration from initiating a write cycle.

When the $\overline{OE}$ control is in logic zero condition, a write cycle cannot be initiated.

Page Write Mode

The page write allows from 1 to 32 bytes of data to be written into the EEPROM in a single write cycle. The page write mode consists of a load sequence followed by an automatic write sequence.

During the load portion, sequential $\overline{WE}$ pulses load the byte address and the byte data into a 32-byte register. The bytes can be loaded into this register in any order. On each $\overline{WE}$ pulse, the "Y" address is latched on the falling edge of the $\overline{WE}$, the data input is latched on the rising edge of $\overline{WE}$, and the page address (A_5-A_{12}) is latched on the falling edge of the last $\overline{WE}$. Note that for a write to occur, $\overline{CE}$ and $\overline{WE}$ must be LOW and $\overline{OE}$ must be HIGH. The load portion of the page write is complete when all the data (up to 32 bytes) is loaded into the register.

The automatic write portion starts t_{WW} after each transition of $\overline{WE}$ from LOW-to-HIGH. If $\overline{WE}$ transitions from HIGH-to-LOW before t_{WW} minimum (100 µs), the timer is reset and the automatic write portion does not start. This is how the bytes are loaded into the register. If $\overline{WE}$ is held LOW, this t_{WW} timer never starts and the write cycle is held indefinitely.

If $\overline{WE}$ transitions from LOW-to-HIGH and stays HIGH for at least t_{WW} maximum, then the automatic write sequence is initiated. Note that the load sequence can also be terminated if $\overline{OE}$ goes LOW. Once $\overline{OE}$ is LOW, further attempts to load will be ignored and the part will time out (t_{WW}) and enter the automatic write sequence.

The automatic write sequence consists of an erase cycle, which erases any data that existed in each addressed cell, and a write cycle, which puts data back into the erased cells. Note that a page write will only write data to the locations being addressed and will not rewrite the entire page.

Byte Mode Write

When $\overline{WE}$ is toggled once, the Am2864A operates in the byte mode. A single byte is loaded into the register and after $\overline{WE}$ goes HIGH and t_{WW} is satisfied, the automatic write cycle starts. It is in this mode that the Am2864A is identical to the Am2864B and Am9864.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EEPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional at 25°C ±5°C ambient temperature.

To activate this mode, programming equipment must force 11.5 V to 12.5 V on address line A_9 of the Am2864A. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code and byte 1 ($A_0 = V_{IH}$) the device identifier code. For the Am2864A, these two identifier bytes are given in Table 1. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (O_7) defined as the parity bit. The auto select code for the Am2864A is identical to the Am2864B.

Output OR-Tieing

To accommodate multiple memory connections, a 2-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the read line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

$\overline{\text{Data}}$ Polling

This feature makes the Am2864A highly flexible. It allows the designer the option of a software polling technique for end of write indication. $\overline{\text{Data}}$ Polling requires a simple software routine that performs a read operation when the chip is in the automatic write mode. The data that becomes valid during this $\overline{\text{Data}}$ Polling read is the inverse of all 8 bits, last written to the outputs. The true data ($DQ_0 - DQ_7$) will become valid when the automatic write has been completed. Note that all 8 bits invert during $\overline{\text{Data}}$ Polling, thereby giving the user more flexibility during design and layout.

Chip Clear Mode (Military only)

Another feature included on AMD's Am2864A for military applications is a single-pulse chip erase. This optional mode allows the user to program all bits to a logic ONE with a single 10-ms write pulse. Additional information is available from AMD regarding this test mode — consult the local AMD sales *office.*

Endurance

Since endurance testing is a destructive test it is sampled and not 100% tested. To test for endurance, a sample of devices are written 10,000 times and checked for data retention capability.

There is one main failure mechanism associated with endurance failures in EEPROMs. This failure mechanism is due to charge trapping in the thin tunneling dielectric. At a point, when the amount of trapped charge creates an electric field that exceeds the dielectric breakdown of the oxide, the oxide becomes conductive, and reliable storage of charge on the floating gate is no longer possible. This results in the failure of a single bit to properly write and retain data.

There are three different failure rates associated with this failure mechanism, and the failure rates are a function of the number of write cycles. For less than a few hundred write cycles, the failure rate is relatively high. During AMD testing, each part is written hundreds of times to allow those cells that would be infant-mortality failures to be screened out. For the next 20,000 to 30,000 write cycles the failure rate is low. It is in this region that AMD EEPROMs are operated. Somewhere above this region, typically well above the guarantee of 10^4 total write cycles, the failure rate again starts increasing.

The endurance failure rate is a function of the number of write cycles that the part has experienced. All parts that pass the AMD test screens will write a minimum of 10,000 times at every byte location with a maximum failure rate of 5%. In other words, 5% of a sample of devices will fail to write or to retain information after write if they are written 10,000 times. Those devices that fail will typically have a single bit that fails to retain the correct data after being written. This failure rate is measured from a sample of devices, in the same manner that other reliability failure mechanisms are measured.

For more detailed information on how this data was obtained please refer to the Am9864 Reliability Report (PID#06891A).

APPLICATIONS

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. A 0.1 μF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EEPROM arrays, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

PROGRAMMING

TABLE 1. IDENTIFIER BYTES (Notes 1, 2 & 3)

Identifier	A_0	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0	Hex
Manufacturer Code	V_{IL}	0	0	0	0	0	0	0	1	01
Device Code	V_{IH}	1	0	0	0	1	0	1	0	8A

Legend: 1 = HIGH
0 = LOW

Notes: 1. $A_9 = 12.0\ V \pm 0.5\ V$
2. $A_1 - A_8$, $A_{10} - A_{12}$, $\overline{CE}$, $\overline{OE} = V_{IL}$
3. $\overline{WE} = V_{IH}$

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ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with Power Applied . −65 to +135°C
Voltage on All Inputs with Respect to GND ..... +6.50 to −0.6 V
Voltage on A_9 with Respect to GND ..... +13.5 to −0.6 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_C) ..... 0 to +70°C
Supply Voltage (V_{CC} ±5%) ..... +4.75 to +5.25 V
(V_{CC} ±10%) ..... +4.50 to +5.50 V

Industrial (I) Devices
Temperature (T_C) ..... −40 to +85°C
Supply Voltage (V_{CC} ±5%) ..... +4.75 to +5.25 V
(V_{CC} ±10%) ..... +4.50 to +5.50 V

Extended Commercial (E) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC} ±10%) ..... +4.50 to +5.50 V

Military (M) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC} ±10%) ..... +4.50 to +5.50 V

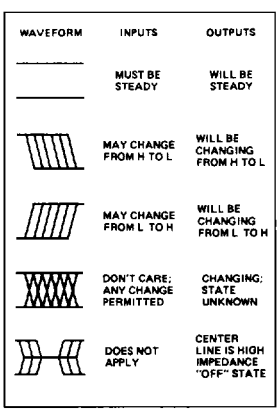
Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
I_{LI}	Input Leakage Current	V_{IN} = 0 to 5.5 V			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 to 5.5 V			10	µA
I_{CC1}	V_{CC} Current (Standby)	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}			40	mA
I_{CC2}	V_{CC} Current (Active)	$\overline{OE}$ = $\overline{CE}$ = V_{IL}			100	mA
I_{CC}	V_{CC} Current (Write)	$\overline{WE}$ = ⌐¬, $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}			100	mA
V_{IL}	Input LOW Voltage		−0.1		.8	Volts
V_{IH}	Input HIGH Voltage		2.0		V_{CC}+1	Volts
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			.45	Volts
V_{OH}	Output HIGH Voltage	I_{OH} = −400 µA	2.4			Volts
C_{IN}	Input Capacitance (Note 1, 2)	V_{IN} = 0 V		4	10	pF
C_{OUT}	Output Capacitance (Note 1, 2)	$\overline{OE}$ = $\overline{CE}$ = V_{IH}, V_{OUT} = 0 V		8	12	pF
V_{WI}	Write Inhibit Voltage		3.3	3.8		Volts

Notes: 1. This parameter is sampled on a periodic basis and not 100% tested.
2. Freq. = 1 MHz @ 25°C.
3. Typical values are for nominal supply voltages.
*See the last page of this spec for Group A Subgroup Testing information.

KEY TO SWITCHING WAVEFORMS



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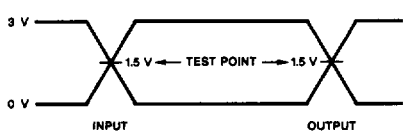
SWITCHING TEST WAVEFORM



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AC Testing: Input are driven at 3 V for logic "1" and 0 V for logic "0." Timing measurements are made at 1.5 V . Input pulse rise and fall times are 10 ns.

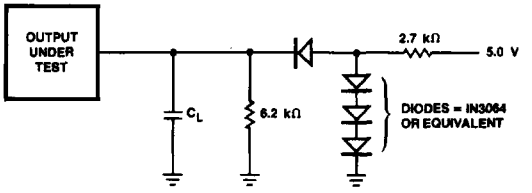
SWITCHING TEST CIRCUIT

Switching Test Conditions

Output load: 1 TTL gate and C_L = 100 pF
Input pulse levels: 0 V to 3.0 V

Timing Measurement Reference Levels

Input: 1.5 V
Output: 1.5 V



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C_L = 100 pF, including jig capacitance.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

No.	Parameter Symbol	Parameter Description	Test Conditions	Am2864A-2, Am2864A-20 Min.	Am2864A-2, Am2864A-20 Max.	Am2864A, Am2864A-25 Min.	Am2864A, Am2864A-25 Max.	Am2864A-3, Am2864A-30 Min.	Am2864A-3, Am2864A-30 Max.	Am2864A-355, Am2864A-35 Min.	Am2864A-355, Am2864A-35 Max.	Units
READ												
1	t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		200		250		300		350	ns
2	t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		200		250		300		350	ns
3	t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$		100		100		110		120	ns
4	t_{DF} (Note 1)	Output Enable HIGH to Output Float	$\overline{CE} = V_{IL}$	0	60	0	60		80	0	80	ns
5	t_{OH} (Note 1)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns
WRITE												
6	t_{AS}	Address to Write Setup Time		20		20		20		60		ns
7	t_{CS}	$\overline{CE}$ to Write Setup Time		0		0		0		0		ns
8	t_{WP}	Write Pulse Width		100		100		120		150		ns
9	t_{AH}	Address Hold Time		80		80		80		100		ns
10	t_{DS}	Data Setup Time		50		50		50		70		ns
11	t_{DH}	Data Hold Time		30		30		30		30		ns
12	t_{CH}	$\overline{CE}$ Hold Time		0		0		0		0		ns
13	t_{OES}	$\overline{OE}$ Setup Time		0		0		0		0		ns
14	t_{OEH}	$\overline{OE}$ Hold Time		0		0		0		0		ns
15	t_{WC}	$\overline{WE}$ Cycle Time		1		1		1		1		μs
16	t_{WW}	Page Write Window (Note 3)		100	500	100	500	100	500	100	1000	μs
17	t_{WH}	$\overline{WE}$ Hold Time		250		250		250		300		ns
18	t_{WB}	Byte Write Cycle			10		10		10		12	ms
19	t_{RED}	Write Recovery from $\overline{Data}$ Polling Time		20		20		20		20		μs
	(Notes 1 & 2)	Number of Writes per Byte		10		10		10		10		x1000

Notes: 1. This parameter is sampled and is not 100% tested.
2. See Am9864 Reliability Report.
3. A timer of t_{WW} duration starts at every LOW-to-HIGH transition of $\overline{WE}$. If it is allowed to time out, a page load will start. A transition of $\overline{WE}$ from HIGH-to-LOW will stop the timer.

*See the last page of this spec for Group A Subgroup Testing information.

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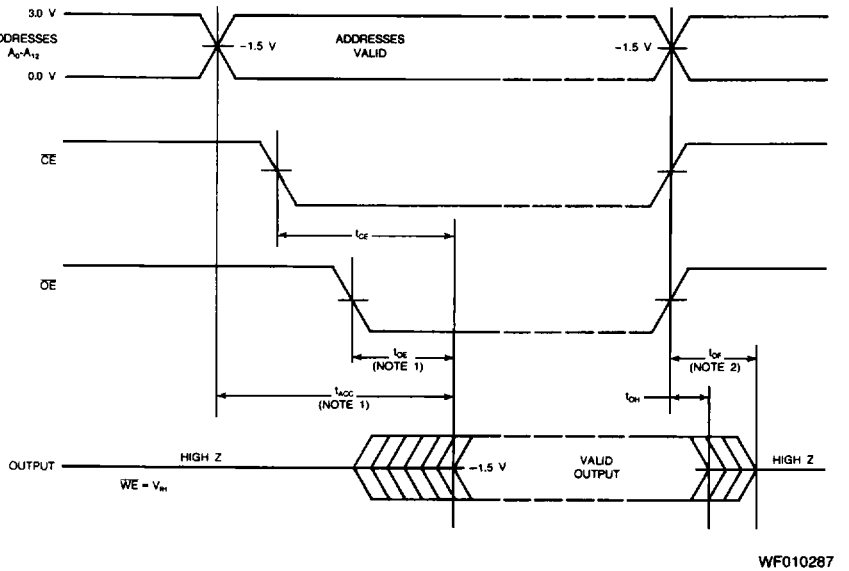
SWITCHING WAVEFORMS (Cont'd.)



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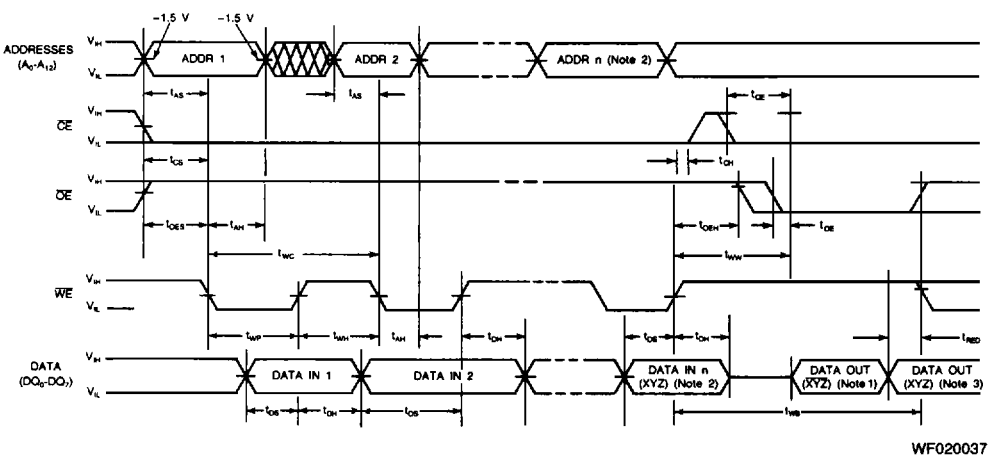
Read

Notes: 1. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.



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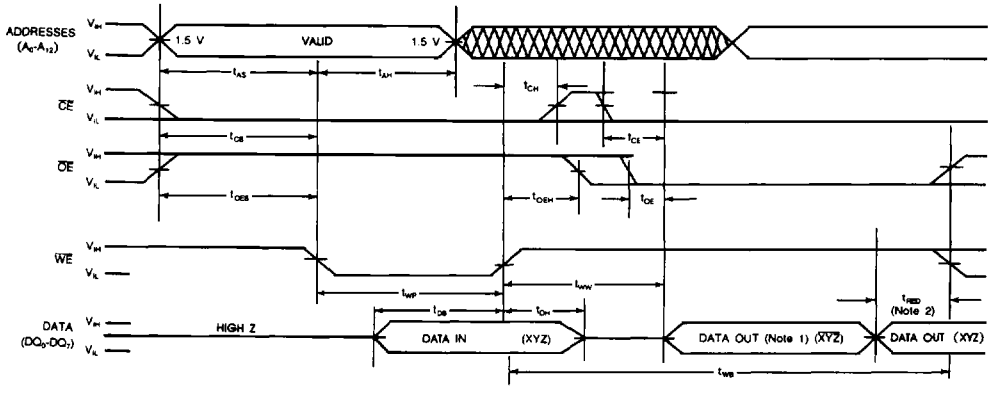
Page Write With $\overline{Data}$ Polling

Notes: 1. This is where $\overline{Data}$ Polling is available (if a write operation is performed).
2. $n \leqslant 32$.
3. After the write cycle is completed (Data Out True), the user must meet one of the following conditions to prevent an accidental write: $\overline{OE}$ LOW, $\overline{CE}$ HIGH, or $\overline{WE}$ HIGH.

SWITCHING WAVEFORMS



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Byte Write With $\overline{\text{Data}}$ Polling

Notes: 1. This is where $\overline{\text{Data}}$ Polling is available (if a read operation is performed).
2. After the write cycle is completed (Data Out True), the user must meet one of the following conditions to prevent an accidental write: $\overline{OE}$ LOW, $\overline{CE}$ HIGH, or $\overline{WE}$ HIGH.

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
I_{LI}	1, 2, 3
I_{LO}	1, 2, 3
I_{CC1}	1, 2, 3
I_{CC2}	1, 2, 3
I_{CC}	1, 2, 3
V_{IL}	1, 2, 3
V_{IH}	1, 2, 3
V_{OL}	1, 2, 3
V_{OH}	1, 2, 3
C_{IN}	4
C_{OUT}	4
V_{WI}	7, 8

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups	No.	Parameter Symbol	Subgroups
1	t_{ACC}	9, 10, 11	11	t_{DH}	9, 10, 11
2	t_{CE}	9, 10, 11	12	t_{CH}	9, 10, 11
3	t_{OE}	9, 10, 11	13	t_{OES}	9, 10, 11
4	t_{DF}	9, 10, 11	14	t_{OEH}	9, 10, 11
5	t_{OH}	9, 10, 11	15	t_{WC}	9, 10, 11
6	t_{AS}	9, 10, 11	16	t_{WW}	9, 10, 11
7	t_{CS}	9, 10, 11	17	t_{WH}	9, 10, 11
8	t_{WP}	9, 10, 11	18	t_{WB}	9, 10, 11
9	t_{AH}	9, 10, 11	19	t_{RED}	9, 10, 11
10	t_{DS}	9, 10, 11			

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.