Le7926

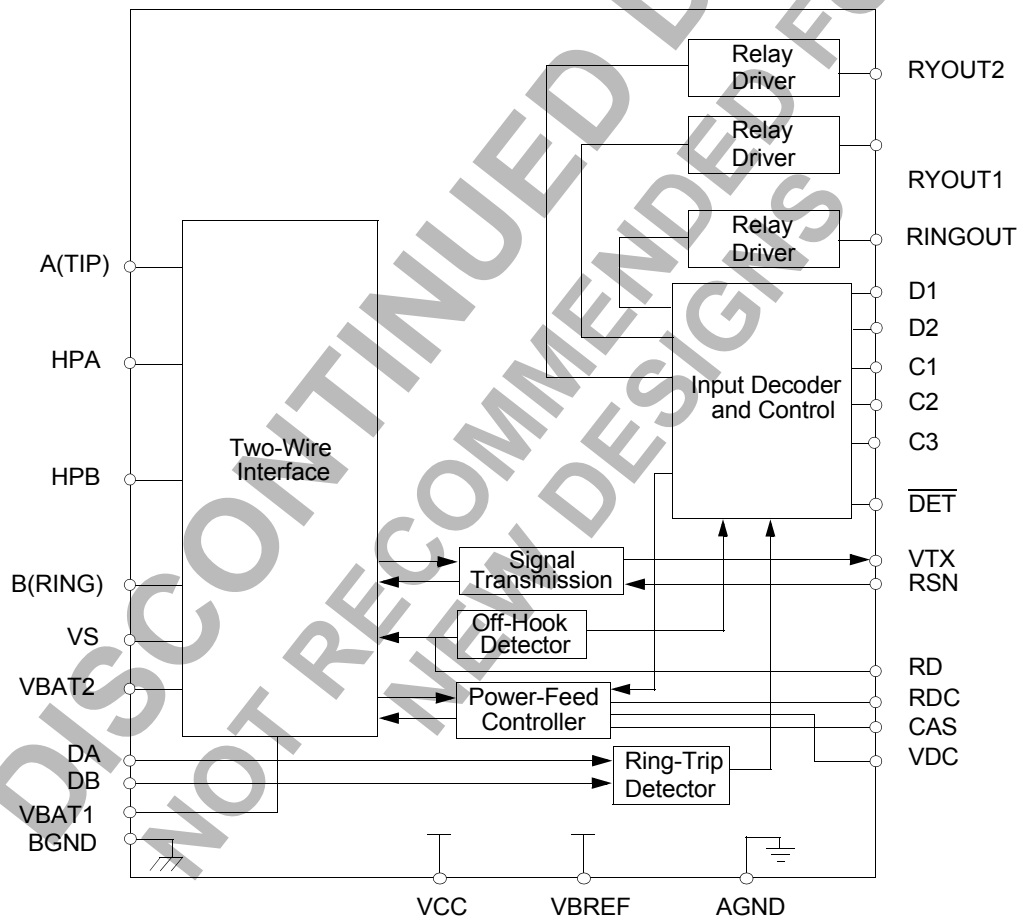
Subscriber Line Interface Circuit

The Le7926 Subscriber Line Interface Circuit implements the basic telephone line interface functions, and enables the design of low power, high performance, POTS line interface cards.

DISTINCTIVE CHARACTERISTICS

- **Ideal for high-density, low-power linecard applications**
- **Control states: Active, Reverse Polarity, Tip Open, Ringing, Standby, and Open Circuit**
- **Low standby power (45 mW)**
- **–16 V to –58 V battery operation**
- **On-hook transmission**
- **Two-wire impedance set by single external impedance**
- **Programmable constant-current feed**
- **Low Overhead Voltage (6 V)**
- **Programmable loop-detect threshold**
- **Ground-start detector**
- **Programmable ring-trip detect threshold**
- **No –5 V supply required**
- **Current Gain = 500**
- **Three on-chip relay drivers and relay snubbers, one ringing and two general purpose**
- **Tip Open state for ground-start lines**

BLOCK DIAGRAM

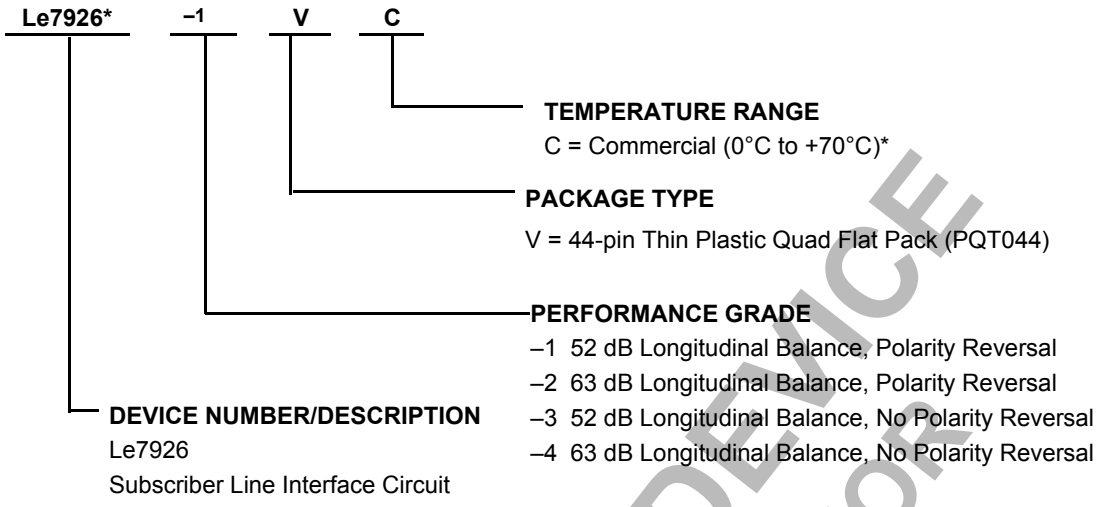


Document ID#	**080449**	Date:	**Jun 18, 2002**
Rev:	**B**	Version:	**1**
Distribution:	**Public Document**		

ORDERING INFORMATION

Standard Products

Legerity standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations		
Le7926*	–1	VC
	–2	
	–3	
	–4	

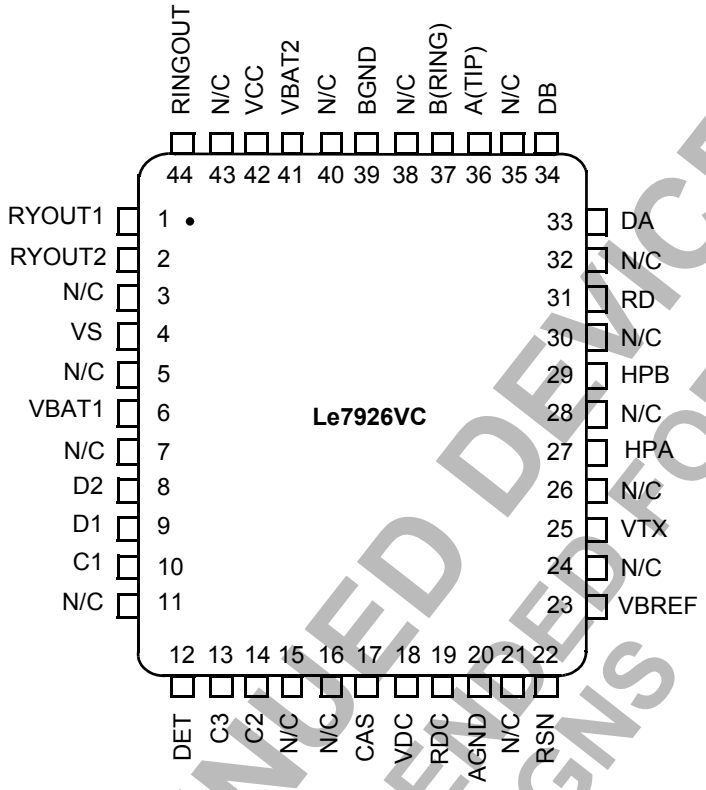
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Legerity sales office to confirm availability of specific valid combinations, to check on newly released combinations.

**Legerity reserves the right to fulfill all orders for this device with parts marked with the "Am" part number prefix, until such time as all inventory bearing this mark has been depleted. It should be noted that parts marked with either the "Am" or the "Le" part number prefix are equivalent devices in terms of form, fit, and function. The only difference between the two is in the part number prefix appearing on the topside mark.*

CONNECTION DIAGRAMS

Top View



Notes:

1. *Pin 1 is marked for orientation.*
2. *N/C = No Connect*
3. *RSVD = Reserved. Do not connect to this pin.*

PIN DESCRIPTIONS

Pin Name	Type	Description
AGND	Gnd	Analog and Digital ground.
A(TIP)	Output	Output of A(TIP) power amplifier.
BGND	Gnd	Battery (power) ground.
B(RING)	Output	Output of B(RING) power amplifier.
C3–C1	Input	SLIC control pins. C3 is MSB and C1 is LSB.
CAS	Capacitor	Anti-Saturation pin for capacitor to filter reference voltage when operating in anti-saturation region.
D2–D1	Input	Relay Driver Control. D1 and D2 control the relay drivers RYOUT1 and RYOUT2. Logic Low on D1 activates the RYOUT1 relay driver. Logic Low on D2 activates the RYOUT2 relay driver.
DA	Input	Negative input to ring-trip comparator.
DB	Input	Positive input to ring-trip comparator.
$\overline{\text{DET}}$	Output	Switchhook Detector. A logic Low indicates that selected condition is detected. The detect condition is selected by the logic inputs (C3–C1). The output is open-collector with a built-in 15 kΩ pull-up resistor.
HPA	Capacitor	A (TIP) side of high-pass filter capacitor.
HPB	Capacitor	B (RING) side of high-pass filter capacitor.
N/C	—	No Connect. This pin is not internally connected.
RD	Resistor	Detector threshold set and filter pin.
RDC	Resistor	Connection point for the DC feed current programming network. The other end of the network connects to the receiver summing node (RSN).
RINGOUT	Output	Ring Relay Driver. Open-collector driver with emitter internally connected to BGND.
RSN	Input	Receive Summing Node. The metallic current (both AC and DC) between A(TIP) and B(RING) is equal to 500 times the current into this pin. The networks which program receive gain, two-wire impedance, and feed resistance all connect to this node.
RYOUT1	Output	Relay/Switch Driver. Open-collector driver with emitter internally connected to BGND.
RYOUT2	Output	Relay/Switch Driver. Open-collector driver with emitter internally connected to BGND.
VBAT1	Battery	Battery supply and connection to substrate. When on hook, switcher should not be in use. Current draw is from VBAT1
VBAT2	Battery	Battery supply for output amplifiers.
VBREF	—	This is a Legerity reserved pin and must always be connected to the VBAT pin.
VCC	Power Supply	+5 V power supply.
VDC	Output	Output that is proportional to the line voltage: VDC = | V_A–V_B | / 20.
VS	Output	Output that is equal to $VREG_{MIN}$ + 2.4 V (total overhead needed is 6 V). The output can be used as a control input to an external switching regulator. The switching regulator output must be set to VS –2.4 V (or more negative) in order to guarantee performance of the SLIC.
VTX	Output	Transmit Audio. This output is a 0.50 gain version of the A(TIP) and B(RING) metallic voltage. VTX also sources the two-wire input impedance programming network.

ABSOLUTE MAXIMUM RATINGS

Storage temperature ..... –55°C to +150°C

V_{CC} with respect to AGND ..... –0.4 V to +7.0 V

V_{BAT1}, V_{BAT2} with respect to AGND:
- Continuous ..... +0.4 V to –70 V
- 10 ms ..... +0.4 V to –75 V

BGND with respect to AGND ..... +3 V to –3 V

A(TIP) or B(RING) to BGND:
- Continuous ..... V_{BAT} to +1 V
- 10 ms (f = 0.1 Hz) ..... –70 V to +5 V
- 1 µs (f = 0.1 Hz) ..... –80 V to +8 V
- 250 ns (f = 0.1 Hz) ..... –90 V to +12 V

Current from A(TIP) or B(RING)..... ±150 mA

RINGOUT/RYOUT1,2 current..... 50 mA

RINGOUT/RYOUT1,2 voltage ..... BGND to +7 V

RINGOUT/RYOUT1,2 transient ..... BGND to +10 V

DA and DB inputs
- Voltage on ring-trip inputs ..... V_{BAT} to 0 V
- Current into ring-trip inputs ..... ±10 mA

C3–C1 and D2–D1
- Input voltage ..... –0.4 V to V_{CC} + 0.4 V

Maximum power dissipation, continuous, T_A = 70°C, No heat sink (See note)
- In 44-pin TQFP package..... 1.4 W

Thermal Data:..... θ_{JA}
- In 44-pin TQFP package..... 52°C/W typ

ESD immunity/pin (HBM) ..... 1500 V

Note: *Thermal limiting circuitry on-chip will shut down the circuit at a junction temperature of about 165°C. The device should never see this temperature and operation above 145°C junction temperature may degrade device reliability.*

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient temperature ..... 0°C to +70°C*

V_{CC} ..... 4.75 V to 5.25 V

V_{BAT1}, V_{BAT2} ..... –15 V to –58 V

AGND..... 0 V

BGND with respect to AGND ..... –100 mV to +100 mV

Load resistance on VTX to ground ..... 20 kΩ min

**The operating ranges define those limits between which the functionality of the device is guaranteed.*

** Legerity guarantees the performance of this device over commercial (0 to 70° C) and industrial (-40 to 85 °C) temperature ranges by conducting electrical characterization over each range and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with section 4.6.2 of Bellcore TR-TSY-000357 Component Reliability Assurance Requirements for Telecommunications Equipment.*

ELECTRICAL CHARACTERISTICS

Description	Test Conditions (see Note 1)	Min	Typ	Max	Unit	Note
Transmission Performance						
2-wire return loss	200 Hz to 3.4 kHz	26			dB	1, 4
Analog output (VTX) impedance			1	20	Ω	4
Analog (VTX) output offset voltage		–50		+50	mV	
Overload level, 2-wire	Active state	2.5			Vpk	2a
Overload level	On hook, R_{LAC} = 600 Ω	0.77			Vrms	2b
THD, Total Harmonic Distortion	0 dBm +7 dBm		–64 –55	–50 –40	dB	5
THD, On hook	0 dBm, R_{LAC} = 600 Ω			–36		
Longitudinal Capability (See Test Circuit D)						
Longitudinal to metallic L-T, L-4 200 Hz to 1 kHz	Normal Polarity 0°C to +70°C -2,-4 -40°C to +85°C -2,-4 0°C to +70°C -1,-3 -40°C to +85°C -1,-3 Reverse Polarity -40°C to +85°C -2 0°C to +70°C -1 -40°C to +85°C -1	 63 58 52 50 54 52 50			dB	 4 4 4 4
Longitudinal to metallic L-T, L-4 1 kHz to 3.4 kHz	Normal Polarity 0°C to +70°C -2,-4 -40°C to +85°C -2,-4 0°C to +70°C -1,-3 -40°C to +85°C -1,-3 Reverse Polarity -40°C to +85°C -2 0°C to +70°C -1 -40°C to +85°C -1	 58 53 52 50 53 52 50			dB	 4 4 4 4
Longitudinal signal generation 4-L	200 Hz to 3.4 kHz	40				
Longitudinal current per pin (A or B)	Active state	17	27		mArms	8
Longitudinal impedance at A or B	0 to 100 Hz		25		Ω/pin	4
Idle Channel Noise						
C-message weighted noise	R_L = 600 Ω 0°C to +70°C R_L = 600 Ω –40°C to +85°C		7	+10 +12	dBrnc	4
Psophometric weighted noise	R_L = 600 Ω 0°C to +70°C R_L = 600 Ω –40°C to +85°C		–83	–80 –78	dBmp	
Insertion Loss and Balance Return Signal (See Test Circuits A and B)						
Gain accuracy 4- to 2-wire	0 dBm, 1 kHz	–0.20	0	+0.20	dB	3
Gain accuracy 2- to 4-wire, 4- to 4-wire	0 dBm, 1 kHz	–6.22	–6.02	–5.82		3
Gain accuracy, 4- to 2-wire	On hook	–0.35		+0.35		3,4
Gain accuracy, 2- to 4-wire, 4- to 4-wire	On hook	–6.37	–6.02	–5.67		
Gain accuracy over frequency	300 to 3.4 kHz relative to 1 kHz	–0.15		+0.15		3
Gain tracking	+3 dBm to –55 dBm relative to 0 dBm	–0.15		+0.15		3,4
Gain tracking On hook	0 dBm to –37 dBm +3 dBm to 0 dBm	–0.15 –0.35		+0.15 +0.35		3,4
Group delay	0 dBm, 1 kHz		4		µs	4, 7

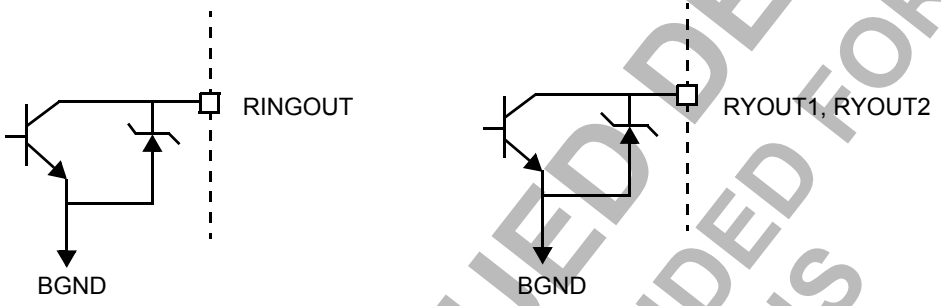
ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Line Characteristics						
I_L, Short Loops, Active state	R_{LDC} = 600 Ω	22.5	24.5	26.5	mA	
I_L, Long Loops, Active state	R_{LDC} = 2010 Ω, VBAT = –50 V	20	22.5			
I_L, Accuracy, Standby state	$I_L = \frac{\lvert BAT\rvert - 3\ V}{R_{L,} + 400}$ $T_A = 25°C$	16				
	Constant-current region	18	30			
I_LLIM	Active, A and B to ground		75	120	mA	
VDC Accuracy	VDC = |VAB| /20 Ri = 300 to 1500 Ω	0.053	0.055	0.057		9
VAB, Open Circuit voltage	$V_{BAT} = V_{BAT1}$, V_{BAT2} = –50 V	42.75	44		V	
I_A, Leakage, Tip Open state	R_L = 0			100	µA	
I_B, Current, Tip Open state	B to GND	15	30	56	mA	
V_A, Active	RA to BAT = 7 kΩ, RB to GND = 100 Ω	–7.5	–5		V	4
VS, Act/Nor IL = 25 mA	V_{BAT} = VS –2.4 V	VB–0.5	VB–1.1	VB–1.7	V	
VS, Pol–Rev IL = 25 mA		VA–0.5	VA–1.1	VA–1.7		
VS, Max Load		–20		100	µA	4
Power Supply Rejection Ratio						
V_{CC}	50 Hz to 3.4 kHz (V_{RIPPLE} = 100 mVrms)	30	40		dB	5
V_{BAT}	50 Hz to 3.4 kHz off-hook constant current (V_{RIPPLE} = 500 mVpp)	28	50			
Effective internal resistance	CAS pin to V_{BAT}	85	170	255	kΩ	4
Power Dissipation						
On hook, Standby state			45	60	mW	
On hook, Active state			130	170		
Off hook, Standby state	R_L = 600 Ω		860	1200		
Off hook, Active state	R_L = 600 Ω, V_{BAT} = – (|VAB| + 6.5 V)		230	320		
Supply Currents						
I_{CC}, On-hook V_{CC} supply current	Standby state Active state		2.3 4.25	3.2 6.0	mA	
I_{BAT}, On-hook V_{BAT} supply current	Standby state Active state		0.65 2.0	0.9 3.0		
RFI Rejection						
RFI rejection	100 kHz to 30 MHz, (See Figure F)			1.0	mVrms	4
Receive Summing Node (RSN)						
RSN DC voltage	I_{RSN} = 0 mA		0		V	4
RSN impedance	200 Hz to 3.4 kHz		10	20	Ω	
Logic Inputs (C3–C1 and D2–D1)						
V_{IH}, Input High voltage (except C3)		2.0			V	
V_{IH}, C3		2.5				
V_{IL}, Input Low voltage				0.8		
I_{IH}, Input High current		–75		40	µA	
I_{IL}, Input Low current		–400				
Logic Output ($\overline{\text{DET}}$)						
V_{OL}, Output Low voltage	I_{OUT} = 0.3 mA, 15 kΩ to V_{CC}			0.40	V	
V_{OH}, Output High voltage	I_{OUT} = –0.1 mA, 15 kΩ to V_{CC}	2.4				

ELECTRICAL CHARACTERISTICS (continued)

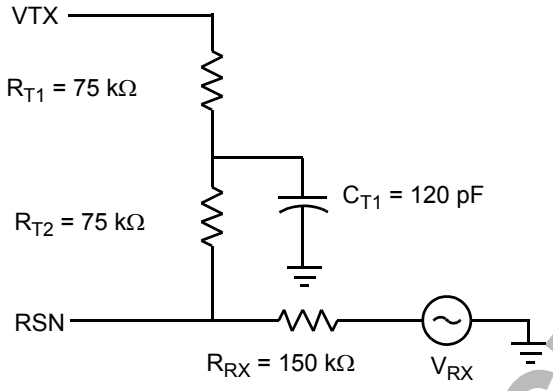
Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Ring-Trip Detector Input (DA, DB)						
Bias current		–500	–50		nA	
Offset voltage	Source resistance = 2 MΩ	–50	0	+50	mV	6
Loop Detector						
On threshold	R_D = 35.4 kΩ	9.4	11.7	14.0	mA	
Off threshold	R_D = 35.4 kΩ	8.8	10.4	12.0		
Hysteresis	R_D = 35.4 kΩ		1.3			
IGK, Ground-key detector threshold	R_L from BX to GND Active, Standby, and Tip open	5	9	13	mA	
Relay Driver Output (RINGOUT, RYOUT1, RYOUT2)						
On voltage	I_{OL} = 40 mA		+0.3	+0.7	V	
Off leakage	V_{OH} = +5 V			100	µA	
Zener breakover	I_Z = 100 µA	6	7.2		V	
Zener On voltage	I_Z = 30 mA		8			

RELAY DRIVER SCHEMATICS



Notes:

1. *Unless otherwise noted, test conditions are VBAT1 = VBAT2 = –52 V, V_{CC} = +5 V, R_L = 600 Ω, R_{DC1} = R_{DC2} = 13.02K, R_D = 35.4 kΩ, no fuse resistors, C_{HP} = 0.22 µF, C_{DC} = 0.33 µF, C_{CAS} = 0.33 µF, D1 = 1N400x, two-wire AC input impedance is a 600 Ω resistance synthesized by the programming network shown below.*



2. *a. Overload level is defined when THD = 1%.*
   b. Overload level is defined when THD = 1.5%.
3. *Balance return signal is the signal generated at V_{TX} by V_{RX}. This specification assumes that the two-wire, AC-load impedance matches the programmed impedance.*
4. *Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.*
5. *This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.*
6. *Tested with 0 Ω source impedance. 2 MΩ is specified for system design only.*
7. *Group delay can be greatly reduced by using a Z_T network such as that shown in Note 1. The network reduces the group delay to less than 2 µs and increases 2WRL. The effect of group delay on linecard performance also may be compensated for by synthesizing complex impedance with the QSLAC™ or DSLAC™ device.*
8. *Minimum current level guaranteed not to cause a false loop detect.*
9. *V_{DC}/V_{AB}*

Table 1. SLIC Decoding

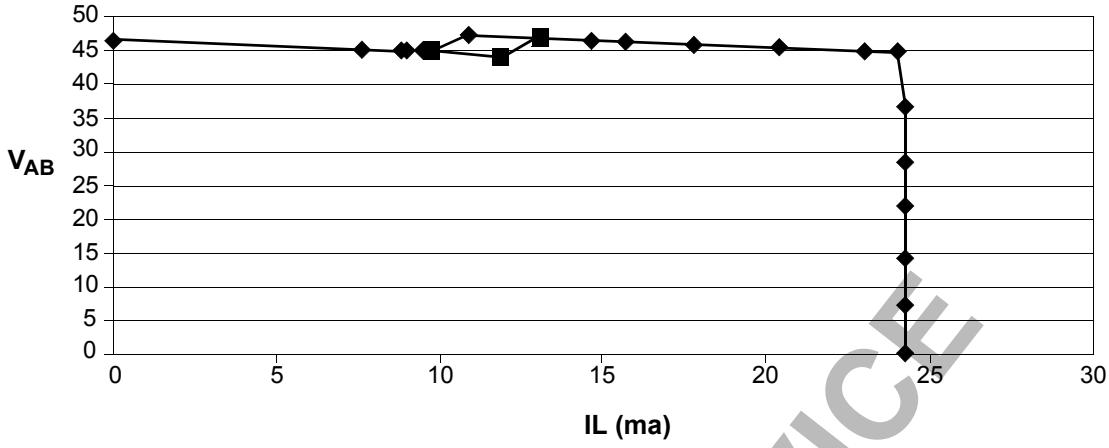
State	C3	C2	C1	Two-Wire Status	$\overline{\text{DET}}$ Output
0	0	0	0	Reserved	X
1	0	0	1	Reserved	X
2	0	1	0	Active Polarity Reversal	Loop detector
3	0	1	1	Tip Open	Ground Key*
4	1	0	0	Open Circuit	Ring trip
5	1	0	1	Ringing	Ring trip
6	1	1	0	Active	Loop detector
7	1	1	1	Standby	Loop detector

**Ground key selection in Tip Open is automatic. If longitudinal current is greater than 9 mA in Active, Standby, or Tip Open, the $\overline{\text{DET}}$ will go low. Therefore, if in Active or Standby, $\overline{\text{DET}}$ may be an indication of off hook, ground key, or both.*

Table 2. User-Programmable Components

$Z_T = 250(Z_{2WIN} - 2R_F)$	Z_T is connected between the VTX and RSN pins. The fuse resistors are R_F, and Z_{2WIN} is the desired 2-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between VTX and RSN must be taken into account.
$Z_{RX} = \frac{Z_L}{G_{42L}} \bullet \frac{500Z_T}{Z_T + 250(Z_L + 2R_F)}$	Z_{RX} is connected from VRX to RSN. Z_T is defined above, and G_{42L} is the desired receive gain.
$R_{DC1} + R_{DC2} = \frac{625}{I_{LOOP}}$ $C_{DC} = 1.5\ ms \bullet \frac{R_{DC1} + R_{DC2}}{R_{DC1} \bullet R_{DC2}}$	R_{DC1}, R_{DC2}, and C_{DC} form the network connected to the R_{DC} pin. R_{DC1} and R_{DC2} are approximately equal. I_{LOOP} is the desired loop current in the constant-current region.
$RD_{ON} = \frac{390}{I_T}$, $RD_{OFF} = \frac{355}{I_T}$, $C_D = \frac{0.5\ ms}{R_D}$	R_D and C_D form the network connected from R_D to AGND/DGND and I_T is the threshold current between on hook and off hook.
$C_{CAS} = \frac{1}{3.4 \bullet 10^5 \pi f_c}$	C_{CAS} is the regulator filter capacitor and f_c is the desired filter cut-off frequency.
$I_{STANDBY} = \frac{\lvert V_{BAT} \rvert - 3\ V}{400\ \Omega + R_L}$	Standby loop current (resistive region).

DC Characteristics



Notes:

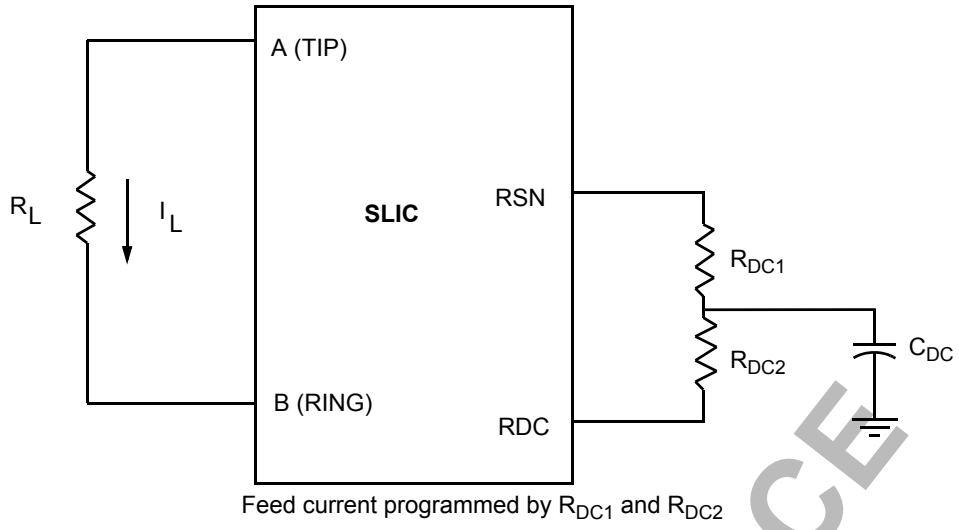
1. *Constant current region:* $V_{AB} = I_L R_L' = \frac{625}{R_{DC}} R_L'$, where $R_L' = R_L + 2R_F$

2. *Battery tracking anti-sat (off hook):*
   - *a)* $V_{AB} \leq 41.6$ V $\quad V_{AB} = |V_{BAT}| - 2.0 - I_L(R_{DC}/138)$
   - *b)* $V_{AB} \geq 41.6$ V $\quad V_{AB} = .8|V_{BAT}| + 6.73 - I_L(R_{DC}/172)$

3. *Battery tracking anti-sat (on hook):*
   - *a)* $V_{AB} \leq 41.6$ V $\quad V_{AB} = |V_{BAT}| - 5.3 - I_L(R_{DC}/138)$
   - *b)* $V_{AB} \geq 41.6$ V $\quad V_{AB} = .8|V_{BAT}| + 4.08 - I_L(R_{DC}/172)$

a. Load Line (Typical)

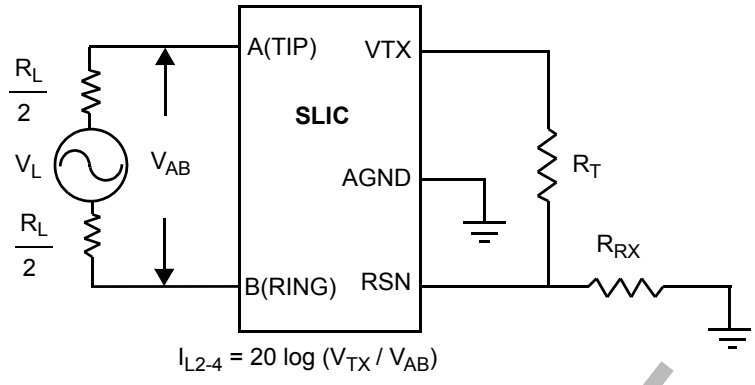
DC FEED CHARACTERISTICS (continued)



b. Feed Programming

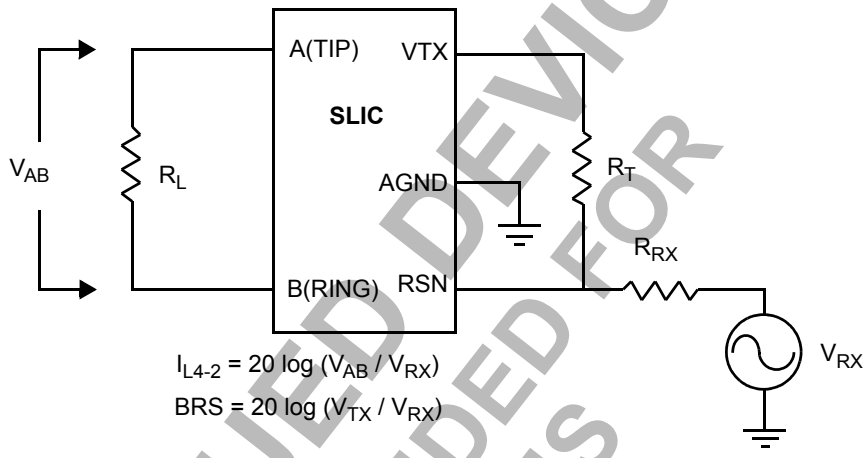
Figure 1. DC Feed Characteristics

TEST CIRCUITS



$I_{L2-4} = 20 \log (V_{TX} / V_{AB})$

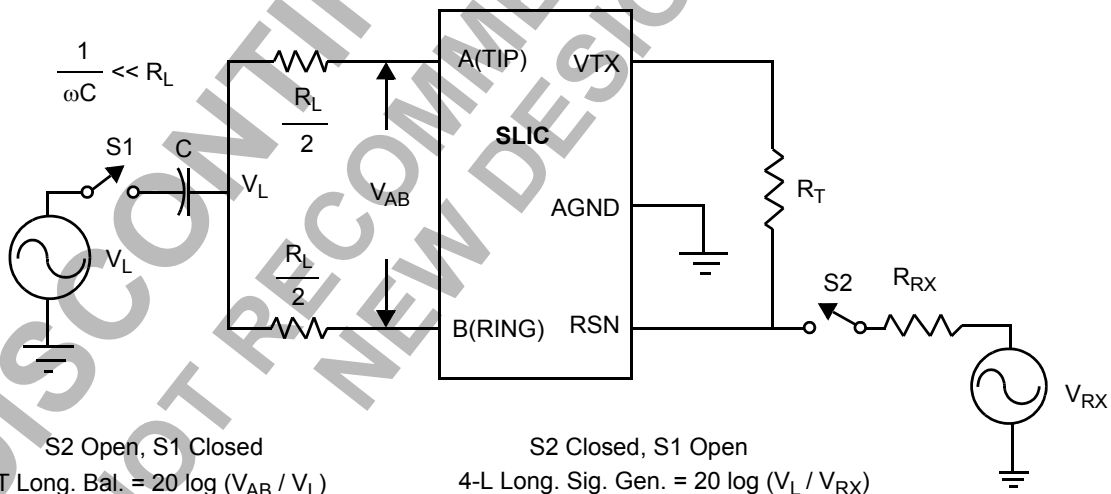
A. Two- to Four-Wire Insertion Loss



$I_{L4-2} = 20 \log (V_{AB} / V_{RX})$

$BRS = 20 \log (V_{TX} / V_{RX})$

B. Four- to Two-Wire Insertion Loss and Balance Return Signal



S2 Open, S1 Closed

L-T Long. Bal. = $20 \log (V_{AB} / V_L)$

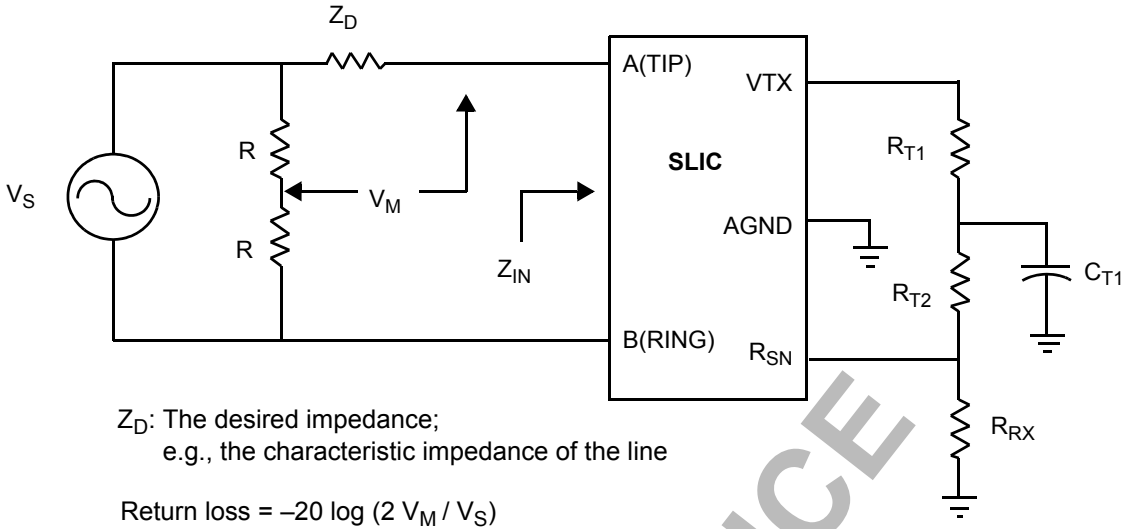
L-4 Long. Bal. = $20 \log (V_{TX} / V_L)$

S2 Closed, S1 Open

4-L Long. Sig. Gen. = $20 \log (V_L / V_{RX})$

C. Longitudinal Balance

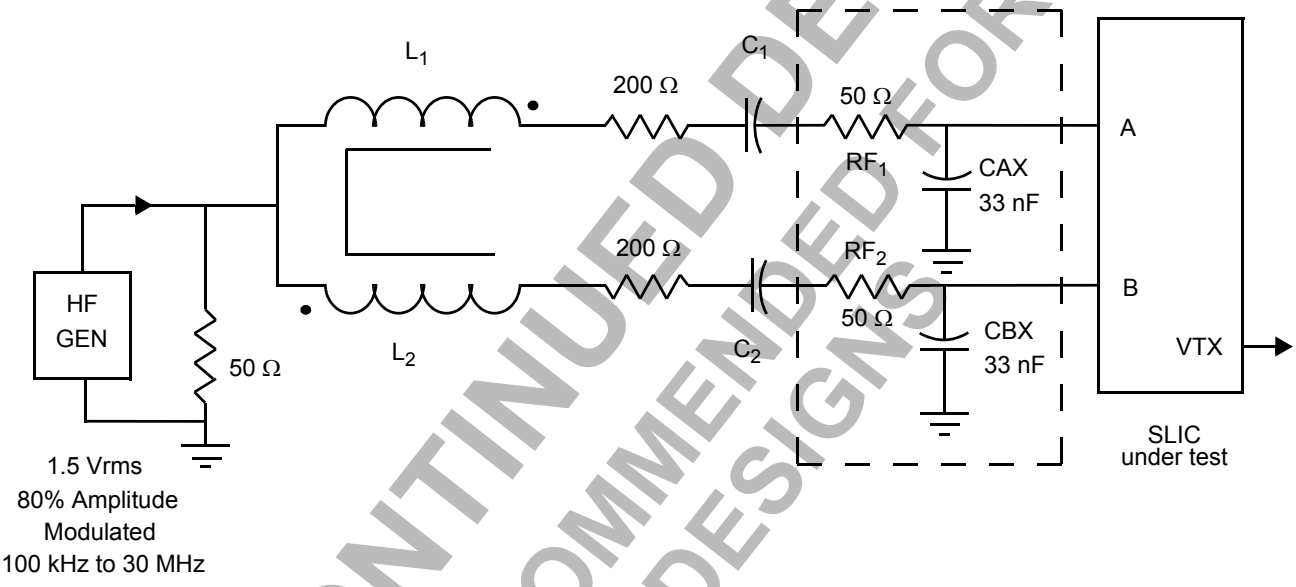
TEST CIRCUITS (continued)



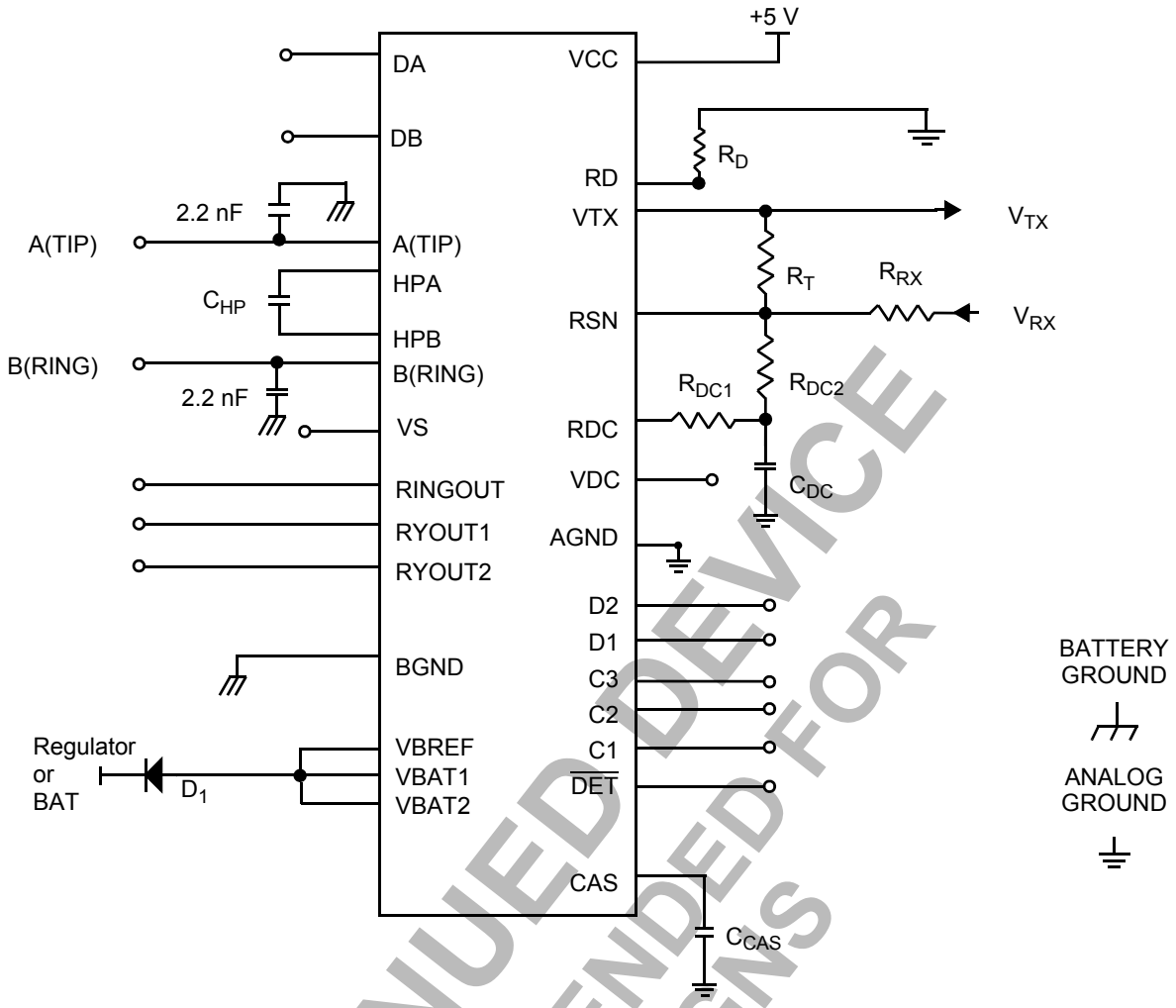
Z_D: The desired impedance;
e.g., the characteristic impedance of the line

Return loss = –20 log (2 V_M / V_S)

D. Two-Wire Return Loss Test Circuit

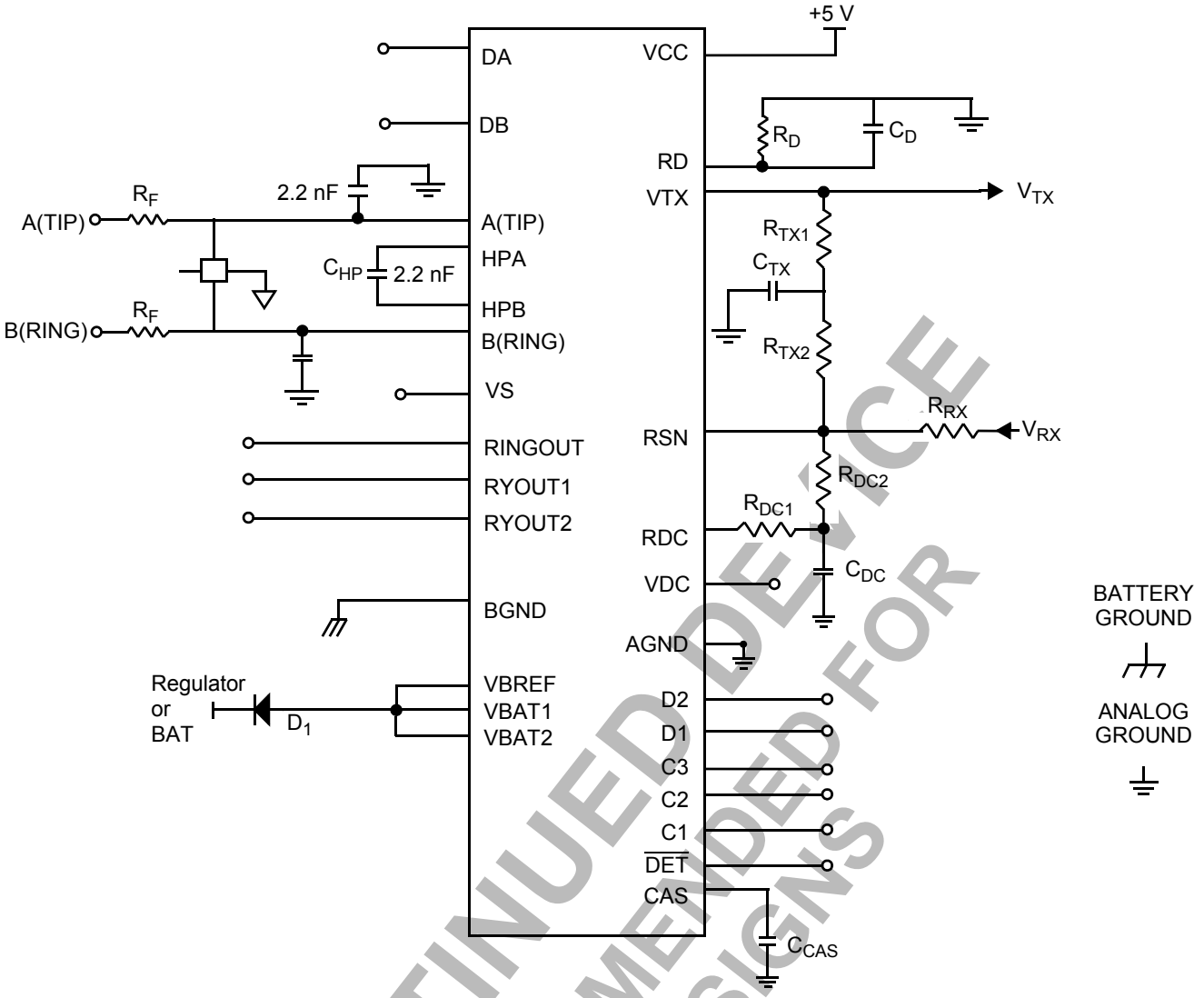


E. RFI Test Circuit



F. Le7926 Test Circuit

APPLICATION CIRCUIT



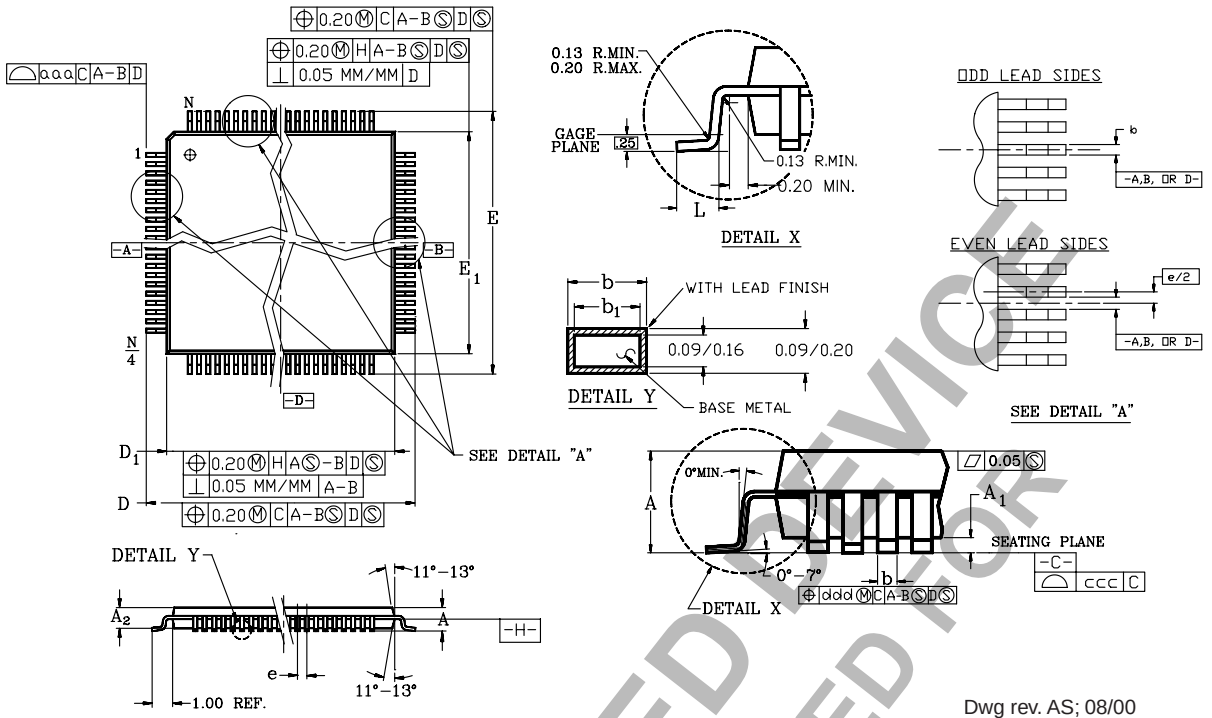
F. Le7926 Application Circuit

PHYSICAL DIMENSION

PQT044

BSC is an ANSI standard for Basic Centering. Dimensions are measured in millimeters.

TQFP 044



Dwg rev. AS; 08/00

PACKAGE	TQFP 044		
JEDEC	MS-026 (C) ACB		
SYMBOL	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	--	0.15
A2	0.95	1.00	1.05
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
L	0.45	0.60	0.75
N	44		
e	0.80 BASIC		
b	0.30	0.37	0.45
b1	0.30	0.35	0.40
TOLERANCES OF FORM AND POSITION			
ccc	0.10		
ddd	0.20		
aaa	0.20		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. DATUM PLANE -H- IS LOCATED AT THE MOLD PARTING LINE AND IS COINCIDENT WITH THE BOTTOM OF THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY.
3. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.254mm PER SIDE. DIMENSIONS "D1" AND "E1" INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-
4. DIMENSION "B" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
5. CONTROLLING DIMENSIONS: MILLIMETER.
6. DIMENSIONS "D" AND "E" ARE MEASURED FROM BOTH INNERMOST AND OUTERMOST POINTS.
7. DEVIATION FROM LEAD-TIP TRUE POSITION SHALL BE WITHIN ±0.076 MM. FOR PITCH >0.5mm. AND WITHIN ±0.04 FOR PITCH ≤ 0.5 mm.
8. LEAD COPLANARITY SHALL BE WITHIN: (REFER TO 06-500)
   1- 0.10 mm FOR DEVICES WITH LEAD PITCH OF 0.65-0.80 mm.
   2- 0.076 mm FOR DEVICES WITH LEAD PITCH OF 0.50 mm.
   COPLANARITY IS MEASURED PER SPECIFICATION 06-500.
9. HALF SPAN (CENTER OF PACKAGE TO LEAD TIP) SHALL BE 15.30±.165{.602"±.0065"}
10. "N" IS THE TOTAL NUMBER OF TERMINALS.
11. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF THE PACKAGE BY 0.15 MILLIMETERS.
12. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-026.
13. THE 160 LEAD IS A COMPLIANT DEPOPULATION OF THE 176 LEAD MS-026 VARIATION BGA.

REVISION SUMMARY

Revision A to Revision A2

- Updated the Pin Description table to correct inconsistencies.
- The physical dimension (PQT044) was added to the Physical Dimension section.
- Added the Connection Diagram on page 3.

Revision A2 to Revision A3

- Changed 8 V to 6 V in the Distinctive Characteristics section.
- Added the 32-pin PLCC information to the Ordering Information and Absolute Maximum Ratings sections and added the connection diagram.
- In the Electrical Characteristics table:
  - — Updated the information in the Line Characteristics section on the Long Loops row and the VDC Accuracy row.
  - — Deleted the Disconnect state information in the Power Dissipation and Supply Currents sections.

Revision A3 to Revision B

- Updated OPN (Ordering Part Number) throughout document.
- Replaced obsolete sales office listing page.
- Updated physical dimensions drawings.
- Absolute Maximum Ratings: Notes updated to standard.
- Operating Ranges: Temperature statement updated to standard.