A1 PROs

Ai9943

Complete 10-bit , 25MHz CCD Signal Processor

General Description

The Ai9943 is a complete analog signal processor for CCD applications. It features a 25 MHz single-channel architecture designed to sample and condition the outputs of interlaced and progressive scan area CCD arrays. The signal chain for the Ai9943 consists of a correlated double sampler (CDS), a digitally controlled variable gain amplifier (VGA), and a black level clamp. The Ai9943 offers 10-bit ADC resolution.

The internal registers are programmed through a 3-wire serial digital interface. Programmable features include gain adjustment, black level adjustment, input clock polarity, and power-down modes. The Ai9943 operates from a single 3 V power supply and typically dissipates 79 mW.

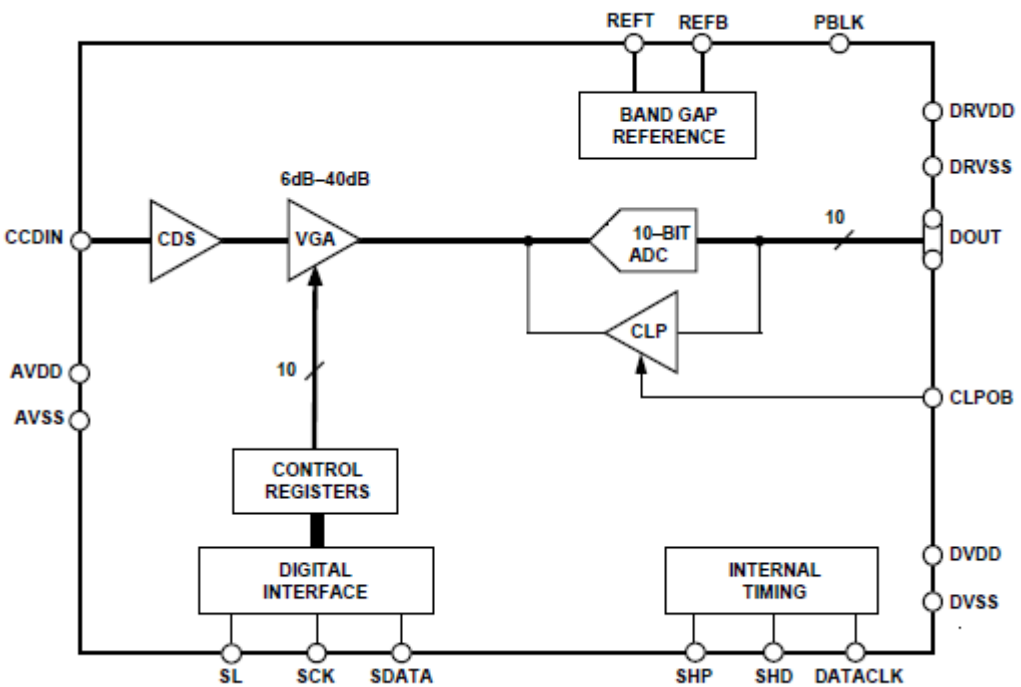
Features

- 25 MSPS correlated double sampler (CDS)
- 6 dB to 40 dB 10-bit variable gain amplifier (VGA)
- Low noise optical black clamp circuit
- Preblanking function
- 10-bit, 25 MSPS A/D converter
- No missing codes guaranteed
- 3-wire serial digital interface
- 3 V single-supply operation
- Space-saving 32-lead, 5 mm × 5 mm QFN package

Applications

- Digital still cameras
- Digital video camcorders
- PC cameras
- Portable CCD imaging devices
- CCTV cameras

Functional Block Diagram



General Specifications

(T_{MIN} to T_{MAX}, AVDD = DVDD = DRVDD = 3 V, f_{SAMP} = 25 MHz, unless otherwise noted)

Parameter		Value			Unit
		Min	Typ	Max	
Temperature Range	Operating	-20		+85	℃
	Storage	-65		+150	℃
Power Supply Voltage (AVDD, DVDD, DRVDD)		2.7		3.6	V
Power Consumption	Normal Operation		79		mW
	Power-down Mode		150		μW
Maximum Clock Rate		25			MHz

Digital Specifications

(DRVDD = DVDD = 2.7 V, C_L = 20 pF, unless otherwise noted.)

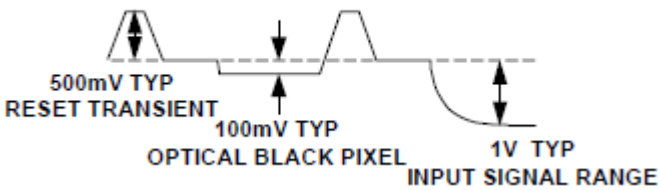
Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Logic Inputs	High Level Input Voltage	V_{IH}	2.1			V
	Low Level Input Voltage	V_{IL}			0.6	V
	High Level Input Current	I_{IH}		10		μA
	Low Level Input Current	I_{IL}		10		μA
	Input Capacitance	C_{IN}		10		pF
Logic Outputs	High Level Output Voltage I_{OH} = 2 mA	V_{OH}	2.2			V
	Low Level Output Voltage I_{OL} = 2 mA	V_{OL}			0.5	V

System Specifications

(T_{MIN} to T_{MAX}, AVDD = DVDD = DRVDD = 3 V, fSAMP = 25 MHz, unless otherwise noted)

Parameter		Value			Unit	Conditions
		Min	Typ	Max		
CDS						
Maximum Input Range before Saturation (*1)			1.0		Vp-p	
Allowable CCD Reset Transient			500		mV	See input waveform in footnote
Maximum CCD Black Pixel Amplitude			100		mV	
Variable Gain Amplifier (VGA)						
Gain Control Resolution			1024		steps	
Gain Monotonicity			Guaranteed			
Gain Range	Minimum gain		5.3		dB	See "*Variable Gain Amplifier*" section for VGA gain equation and the VGA gain curve.
	Maximum gain	40	41.5		dB	
Black Level Clamp						
Clamp Level Resolution			256		steps	
Clamp Level	Minimum clamp level		0		LSB	Measured at ADC output
	Maximum clamp level		63.75		LSB	
A/D Converter						
Resolution		10			Bits	
Differential Nonlinearity (DNL)			± 0.3		LSB	
No Missing Codes			Guaranteed			
Data Output Coding			Straight binary			
Full Scale Input Voltage			2.0		V	
Voltage Reference						
Reference Top Voltage (REFT)			2.0		V	
Reference Bottom Voltage (REFB)			1.0		V	
System Performance						Specifications include entire signal chain.
Gain Range	Low gain (VGA code = 0)		5.3		dB	
	Maximum gain (VGA code = 1023)	40	41.5		dB	
Gain Accuracy			± 1		dB	
Peak Nonlinearity 500 mV Input Signal			0.1		%	12 dB gain applied
Total Output Noise			0.3		LSB rms	AC grounded input, 6dB gain applied
Power Supply Rejection (PSR)			50		dB	Measured with step change on supply

(*1): **Input signal characteristics defined as follows:**



Timing Specifications

(CL = 20 pF, f_{SAMP} = 25 MHz. See CCD-mode timing in the section “CCD-mode Timing”)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Sample Clocks					
DATACLK, SHP, SHD Clock Period	t_{CONV}	40			ns
DATACLK High / Low Pulse Width	t_{ADC}	16	20		ns
SHP Pulse Width	t_{SHP}		10		ns
SHD Pulse Width	t_{SHD}		10		ns
CLPOB Pulse Width (*1)	t_{COB}	2	20		Pixels
SHP Rising Edge to SHD Falling Edge	t_{S1}		10		ns
SHP Rising Edge to SHD Rising Edge	t_{S2}	16	20		ns
Internal Clock Delay	t_{ID}		3.0		ns
Data Outputs					
Output Delay	t_{OD}		9.5		ns
Pipeline Delay			9		Cycles
Serial Interface					
Maximum SCK Frequency	t_{SCLK}	10			MHz
SL to SCK Setup Time	t_{LS}	10			ns
SCK to SL Hold Time	t_{LH}	10			ns
SDATA Valid to SCK Rising Edge Setup	t_{DS}	10			ns
SCK Falling Edge to SDATA Valid Hold	t_{DH}	10			ns

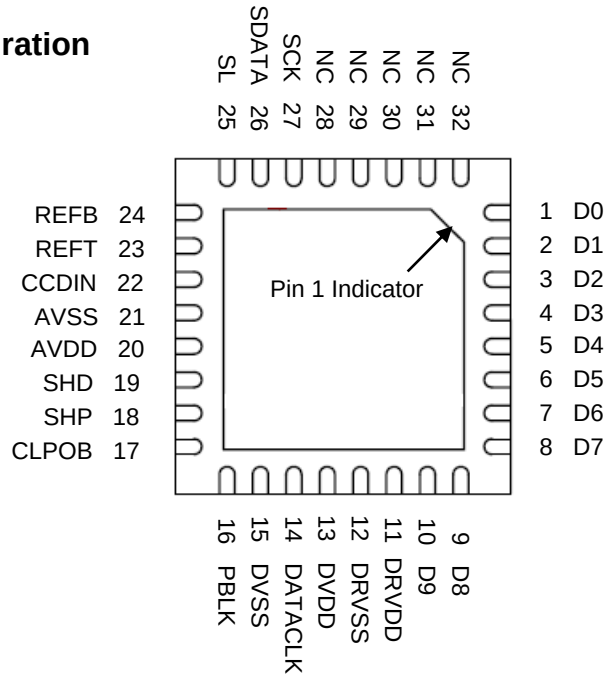
(*1): Minimum CLPOB pulse width is for functional operation only. Wider pulses are recommended to obtain low noise clamp performance.

Absolute Maximum Ratings

Parameter (with respect to)		Rating			Unit
		Min	Typ	Max	
Supply Voltage	AVDD (AVSS)	- 0.3		+ 3.9	V
	DVDD (DVSS)	- 0.3		+ 3.9	V
	DRVDD (DRVSS)	- 0.3		+ 3.9	V
Input Voltage	SHD, SHP, DATACLK (DVSS)	- 0.3		DVDD + 0.3	V
	CLPOB, PBLK (DVSS)	- 0.3		DVDD + 0.3	V
	SCK, SL, SDATA (DVSS)	- 0.3		DVDD + 0.3	V
	CCDIN (AVSS)	- 0.3		AVDD + 0.3	V
Output Voltage	D0 - D9 (DRVSS)	- 0.3		DRVDD + 0.3	V
	REFT, REFTB (AVSS)	- 0.3		AVDD + 0.3	V

NOTE : Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Configuration



QFNWB5×5-32L **(Bottom View)**

Pin Description

No.	Symbol	Type (*1)	Description
1 to 10	D0 to D9	DO	Digital Data Outputs.
11	DRVDD	P	Digital Output Driver Supply
12	DRVSS	P	Digital Output Driver Ground.
13	DVDD	P	Digital Supply
14	DATACLK	DI	Digital Data Output Latch Clock
15	DVSS	P	Digital Supply Ground
16	PBLK	DI	Preblanking Clock Input
17	CLPOB	DI	Black Level Clamp Clock Input
18	SHP	DI	CDS Sampling Clock for CCD Reference Level
19	SHD	DI	CDS Sampling Clock for CCD Data Level
20	AVDD	P	Analog Supply
21	AVSS	P	Analog Ground
22	CCDIN	AI	Analog Input for CCD Signal
23	REFT	AO	A/D Converter Top Reference Voltage Decoupling
24	REFB	AO	A/D Converter Bottom Reference Voltage Decoupling
25	SL	DI	Serial Digital Interface Load Pulse
26	SDATA	DI	Serial Digital Interface Data Input
27	SCK	DI	Serial Digital Interface Clock Input
28 to 30	NC	NC	Internally pulled down. Float or connect to GND
31 to 32	NC	NC	Internally not connected

(*1) Type: AI = analog input, AO = analog output, DI = digital input, DO = digital output, P = power, and NC = no connect

Terminology

Differential Nonlinearity (DNL)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Therefore every code must have a finite width. No missing codes guaranteed to 10-bit resolution indicates that all 1024 codes, respectively, must be present over all operating conditions.

Peak Nonlinearity

Peak nonlinearity, a full-signal chain specification, refers to the peak deviation of the output of the Ai9943 from a true straight line. The point used as zero scale occurs 1/2 LSB before the first code transition. Positive full scale is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular output code to the true straight line. The error is then expressed as a percentage of the 2 V ADC full-scale signal. The input signal is always appropriately gained up to fill the ADC's full-scale range.

Total Output Noise

The rms output noise is measured using histogram techniques. The standard deviation of the ADC output codes is calculated in LSB and represents the rms noise level of the total signal chain at the specified gain setting. The output noise can be converted to an equivalent voltage, using the relationship

1 LSB = *(ADC Full Scale / 2^N codes)*

where *N* is the bit resolution of the ADC. For example, 1 LSB of the Ai9943 is 1.95 mV

Power Supply Rejection (PSR)

The PSR is measured with a step change applied to the supply pins. This represents a very high frequency disturbance on the Ai9943's power supply. The PSR specification is calculated from the change in the data outputs for a given step change in the supply voltage.

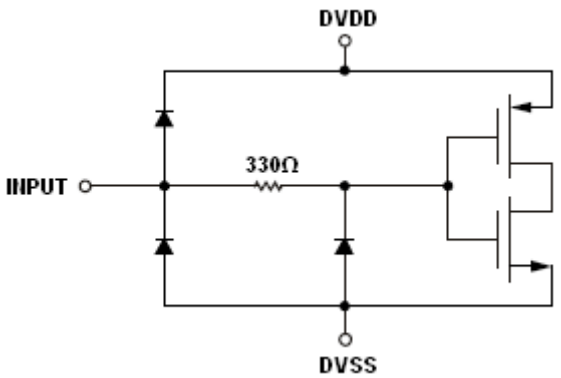
Internal Delay for SHP/SHD

The internal delay (also called aperture delay) is the time delay that occurs from the time a sampling edge is applied to the Ai9943 until the actual sample of the input signal is held. Both SHP and SHD sample the input signal during the transition from low to high, so the internal delay is measured from each clock's rising edge to the instant the actual internal sample is taken.

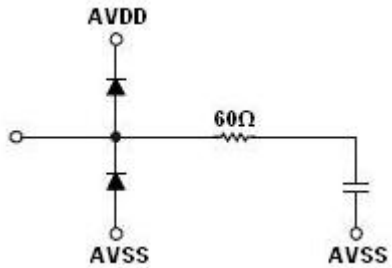
Equivalent Input Circuits

Digital Inputs

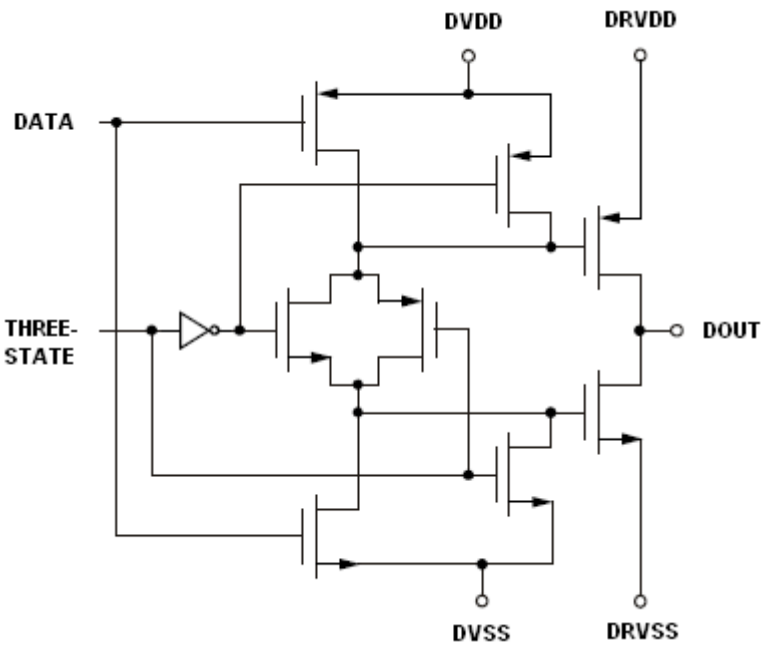
—SHP, SHD, DATACLK, CLOB, PBLK, SCK, SL



CCDIN (Pin 22)

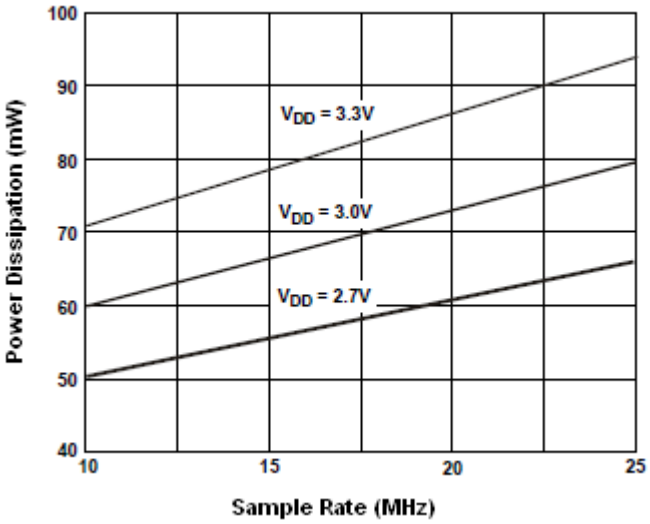


Data outputs

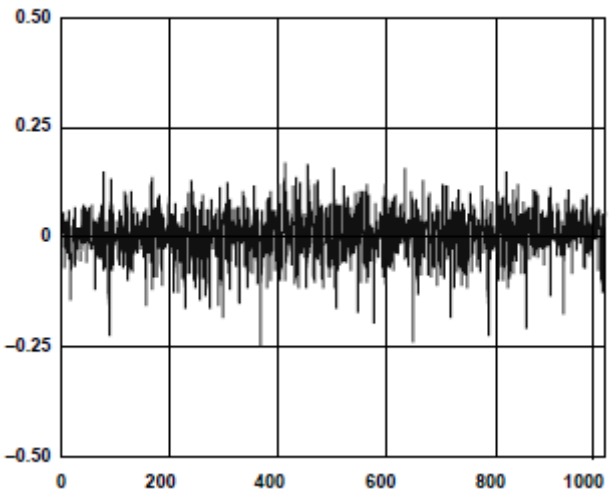


Typical Performance Characteristics

Power Vs Sample Rate



Typical DNL Performance



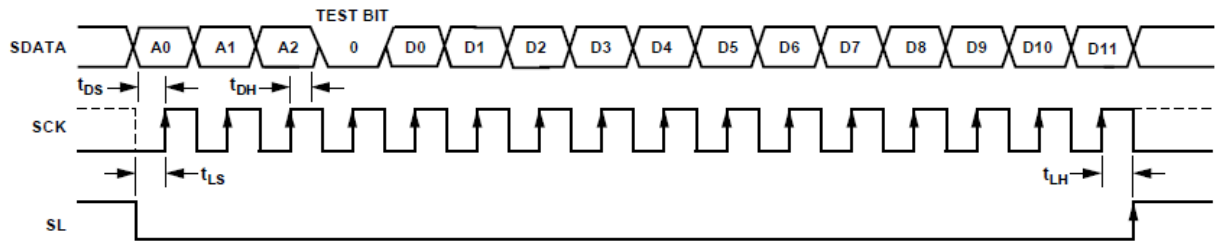
Internal Register Map

(All register values default to 0x000 at power-up except clamp level, which defaults to 128 decimal, corresponding to a clamp level of 32 LSB.)

Register Name	Address Bits			Data Bits	Function
	A2	A1	A0		
Operation	0	0	0	D0	Software Reset (0 = normal operation, 1 = reset all registers to default).
				D2, D1	Power-Down Modes (00 = normal power, 01 = standby, 10 = total shutdown).
				D3	OB Clamp Disable (0 = clamp on, 1 = clamp off).
				D5, D4	Test Mode. Should always be set to 00.
				D6	PBLK Blanking Level (0 = blank output to zero, 1 = blank to ob clamp level).
				D8, D7	Test Mode 1. Should always be set to 00.
				D11 to D9	Test Mode 2. Should always be set to 000.
Control	0	0	1	D0	SHP/SHD Input Polarity (0 = active low, 1 = active high).
				D1	DATACLK Input Polarity (0 = active low, 1 = active high).
				D2	CLPOB Input Polarity (0 = active low, 1 = active high).
				D3	PBLK Input Polarity (0 = active low, 1 = active high).
				D4	Three-State Data Outputs (0 = outputs active, 1 = outputs three-stated).
				D5	Data Output Latching (0 = latched by DATACLK, 1 = latch is transparent).
				D6	Data Output Coding (0 = binary output, 1 = gray code output).
				D11 to D7	Test Mode. Should always be set to 00000
Clamp Level	0	1	0	D7 to D0	OB Clamp Level (0 = 0 LSB, 255 = 63.75 LSB)
VGA Gain	0	1	1	D9 to D0	VGA Gain (0 = 6dB, 1023 = 40dB)

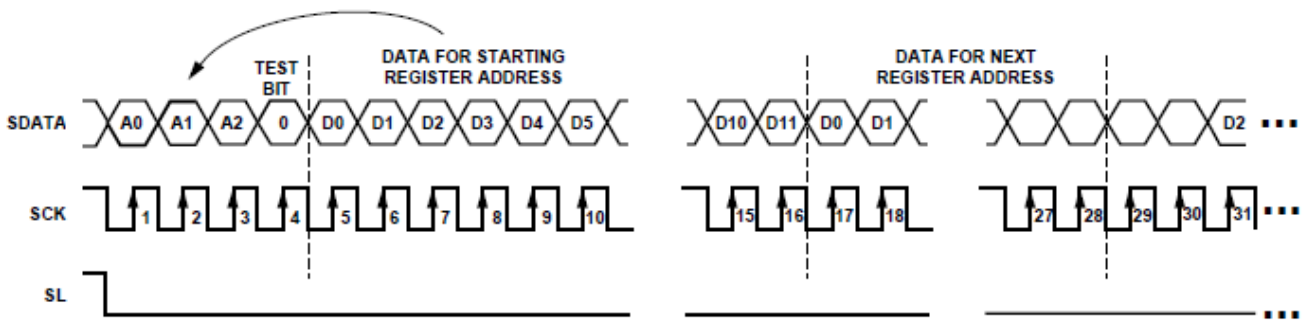
Serial Interface

Serial Write Operation



NOTE: 1. SDATA bits are internally latched on the rising edges of SCK.
2. System update of loaded registers occurs on SL rising edge.
3. All 12 data bits D0-D11 must be written. If the register contains fewer than 12 bits, zeros should be used for undefined bits.
4. Test bit is for internal use only and must be set low.

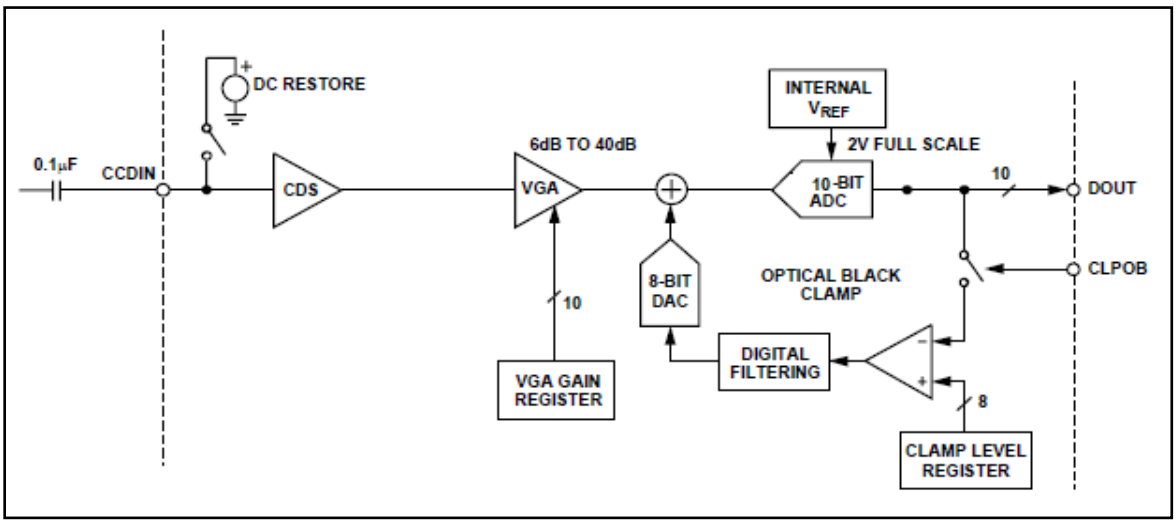
Continuous Serial Write Operation to All Registers



NOTE: 1. Multiple sequential registers may be loaded continuously.
2. The first (LOWEST address) register address is written, followed by multiple 12-bit data-words.
3. The address automatically increments with each 12-bit data-word. (All 12 bits must be written.)
4. SL is held LOW until the last desired register has been loaded.
5. New data is updated at the next SL rising edge.

Circuit Description and Operation

CCD Mode Block Diagram



The Ai9943 signal processing chain is shown in the above *"CCD Mode Block Diagram".* Each processing step is essential for achieving a high quality image from the raw CCD pixel data.

DC Restore

To reduce the large dc offset of the CCD output signal, a dc restore circuit is used with an external 0.1 µF series coupling capacitor. This restores the dc level of the CCD signal to approximately 1.5 V, which is compatible with the 3 V single supply of the Ai9943.

Correlated Double Sampler

The CDS circuit samples each CCD pixel twice to extract video information and reject low frequency noise. The figure *"CCD Mode Timing"* illustrates how the two CDS clocks, SHP and SHD, are used, respectively, to sample the reference level and data level of the CCD signal. The CCD signal is sampled on the rising edges of SHP and SHD. Placement of these two clock signals is critical for achieving the best performance from the CCD. An internal SHP/SHD delay (t_{ID}) of 3 ns is caused by internal propagation delays.

Optical Black Clamp

The optical black clamp loop is used to remove residual offsets in the signal chain and to track low frequency variations in the CCD's black level. During the optical black (shielded) pixel interval on each line, the ADC output is compared with the fixed black level reference selected by the user in the clamp level register. The resulting error signal is filtered to reduce noise, and the correction value is applied to the ADC input through a D/A converter. Normally, the optical black clamp loop is turned on once per horizontal line, but this loop can be updated more slowly to suit a particular application. If external digital clamping is used during the post processing, the optical black clamping for the Ai9943 may be disabled using Bit D3 in the operation register. Refer to the sections *"Serial Interface"* and *"Internal Register Map".*

When the loop is disabled, the clamp level register may still be used to provide programmable offset adjustment. Horizontal timing is shown in the *"Typical CCD Mode Line Clamp Timing"* below. The CLPOB pulse should be placed during the CCD's optical black pixels. It is recommended that the CLPOB pulse be used during valid CCD dark pixels. The CLPOB pulse should be a minimum of 20 pixels wide to minimize clamp noise. Shorter pulse widths may be used, but clamp noise may increase and the loop's ability to track low frequency variations in the black level is reduced.

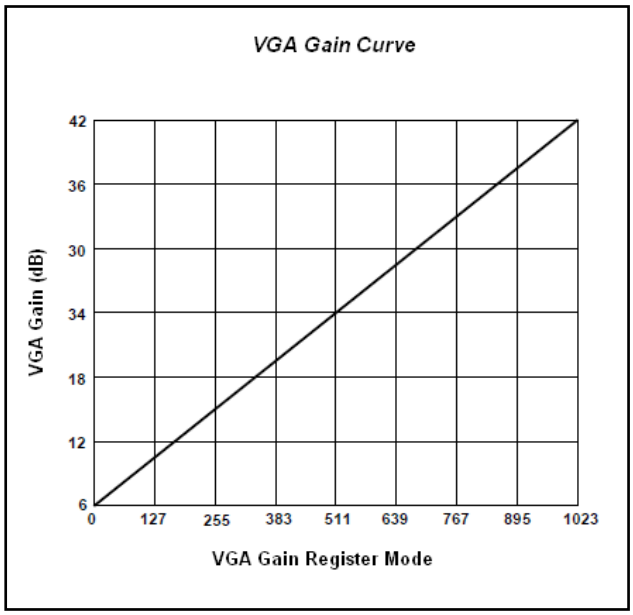
A/D Converter

The ADC uses a 2 V input range. Better noise performance results from using a larger ADC full-scale range. The ADC uses a pipelined architecture with a 2 V full-scale input for low noise performance.

Variable Gain Amplifier

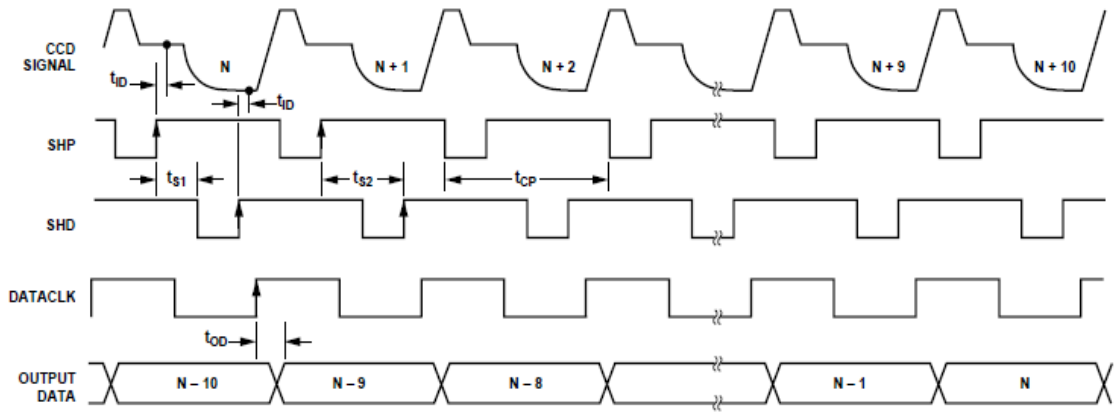
The VGA stage provides a gain range of 6 dB to 40 dB, programmable with 10-bit resolution through the serial digital interface. The minimum gain of 6 dB is needed to match a 1 V input signal with the ADC full-scale range of 2V. A plot of the VGA gain curve is shown on the right.

VGA Gain (dB) = (VGA Code × 0.035dB) +5.3 dB



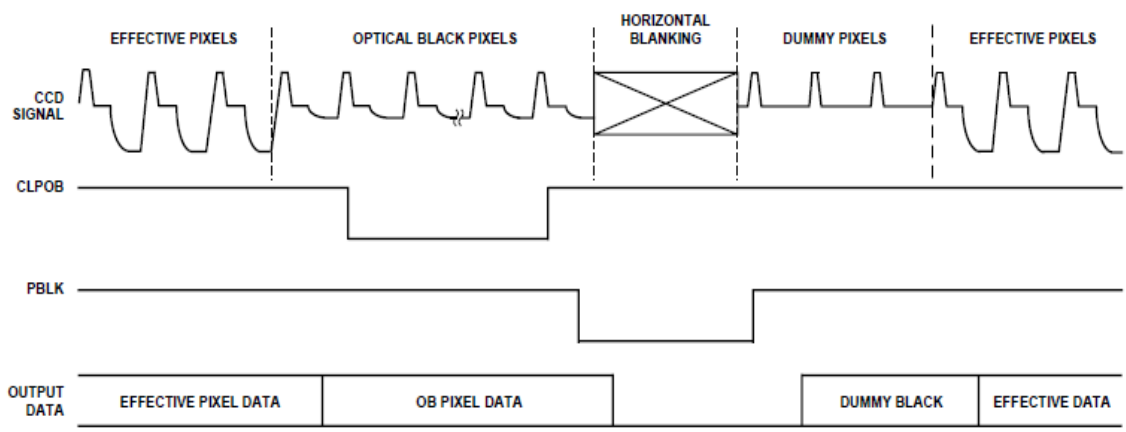
CCD Mode Timing

CCD Mode Timing



NOTES
1. RECOMMENDED PLACEMENT FOR DATACLK RISING EDGE IS BETWEEN THE SHD RISING EDGE AND NEXT SHP FALLING EDGE.
2. CCD SIGNAL IS SAMPLED AT SHP AND SHD RISING EDGES.

Typical CCD Mode Line Clamp Timing

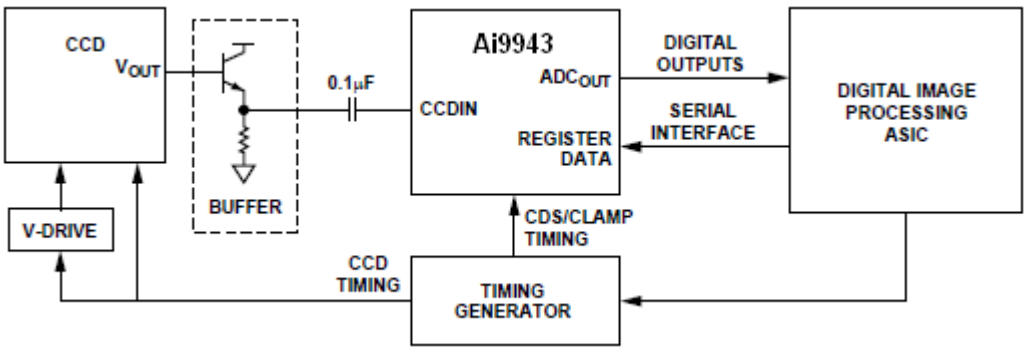


NOTES
1. CLPOB WILL OVERWRITE PBLK. PBLK WILL NOT AFFECT CLAMP OPERATION IF OVERLAPPING WITH CLPOB.
2. PBLK SIGNAL IS OPTIONAL.
3. DIGITAL OUTPUT DATA WILL BE ALL ZEROS DURING PBLK. OUTPUT DATA LATENCY IS NINE DATACLK CYCLES.

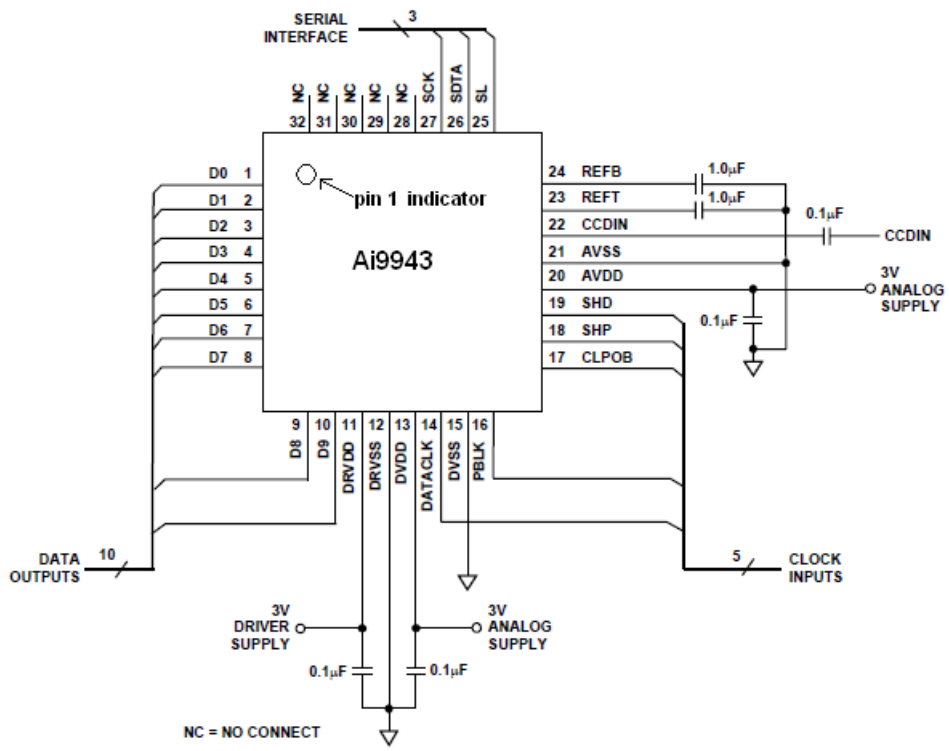
Applications Information

The Ai9943 is complete analog front end (AFE) products for digital still camera and camcorder applications. As shown in the "*CCD Mode Block Diagram"* , the CCD image (pixel) data is buffered and sent to the Ai9943 analog input through a series input capacitor. The Ai9943 performs the dc restoration, CDS, gain adjustment, black level correction, and analog-to-digital conversion. The Ai9943's digital output data is then processed by the image processing ASIC. The internal registers of the Ai9943—used to control gain, offset level, and other functions—are programmed by the ASIC or microprocessor through a 3-wire serial digital interface. A system timing generator provides the clock signals for both the CCD and the AFE.

System Applications Diagram



Recommended Circuit Configuration for CCD Mode



Internal Power-on Reset Circuitry

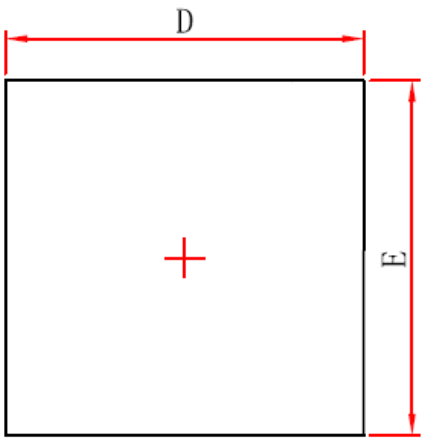
After power-on, the Ai9943 automatically resets all internal registers and performs internal calibration procedures. This takes approximately 1 ms to complete. During this time, normal clock signals and serial write operations may occur. However, serial register writes are ignored until the internal reset operation is completed.

Grounding and Decoupling Recommendations

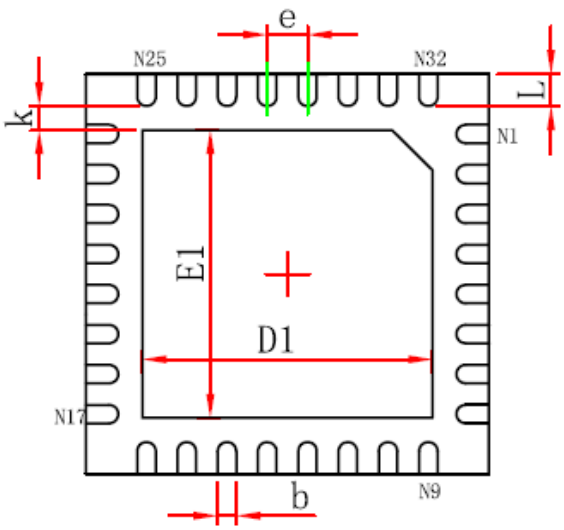
As shown in the "*Recommended Circuit Configuration for CCD Mode"* on the previous page, a single ground plane is recommended for the Ai9943. This ground plane should be as continuous as possible. This ensures that all analog decoupling capacitors provide the lowest possible impedance path between the power and bypass pins and their respective ground pins. All decoupling capacitors should be located as close as possible to the package pins. A single clean power supply is recommended for the Ai9943, but a separate digital driver supply may be used for DRVDD (Pin 11). DRVDD should always be decoupled to DRVSS (Pin 12), which should be connected to the analog ground plane. Advantages of using a separate digital driver supply include using a lower voltage (2.7 V) to match levels with a 2.7 V ASIC, and reducing digital power dissipation and potential noise coupling. If the digital outputs must drive a load larger than 20 pF, buffering is the recommended method to reduce digital code transition noise. Alternatively, placing series resistors close to the digital output pins may also help reduce noise.

Note: The exposed pad on the bottom of the Ai9943 should be soldered to the GND plane of the printed circuit board.

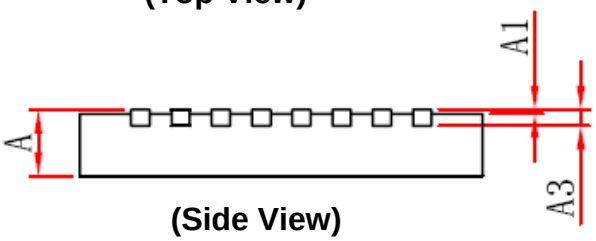
Package Dimension (***Ai9943:*** $QFNWB5\times5-32L(P0.50T0.75/0.85)$ **)**



(Top View)



(Bottom View)



(Side View)

SYMBOL	DIMENSIONS IN MILIMETERS		DIMENSIONS IN INCHES	
	MIN	MAX	MIN	MAX
A	0.700 / 0.800	0.800 / 0.900	0.028 / 0.031	0.031 / 0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF		0.008REF	
D	4.924	5.076	0.194	0.200
E	4.924	5.076	0.194	0.200
D1	3.300	3.500	0.130	0.138
E1	3.300	3.500	0.130	0.138
k	0.200MIN		0.008MIN	
b	0.180	0.300	0.007	0.012
e	0.500TYP		0.020TYP	
L	0.324	0.476	0.013	0.019