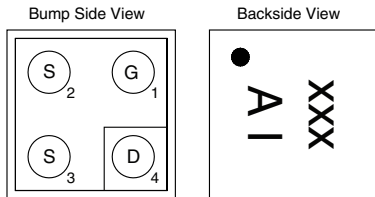




N-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω) Max.	I_D (A) ^a	Q_g (Typ.)
30	0.095 at $V_{GS} = 4.5$ V	2.5	3.7 nC
	0.105 at $V_{GS} = 2.5$ V	2.3	
	0.120 at $V_{GS} = 1.8$ V	2.2	
	0.165 at $V_{GS} = 1.5$ V	1.9	

MICRO FOOT



Device Marking: AI

xxx = Date/Lot Traceability Code

Ordering Information:

Si8808DB-T2-E1 (Lead (Pb)-free and Halogen-free)

FEATURES

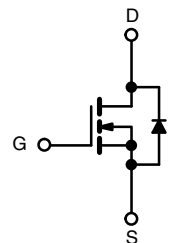
- TrenchFET[®] Power MOSFET
- Small 0.8 mm x 0.8 mm outline area
- Low 0.4 mm max. profile
- 30 V max. Rating and Low On-Resistance
- Material categorization:
For definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Load Switch
- High Speed Switching
- DC/DC Converters
- For Smart Phones, Tablet PCs and Mobile Computing



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V_{DS}	30	V	
Gate-Source Voltage	V_{GS}	± 8		
Continuous Drain Current ($T_J = 150$ °C)	I_D	$T_A = 25$ °C	2.5 ^a	A
		$T_A = 70$ °C	2 ^a	
		$T_A = 25$ °C	1.8 ^b	
		$T_A = 70$ °C	1.4 ^b	
Pulsed Drain Current ($t = 300$ μ s)	I_{DM}	10		
Continuous Source-Drain Diode Current	I_S	$T_A = 25$ °C	0.7 ^a	
		$T_A = 25$ °C	0.4 ^b	
Maximum Power Dissipation	P_D	$T_A = 25$ °C	0.9 ^a	W
		$T_A = 70$ °C	0.6 ^a	
		$T_A = 25$ °C	0.5 ^b	
		$T_A = 70$ °C	0.3 ^b	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature) ^c		260		

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{a, d}	R_{thJA}	105	135	°C/W	
Maximum Junction-to-Ambient ^{b, e}		200	260		

Notes:

- Surface mounted on 1" x 1" FR4 board with full copper, $t = 5$ s.
- Surface mounted on 1" x 1" FR4 board with minimum copper, $t = 5$ s.
- Refer to IPC/JEDEC (J-STD-020), no manual or hand soldering.
- Maximum under steady state conditions is 185 °C/W.
- Maximum under steady state conditions is 330 °C/W.

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	30			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		31		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 2.3		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	0.4		0.9	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 8\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 30\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 55\text{ }^\circ\text{C}$			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}$, $V_{GS} = 4.5\text{ V}$	5			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}$, $I_D = 1\text{ A}$		0.071	0.095	Ω
		$V_{GS} = 2.5\text{ V}$, $I_D = 1\text{ A}$		0.079	0.105	
		$V_{GS} = 1.8\text{ V}$, $I_D = 1\text{ A}$		0.090	0.120	
		$V_{GS} = 1.5\text{ V}$, $I_D = 0.5\text{ A}$		0.105	0.165	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}$, $I_D = 1\text{ A}$		10		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 15\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		330		pF
Output Capacitance	C_{oss}			40		
Reverse Transfer Capacitance	C_{rss}			16		
Total Gate Charge	Q_g	$V_{DS} = 15\text{ V}$, $V_{GS} = 8\text{ V}$, $I_D = 1\text{ A}$		6.5	10	nC
		$V_{DS} = 15\text{ V}$, $V_{GS} = 4.5\text{ V}$, $I_D = 1\text{ A}$		3.7	5.6	
Q_{gs}			0.53			
Gate-Drain Charge	Q_{gd}			0.52		
Gate Resistance	R_g	$f = 1\text{ MHz}$		3.1		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}$, $R_L = 15\text{ }\Omega$ $I_D \cong 1\text{ A}$, $V_{GEN} = 8\text{ V}$, $R_g = 1\text{ }\Omega$		5	10	ns
Rise Time	t_r			12	25	
Turn-Off Delay Time	$t_{d(off)}$			15	30	
Fall Time	t_f			6	15	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}$, $R_L = 15\text{ }\Omega$ $I_D \cong 1\text{ A}$, $V_{GEN} = 4.5\text{ V}$, $R_g = 1\text{ }\Omega$		7	15	
Rise Time	t_r			15	30	
Turn-Off Delay Time	$t_{d(off)}$			22	40	
Fall Time	t_f			10	20	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_A = 25\text{ }^\circ\text{C}$			0.7	A
Pulse Diode Forward Current	I_{SM}				10	
Body Diode Voltage	V_{SD}	$I_S = 1\text{ A}$, $V_{GS} = 0\text{ V}$		0.7	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 1\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^\circ\text{C}$		11	20	ns
Body Diode Reverse Recovery Charge	Q_{rr}			5	10	nC
Reverse Recovery Fall Time	t_a			7		ns
Reverse Recovery Rise Time	t_b			4		

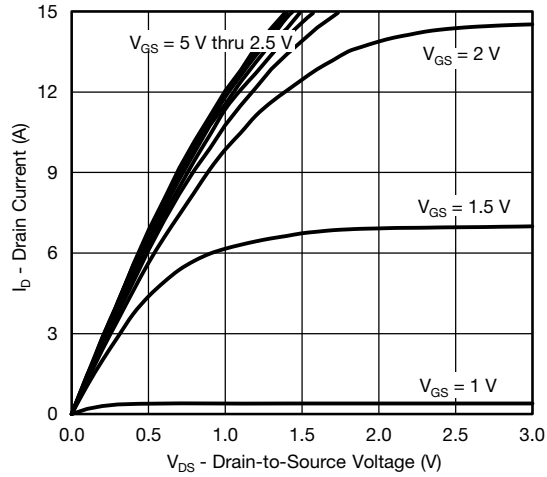
Notes:

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing.

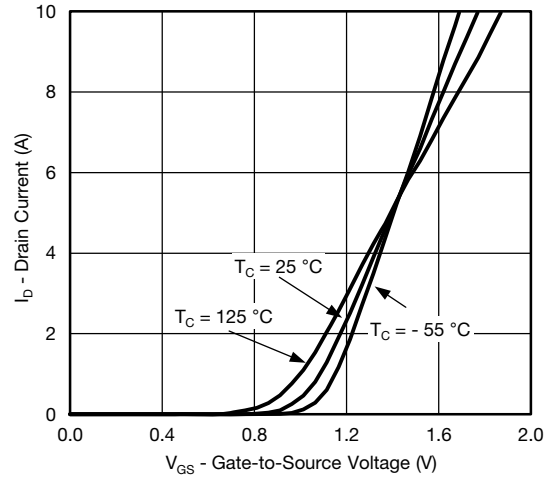
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



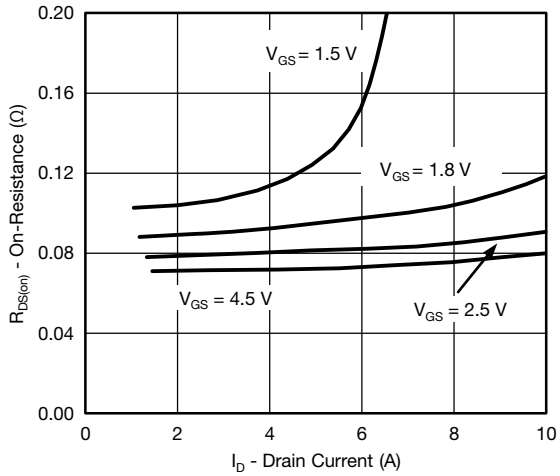
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



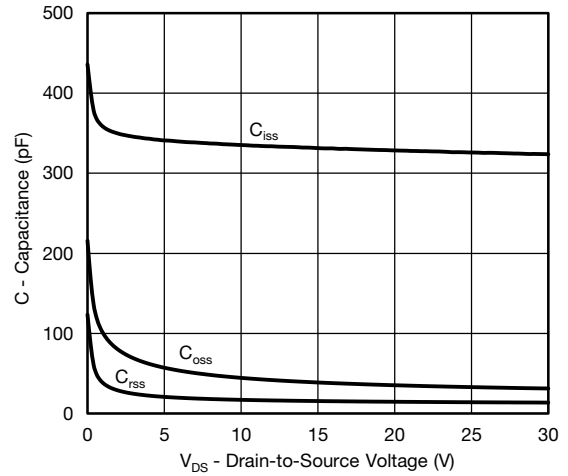
Output Characteristics



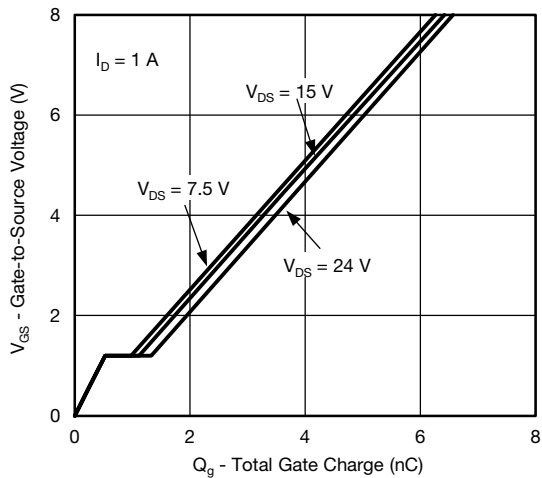
Transfer Characteristics



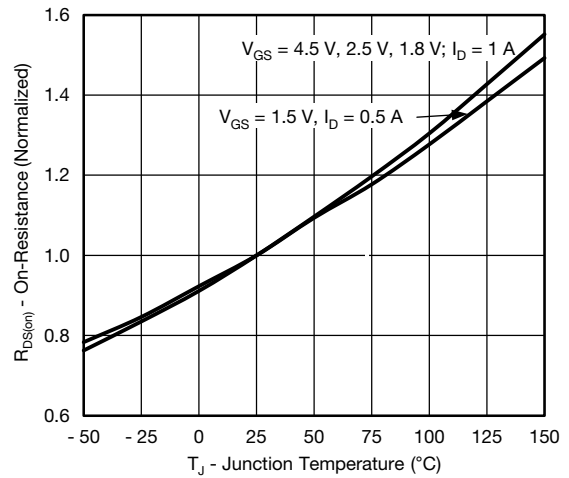
On-Resistance vs. Drain Current



Capacitance

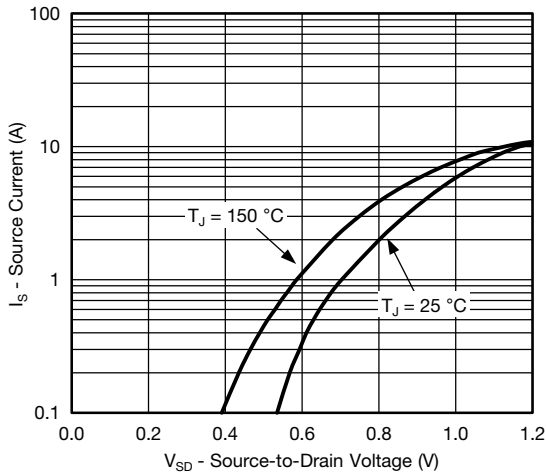


Gate Charge

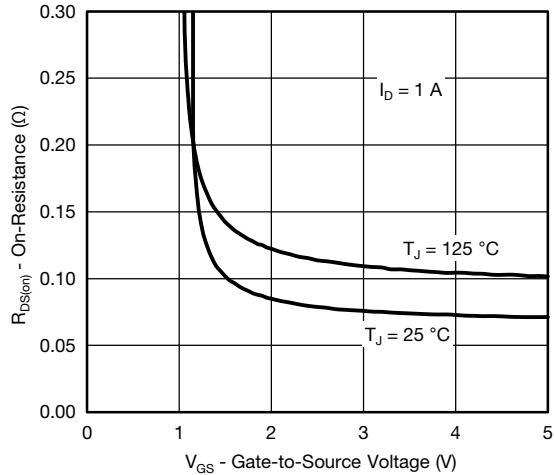


On-Resistance vs. Junction Temperature

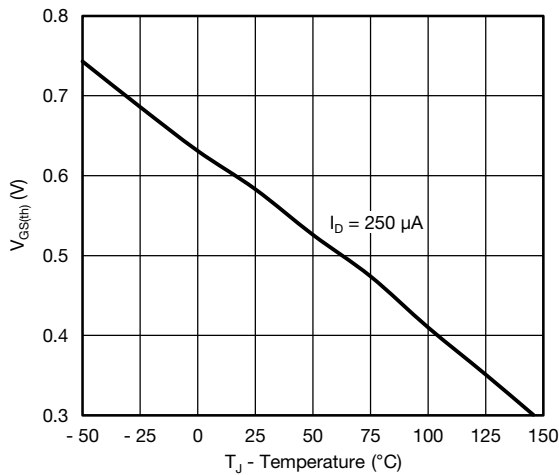
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



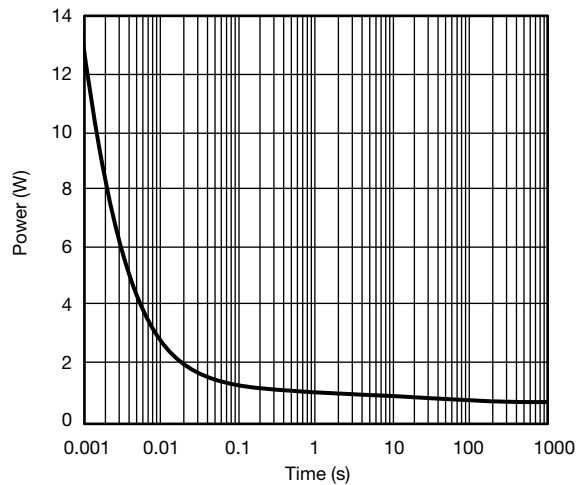
Source-Drain Diode Forward Voltage



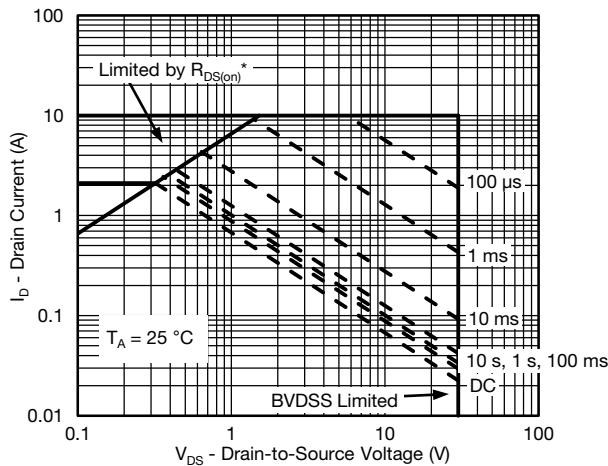
On-Resistance vs. Gate-to-Source Voltage



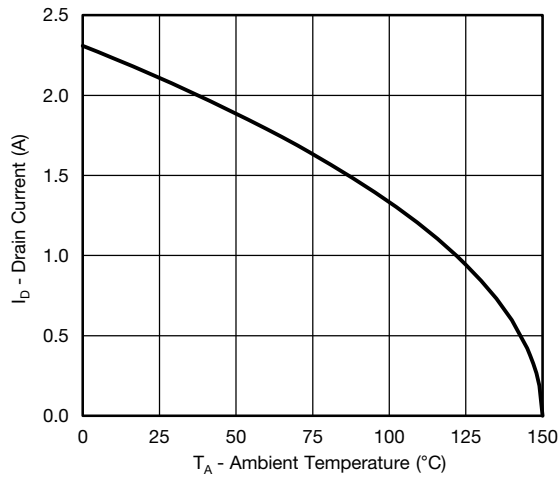
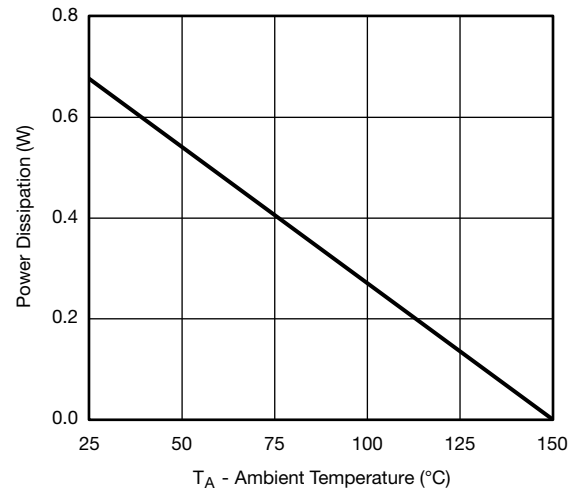
Threshold Voltage



Single Pulse Power (Junction-to-Ambient)



Safe Operating Area, Junction-to-Ambient


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Current Derating*

Power Derating

Note:

When mounted on 1" x 1" FR4 with full copper.

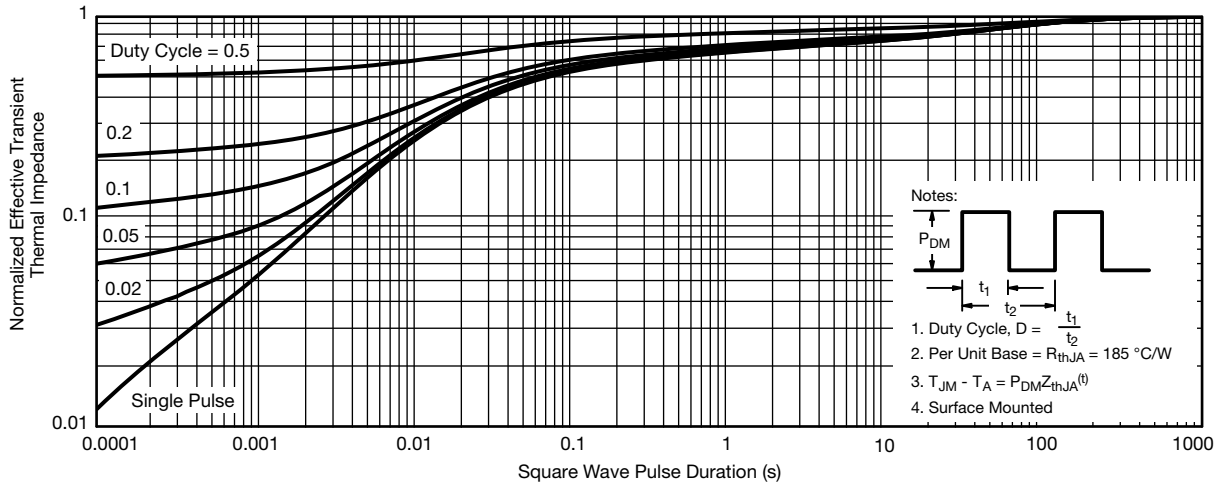
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-ambient thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

Si8808DB

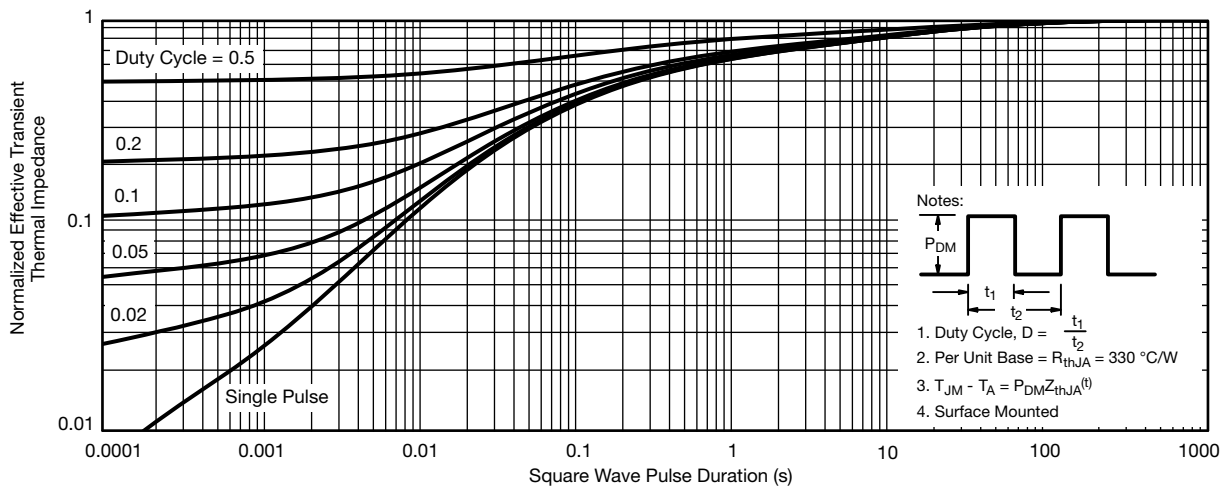
Vishay Siliconix



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient (On 1" x 1" FR4 board with maximum copper)

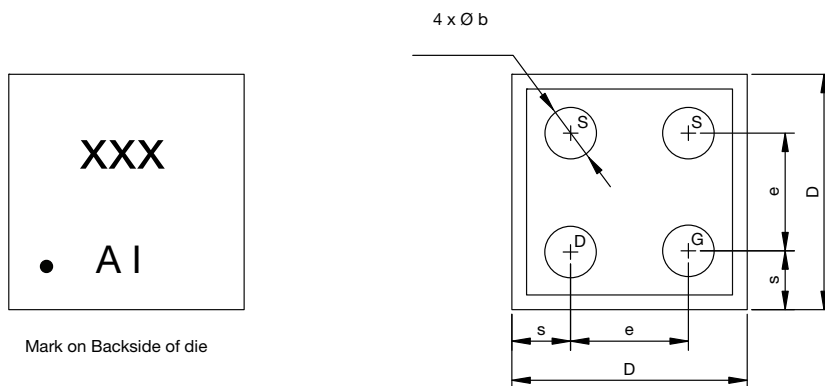


Normalized Thermal Transient Impedance, Junction-to-Ambient (On 1" x 1" FR4 board with minimum copper)



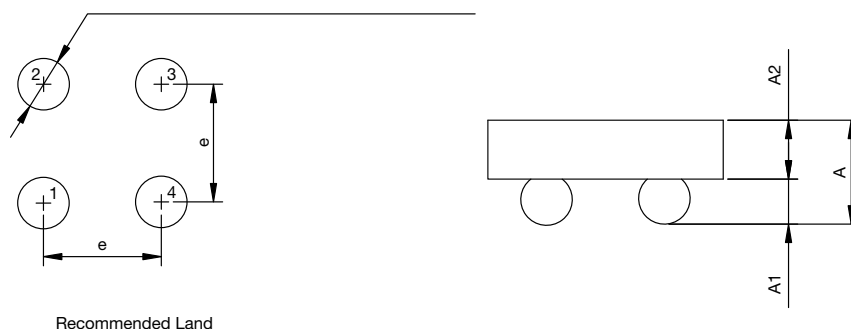
PACKAGE OUTLINE

MICRO FOOT 0.8 mm x 0.8 mm: 4-BUMP (2 x 2, 0.4 mm PITCH)



Mark on Backside of die

4 x Ø 0.205 to 0.225 Note 4
Solder Mask ~ Ø 0.215



Recommended Land

Notes (Unless otherwise specified):

1. All dimensions are in millimeters.
2. Four (4) solder bumps are lead (Pb)-free 95.5Sn/3.5Ag/0.7Cu with diameter Ø 0.165 mm to Ø 0.185 mm.
3. Backside surface is coated with a Ti/Ni/Ag layer.
4. Non-solder mask defined copper landing pad.
5. • is location of pin 1.

Dim.	Millimeters ^a			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.314	0.357	0.400	0.0124	0.0141	0.0157
A ₁	0.127	0.157	0.187	0.0050	0.0062	0.0074
A ₂	0.187	0.200	0.213	0.0074	0.0079	0.0084
b	0.165	0.175	0.185	0.0064	0.0068	0.0072
e		0.400			0.0157	
s	0.180	0.200	0.220	0.0070	0.0078	0.0086
D	0.760	0.800	0.840	0.0299	0.0314	0.0330

Notes:

- a. Use millimeters as the primary measurement.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62547.



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