- **High-Performance Floating-Point DSP**
  - **TMX320C32-60 (5 V)**
    33-ns Instruction Cycle Time
    330 MOPS, 60 MFLOPS, 30 MIPS
  - **TMS320C32-50 (5 V)**
    40-ns Instruction Cycle Time
    275 MOPS, 50 MFLOPS, 25 MIPS
  - **TMS320C32-40 (5 V)**
    50-ns Instruction Cycle Time
    220 MOPS, 40 MFLOPS, 20 MIPS
  - **TMX320LC32-40 (3.3 V)**
    50-ns Instruction Cycle Time
    220 MOPS, 40 MFLOPS, 20 MIPS
- **32-Bit High-Performance CPU**
- **16-/32-Bit Integer and 32-/40-Bit Floating-Point Operations**
- **32-Bit Instruction Word, 24-Bit Addresses**
- **Two 256 × 32-Bit Single-Cycle, Dual-Access On-Chip RAM Blocks**
- **Flexible Boot-Program Loader**
- **On-Chip Memory-Mapped Peripherals:**
  - **One Serial Port**
  - **Two 32-Bit Timers**
  - **Two-Channel Direct Memory Access (DMA) Coprocessor With Configurable Priorities**
- **Enhanced External Memory Interface That Supports 8-/16-/32-Bit Wide External RAM for Data Access and Program Execution From 16-/32-Bit Wide External RAM**
- **TMS320C30 and TMS320C31 Object Code Compatible**
- **Fabricated using 0.7 µm Enhanced Performance Implanted CMOS (EPIC™) Technology by Texas Instruments (TI™)**

- **144-Pin Plastic Quad Flat Package (PCM Suffix) 5 V**
- **144-Pin Thin Plastic Quad Flat Package (PGE Suffix) 3.3 V**
- **Eight Extended-Precision Registers**
- **Two Address Generators With Eight Auxiliary Registers and Two Auxiliary Register Arithmetic Units (ARAUs)**
- **Two Low-Power Modes**
- **Two- and Three-Operand Instructions**
- **Parallel Arithmetic Logic Unit (ALU) and Multiplier Execution in a Single Cycle**
- **Block-Repeat Capability**
- **Zero-Overhead Loops With Single-Cycle Branches**
- **Conditional Calls and Returns**
- **Interlocked Instructions for Multiprocessing Support**
- **One External Pin, PRGW, That Configures the External-Program-Memory Width to 16 or 32 Bits**
- **Two Sets of Memory Strobes ($\overline{\text{STRB0}}$ and $\overline{\text{STRB1}}$) and One I/O Strobe ($\overline{\text{IOSTRB}}$) Allow Zero-Glue Logic Interface to Two Banks of Memory and One Bank of External Peripherals**
- **Separate Bus-Control Registers for Each Strobe-Control Wait-State Generation, External Memory Width, and Data Type Size**
- **$\overline{\text{STRB0}}$ and $\overline{\text{STRB1}}$ Memory Strobes Handle 8-, 16-, or 32-Bit External Data Accesses (Reads and Writes)**
- **Multiprocessor Support Through the $\overline{\text{HOLD}}$ and $\overline{\text{HOLDA}}$ Signals Is Valid for All Strobes**

description

The TMS320C32 is the newest member of the TMS320C3x generation of digital signal processors (DSPs) from Texas Instruments. The TMS320C32 is an enhanced 32-bit floating-point processor manufactured in 0.7-µm triple-level-metal CMOS technology. The enhancements to the TMS320C3x architecture include a variable-width external-memory interface, faster instruction cycle time, power-down modes, two-channel DMA coprocessor with configurable priorities, flexible boot loader, relocatable interrupt-vector table, and edge- or level-triggered interrupts.

EPIC and TI are trademarks of Texas Instruments Incorporated.

TEXAS INSTRUMENTS

POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251–1443

1

pin assignments

PCM AND PGE PACKAGE †
(TOP VIEW)
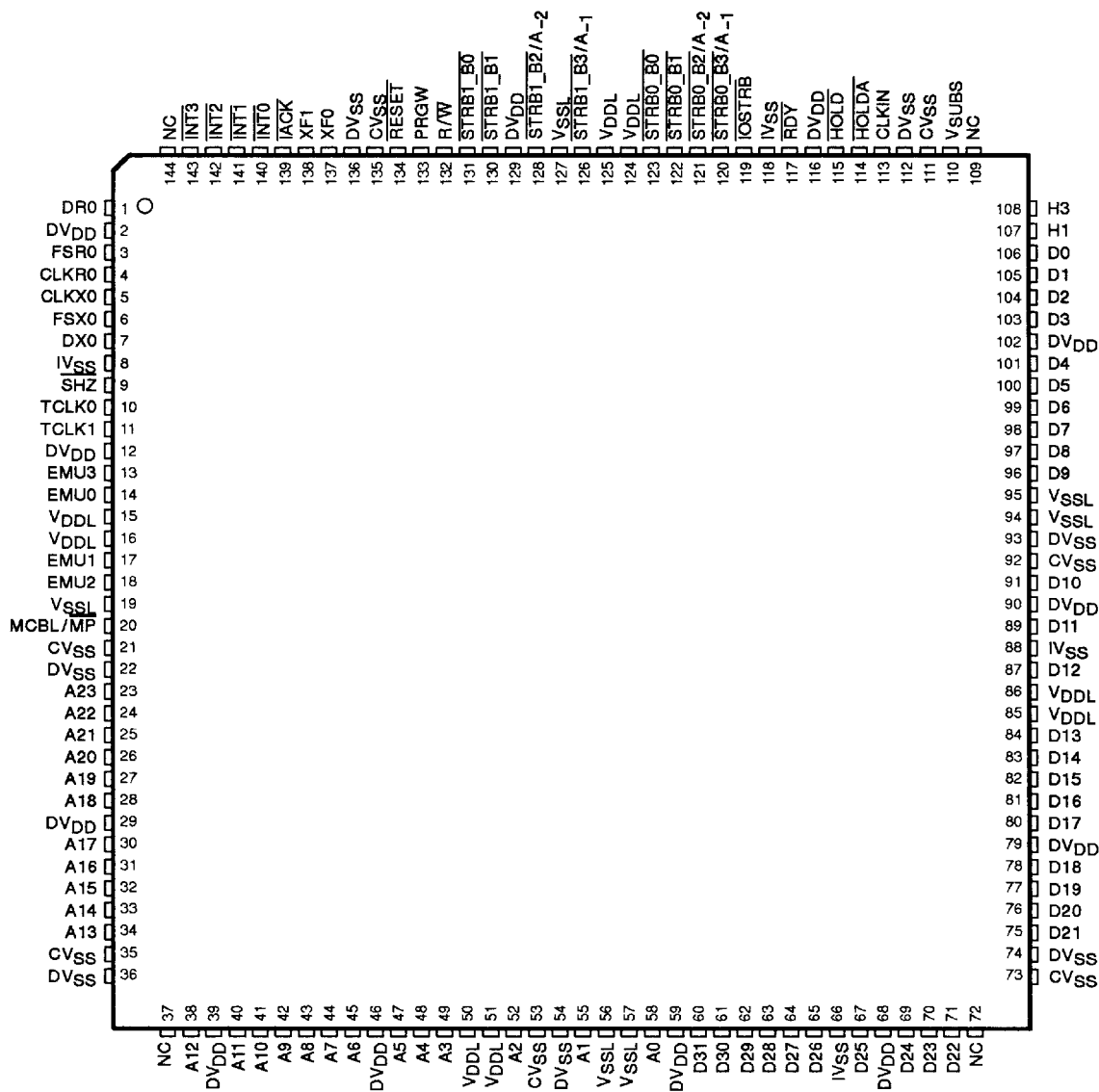
† NC=No internal connection

2

8961722 0097541 553

Pin Assignments

PIN NUMBER	PIN NAME	PIN NUMBER	PIN NAME	PIN NUMBER	PIN NAME	PIN NUMBER	PIN NAME	PIN NUMBER	PIN NAME
1	DR0	30	A17	59	DV_{DD}	88	IV_{SS}	117	$\overline{RDY}$
2	DV_{DD}	31	A16	60	D31	89	D11	118	IV_{SS}
3	FSR0	32	A15	61	D30	90	DV_{DD}	119	$\overline{IOSTRB}$
4	CLKR0	33	A14	62	D29	91	D10	120	$\overline{STRB0\_B3/A_{-1}}$
5	CLKX0	34	A13	63	D28	92	CV_{SS}	121	$\overline{STRB0\_B2/A_{-2}}$
6	FSX0	35	CV_{SS}	64	D27	93	DV_{SS}	122	$\overline{STRB0\_B1}$
7	DX0	36	DV_{SS}	65	D26	94	V_{SSL}	123	$\overline{STRB0\_B0}$
8	IV_{SS}	37	NC	66	IV_{SS}	95	V_{SSL}	124	V_{DDL}
9	$\overline{SHZ}$	38	A12	67	D25	96	D9	125	V_{DDL}
10	TCLK0	39	DV_{DD}	68	DV_{DD}	97	D8	126	$\overline{STRB1\_B3/A_{-1}}$
11	TCLK1	40	A11	69	D24	98	D7	127	V_{SSL}
12	DV_{DD}	41	A10	70	D23	99	D6	128	$\overline{STRB1\_B2/A_{-2}}$
13	EMU3	42	A9	71	D22	100	D5	129	DV_{DD}
14	EMU0	43	A8	72	NC	101	D4	130	$\overline{STRB1\_B1}$
15	V_{DDL}	44	A7	73	CV_{SS}	102	DV_{DD}	131	$\overline{STRB1\_B0}$
16	V_{DDL}	45	A6	74	DV_{SS}	103	D3	132	$R/\overline{W}$
17	EMU1	46	DV_{DD}	75	D21	104	D2	133	PRGW
18	EMU2	47	A5	76	D20	105	D1	134	$\overline{RESET}$
19	V_{SSL}	48	A4	77	D19	106	D0	135	CV_{SS}
20	$MCBL/\overline{MP}$	49	A3	78	D18	107	H1	136	DV_{SS}
21	CV_{SS}	50	V_{DDL}	79	DV_{DD}	108	H3	137	XF0
22	DV_{SS}	51	V_{DDL}	80	D17	109	NC	138	XF1
23	A23	52	A2	81	D16	110	V_{SUBS}	139	$\overline{IACK}$
24	A22	53	CV_{SS}	82	D15	111	CV_{SS}	140	$\overline{INT0}$
25	A21	54	DV_{SS}	83	D14	112	DV_{SS}	141	$\overline{INT1}$
26	A20	55	A1	84	D13	113	CLKIN	142	$\overline{INT2}$
27	A19	56	V_{SSL}	85	V_{DDL}	114	$\overline{HOLDA}$	143	$\overline{INT3}$
28	A18	57	V_{SSL}	86	V_{DDL}	115	$\overline{HOLD}$	144	NC
29	DV_{DD}	58	A0	87	D12	116	DV_{DD}		

8961722 0097542 49T

pin functions

This section provides signal descriptions for the TMS320C32 device. The following table lists each signal, the number of pins, operating modes, and a brief signal description. The table below groups the signals according to their function.

TMS320C32 Pin Functions

PIN NAME	NO.	TYPE†	DESCRIPTION	CONDITIONS WHEN SIGNAL IS IN HIGH Z‡		
EXTERNAL-BUS INTERFACE (70 PINS)						
D31–D0	32	I/O/Z	32-bit data port of the external-bus interface	S	H	R
A23–A0	24	O/Z	24-bit address port of the external-bus interface	S	H	R
R/$\overline{W}$	1	O/Z	Read/write for external-memory interface. R/$\overline{W}$ is high when a read is performed and low when a write is performed over the parallel interface.	S	H	R
$\overline{IOSTRB}$	1	O/Z	External-peripheral I/O strobe for the external-memory interface	S	H	
$\overline{STRB0\_B3}/A_{-1}$	1	O/Z	External-memory access strobe 0, byte enable 3 for 32-bit external-memory interface and address pin for 8-bit and 16-bit external-memory interface	S	H	
$\overline{STRB0\_B2}/A_{-2}$	1	O/Z	External-memory access strobe 0, byte enable 2 for 32-bit external-memory interface and address pin for 8-bit external-memory interface	S	H	
$\overline{STRB0\_B1}$	1	O/Z	External-memory access strobe 0, byte enable 1 for the external-memory interface	S	H	
$\overline{STRB0\_B0}$	1	O/Z	External-memory access strobe 0, byte enable 0 for the external-memory interface	S	H	
$\overline{STRB1\_B3}/A_{-1}$	1	O/Z	External-memory access strobe 1, byte enable 3 for 32-bit external-memory interface and address pin for 8-bit and 16-bit external-memory interface	S	H	
$\overline{STRB1\_B2}/A_{-2}$	1	O/Z	External-memory access strobe 1, byte enable 2 for 32-bit external-memory interface and address pin for 8-bit external-memory interface	S	H	
$\overline{STRB1\_B1}$	1	O/Z	External-memory access strobe 1, byte enable 1 for the external-memory interface	S	H	
$\overline{STRB1\_B0}$	1	O/Z	External-memory access strobe 1, byte enable 0 for the external-memory interface	S	H	
$\overline{RDY}$	1	I	Ready. RDY indicates that the external device is prepared for an external-memory interface transaction to complete.			
$\overline{HOLD}$	1	I	Hold signal for external-memory interface. When HOLD is a logic low, any ongoing transaction is completed. A23–A0, D31–D0, $\overline{IOSTRB}$, $\overline{STRB0\_Bx}$, $\overline{STRB1\_Bx}$, and R/$\overline{W}$ are placed in the high-impedance state, and all transactions over the external-memory interface are held until HOLD becomes a logic high or the NOHOLD bit of the STRB0 bus-control register is set.			
$\overline{HOLDA}$	1	O/Z	Hold acknowledge for external-memory interface. HOLDA is generated in response to a logic low on HOLD. HOLDA indicates that A23–A0, D31–D0, $\overline{IOSTRB}$, $\overline{STRB0\_Bx}$, $\overline{STRB1\_Bx}$, and R/$\overline{W}$ are in the high-impedance state and that all transactions over the memory are held. HOLDA is high in response to a logic high of HOLD or when the NOHOLD bit of the external bus-control register is set.	S		
PRGW	1	I	Program memory width select. When PRGW is a logic low, program is fetched as a single 32-bit word. When PRGW is a logic high, two 16-bit program fetches are performed to fetch a single 32-bit instruction word. The status of PRGW at device reset affects the reset value of the STRB0 and STRB1 bus-control register.			
CONTROL SIGNALS (9 PINS)						
$\overline{RESET}$	1	I	Reset. When RESET is a logic low, the device is in the reset condition. When RESET becomes a logic high, execution begins from the location specified by the reset vector.			
$\overline{INT3}$–$\overline{INT0}$	4	I	External interrupts			

† I = input, O = output, Z = high-impedance state
‡ S = $\overline{SHZ}$ active, H = $\overline{HOLD}$ active, R = $\overline{RESET}$ active

8961722 0097543 326

TMS320C32 Pin Functions (Continued)

PIN NAME	NO.	TYPE†	DESCRIPTION	CONDITIONS WHEN SIGNAL IS IN HIGH Z‡	
CONTROL SIGNALS (9 PINS) (CONTINUED)					
$\overline{IACK}$	1	O/Z	Interrupt acknowledge. $\overline{IACK}$ is set to a logic high by the IACK instruction. This signal can be used to indicate the beginning or end of an interrupt-service routine.	S	
MCBL/$\overline{MP}$	1	I	Microcomputer boot loader/microprocessor mode		
XF1 – XF0	2	I/O/Z	External flags. XF1 and XF0 are used as general-purpose I/Os or used to support interlocked-processor instructions.	S	R
SERIAL PORT SIGNALS (6 PINS)					
CLKX0	1	I/O/Z	Serial port 0 transmit clock. CLKX0 is the serial shift clock for the serial port 0 transmitter.	S	R
DX0	1	I/O/Z	Data transmit output. Serial port 0 transmits serial data on DX0.	S	R
FSX0	1	I/O/Z	Frame-synchronization pulse for transmit. The FSX0 pulse initiates the transmit-data process over DX0.	S	R
CLKR0	1	I/O/Z	Serial port 0 receive clock. CLKR0 is the serial shift clock for the serial port 0 receiver.	S	R
DR0	1	I/O/Z	Data receive. Serial port 0 receives serial data on DR0.	S	R
FSR0	1	I/O/Z	Frame-synchronization pulse for receive. The FSR0 pulse initiates the receive-data process over DR0.	S	R
TIMER SIGNALS (2 PINS)					
TCLK0	1	I/O/Z	Timer clock 0. As an input, TCLK0 is used by timer 0 to count external pulses. As an output, TCLK0 outputs pulses generated by timer 0.	S	R
TCLK1	1	I/O/Z	Timer clock 1. As an input, TCLK1 is used by timer 1 to count external pulses. As an output, TCLK1 outputs pulses generated by timer 1.	S	R
CLOCK SIGNALS (3 PINS)					
CLKIN	1	I	Input to the internal oscillator from an external clock source		
H1	1	O/Z	External H1 clock. H1 has a period equal to twice CLKIN.	S	
H3	1	O/Z	External H3 clock. H3 has a period equal to twice CLKIN.	S	
RESERVED (5 PINS)					
EMU0 – EMU2	3	I	Reserved for emulation. Use 18 kΩ – 22 kΩ pullup resistors to 5 V.		
EMU3	1	O/Z	Reserved for emulation	S	
$\overline{SHZ}$	1	I	Shutdown high impedance. When active, $\overline{SHZ}$ shuts down the 'C32 and places all 3-state I/O pins in the high-impedance state. $\overline{SHZ}$ is used for board-level testing to ensure that no dual-drive conditions occur. **CAUTION:** A low on $\overline{SHZ}$ corrupts 'C32 memory and register contents. Reset the device with $\overline{SHZ}$ high to restore it to a known operating condition.		
POWER/GROUND					
CV_{SS}	7	I	Ground		
DV_{SS}	7	I	Ground		
IV_{SS}	4	I	Ground		
DV_{DD}	12	I	+ 5 V_{dc} supply§		
V_{DDL}	8	I	+ 5 V_{dc} supply§		
V_{SSL}	6	I	Ground		
V_{SUBS}	1	I	Substrate, tie to ground		

† I = input, O = output, Z = high-impedance state
‡ S = $\overline{SHZ}$ active, H = $\overline{HOLD}$ active, R = $\overline{RESET}$ active
§ Recommended decoupling capacitor is 0.1 μF.

5

8961722 0097544 262

functional block diagram
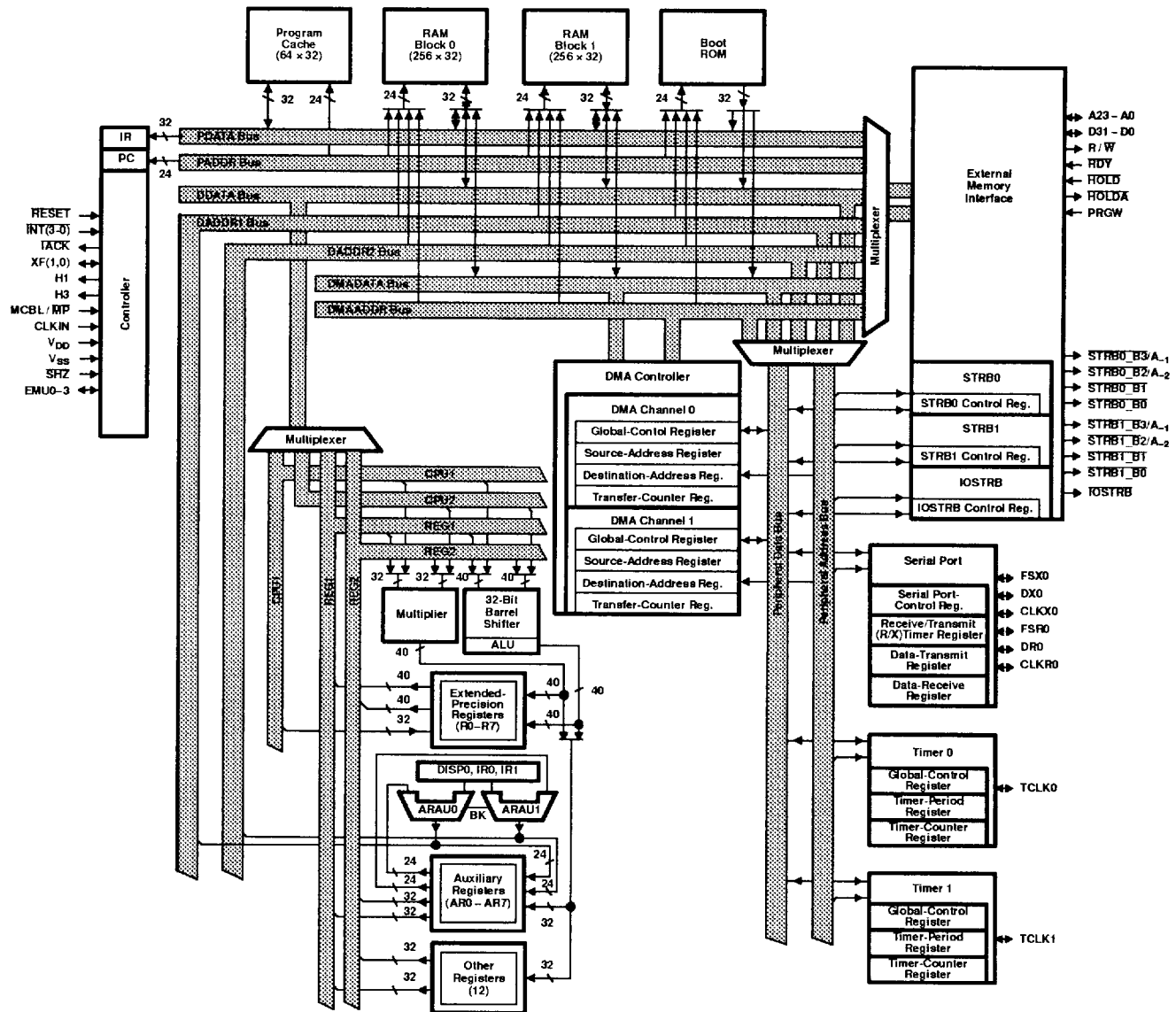
operation

Operation of the TMS320C32 is identical to the TMS320C30 and TMS320C31 digital signal processors, with the exception of an enhanced external memory interface and the addition of two CPU power-management modes.

external memory interface

The TMS320C32 has a configurable external-memory interface with a 24-bit address bus, a 32-bit data bus, and three independent multi-function strobes. The flexibility of this unique interface enables product designers to minimize external-memory chip count.

TEXAS
INSTRUMENTS

POST OFFICE BOX 1443 ● HOUSTON, TEXAS 77251–1443

external memory interface (continued)

Up to three mutually exclusive memory areas—one program area and two data areas—can be implemented. Each memory area's configuration is independent of the physical memory's width and independent of the other memory areas' configurations. See Figure 1.
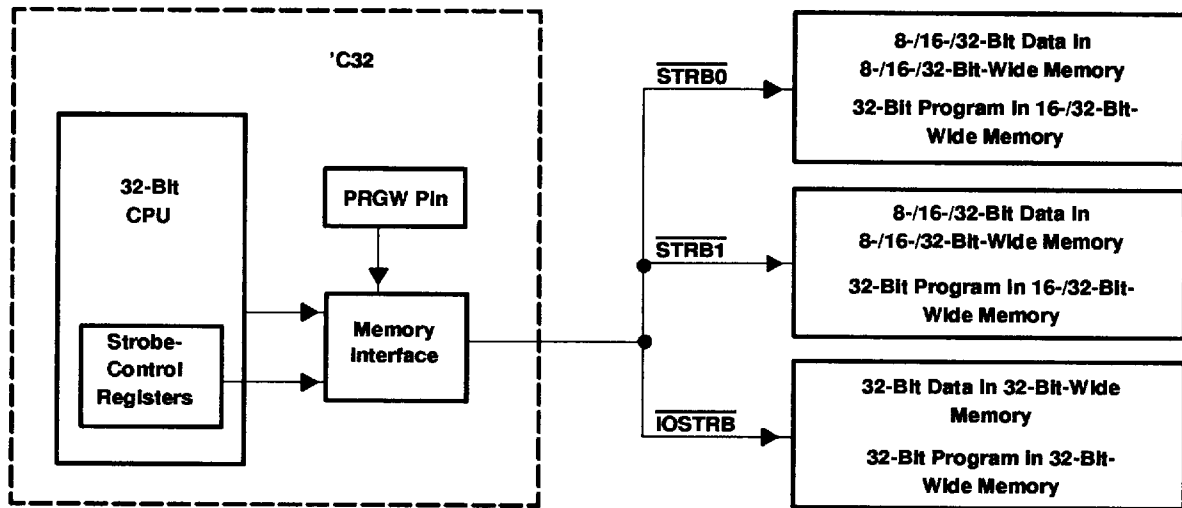
Figure 1. 'C32 External Memory Interface

The TMS320C32's external-memory configuration is controlled by a combination of hardware configuration and memory-mapped control registers and can be reconfigured dynamically. The signals that control external-memory configuration are the PRGW, STRB0, STRB1, and IOSTRB. The signals work as follows:

- The TMS320C32 is a 32-bit microprocessor, that is, the CPU operates on 32-bit program words. The external-memory interface provides the capability of fetching instructions as either 32-bit words or two 16-bit half words from consecutive addresses. Program memory width is 16 bits if the PRGW signal is high, 32 bits if the PRGW signal is low.

- STRB0 and STRB1 are sets of control signals, four signals each, that are mapped to specific ranges of external-memory addresses. When an address within one of these ranges is accessed by a read or write instruction (CPU or DMA), the corresponding set of control signals is activated. Figure 8 illustrates the TMS320C32's memory map, showing the address ranges for which the strobe signals become active.

8961722 0097546 035

external memory interface (continued)

The behavior of the $\overline{\text{STRB0}}$ and $\overline{\text{STRB1}}$ control signals is determined by the contents of the $\overline{\text{STRB0}}$ and $\overline{\text{STRB1}}$ control registers.

The $\overline{\text{STRB0}}$ and $\overline{\text{STRB1}}$ control registers each have a field that specifies the physical memory width (8, 16, or 32 bits) of the external-memory address ranges they control. Another field specifies the data width (8, 16, or 32 bits) of the data contained in those addresses. The values in these fields are not required to match. For example, a 32-bit-wide physical memory space can be configured to segment each 32-bit word into four consecutive 8-bit locations, each having its own address.

Each control-signal set has two pins ($\overline{\text{STRBx\_B2}}/\text{A}_{-2}$ and $\overline{\text{STRBx\_B3}}/\text{A}_{-1}$) that can act as either byte-enable (chip-select) pins or address pins, and two dedicated byte-enable (chip-select) pins ($\overline{\text{STRBx\_B0}}$ and $\overline{\text{STRBx\_B1}}$). The pins' functions are determined by the physical memory width specified in the corresponding control register:

8

⠿ ■■ 8961722 0097547 T71 ■■

external memory interface (continued)

- For 8-bit-wide physical memory, the $\overline{STRBx\_B2}/A_{-2}$ and $\overline{STRBx\_B3}/A_{-1}$ pins function as address pins (least significant address bits) and the $\overline{STRBx\_B0}$ pin functions as a byte-enable (chip-select) pin. $\overline{STRBx\_B1}$ is unused. See Figure 2.
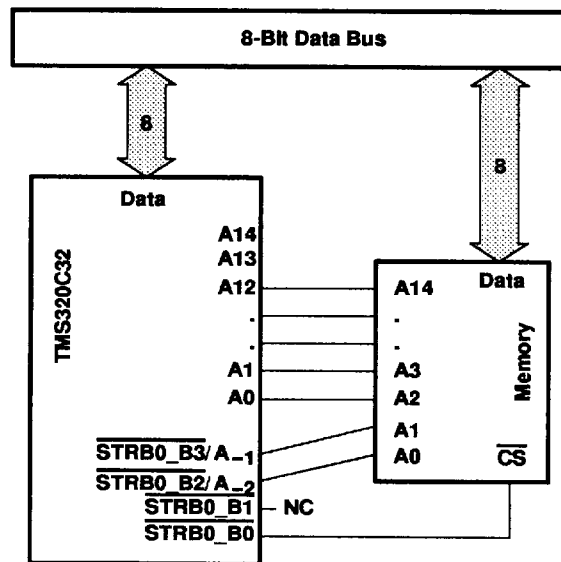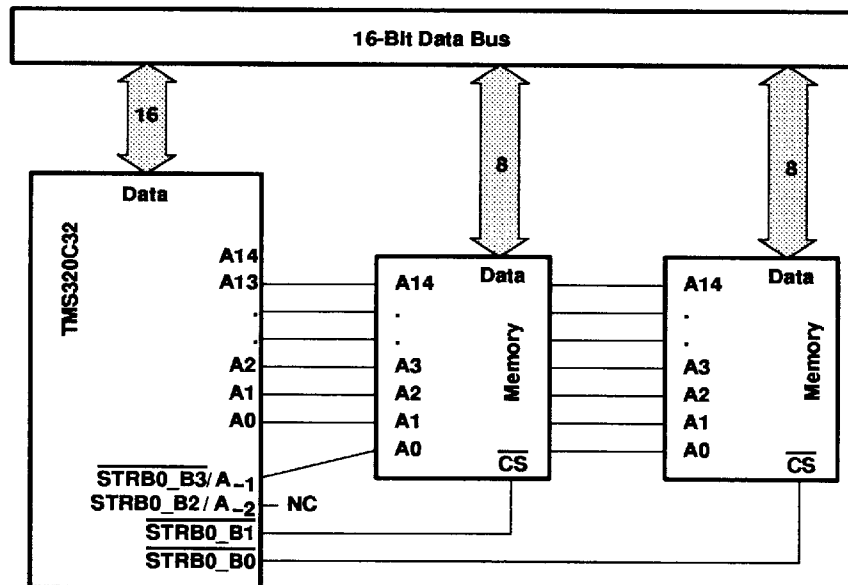

Figure 2. 'C32 With 8-Bit-Wide External Memory

- For 16-bit-wide physical memory, the $\overline{STRBx\_B3}/A_{-1}$ pin functions as an address pin (least significant address bits). The $\overline{STRBx\_B0}$ and $\overline{STRBx\_B1}$ pins function as byte-enable (chip-select) pins. $\overline{STRBx\_B2}/A_{-2}$ is unused. See Figure 3.

Figure 3. 'C32 With 16-Bit-Wide External Memory

9

external memory interface (continued)

- For 32-bit-wide physical memory, all $\overline{STRB0}$ and $\overline{STRB1}$ pins function as byte-enable (chip-select) pins. See Figure 4.
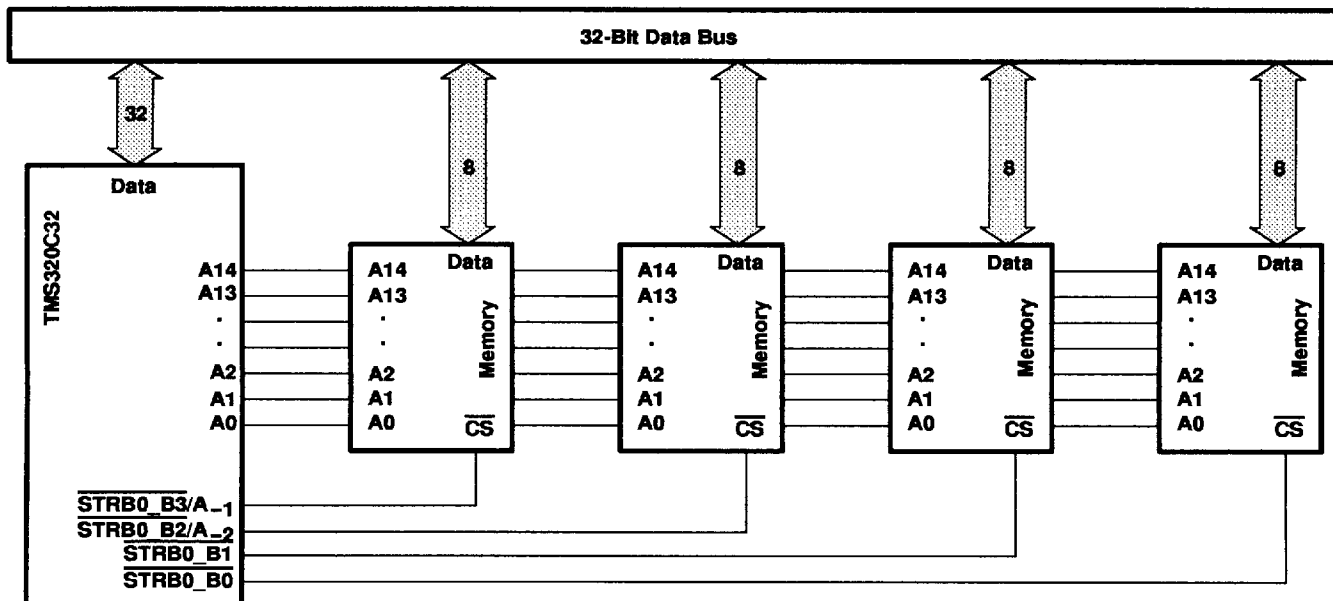

Figure 4. 'C32 With 32-Bit-Wide External Memory

For more detailed information and examples see *TMS320C32 Addendum to the TMS320C3x User's Guide* (literature number SPRU132B) and *Interfacing Memory to the TMS320C32 DSP Application Report* (literature number SPRA040).

- The $\overline{IOSTRB}$ control signal, like $\overline{STRB0}$ and $\overline{STRB1}$, also is mapped to a specific range of addresses but it is a single signal that can access only 32-bit data from 32-bit-wide memory. Its range of addresses appears in the TMS320C32's memory map, shown in Figure 8. The $\overline{IOSTRB}$ bus timing is different from the $\overline{STRB0}$ and $\overline{STRB1}$ bus timings to accommodate slower I/O peripherals.

8961722 0097549 844

external memory interface (continued)

examples

Figure 5 and Figure 6 show examples of external memory configurations that can be implemented using the TMS320C32's external memory interface. The first example has a 32-bit-wide external memory with 8- and 16-bit data areas and a 32-bit program area.
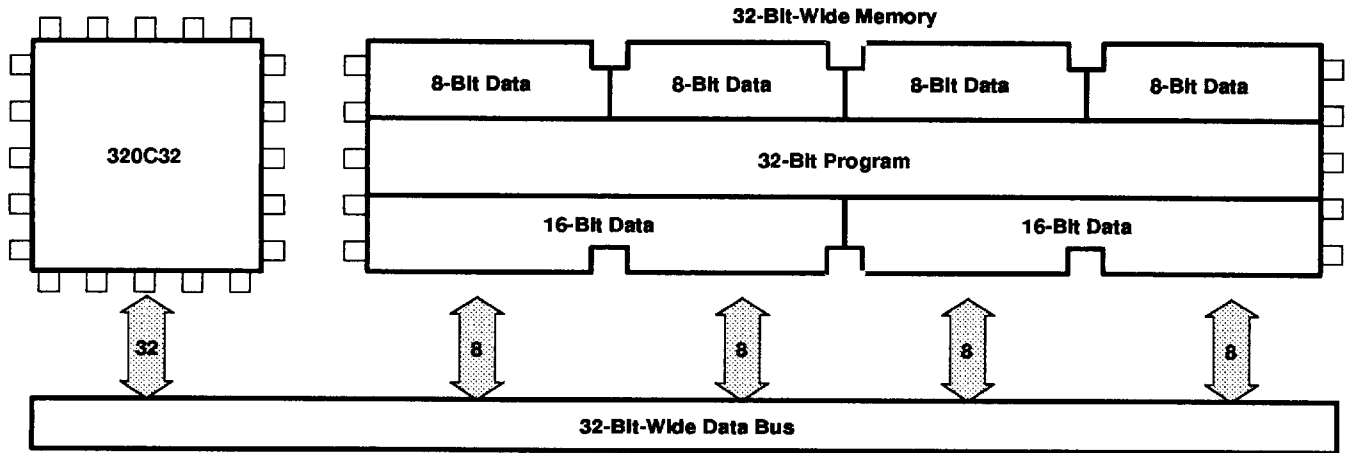

Figure 5. 'C32 With 32-Bit-Wide External Memory Configured With 8- and 16-Bit Data Areas and 32-Bit Program Memory

Figure 6 shows a configuration that can be implemented with 16-bit external memory. Note that 32-bit data and program words can be stored and retrieved as half words.
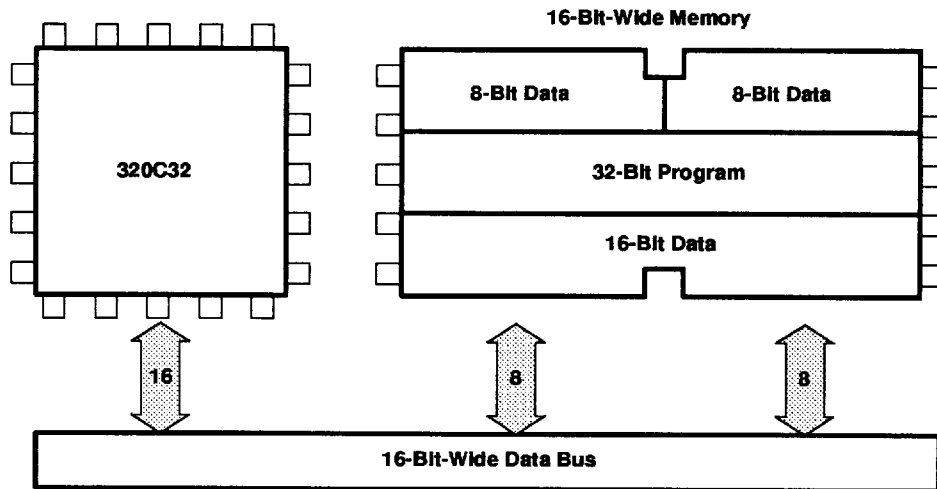

Figure 6. 'C32 With 16-Bit-Wide External Memory Configured With 8- and 16-Bit Data Areas and a 32-Bit Program Area

TEXAS INSTRUMENTS

POST OFFICE BOX 1443 ● HOUSTON, TEXAS 77251–1443

11

8961722 0097550 566

external memory interface (continued)

Figure 7 shows one possible configuration that can be implemented with 8-bit external memory. Note that program words, which are 32-bit, cannot be executed from 8-bit-wide memory.
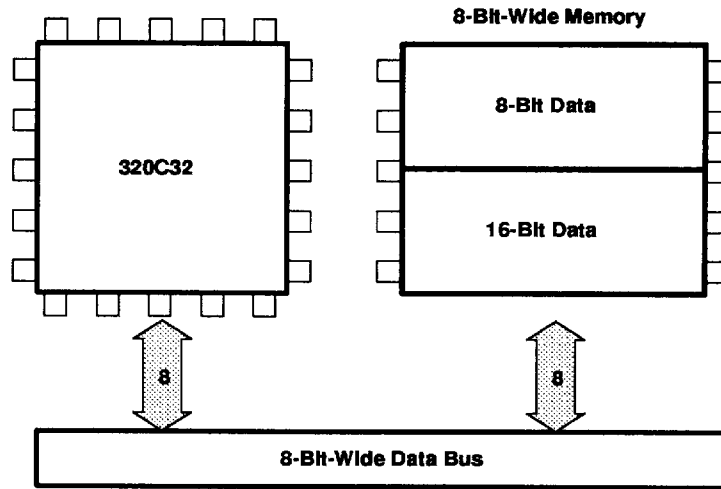
Figure 7. 'C32 With 8-Bit-Wide External Memory Configured With 8- and 16-Bit Data Areas

8961722 0097551 4T2

memory map

Figure 8 depicts the memory map for the TMS320C32. Refer to theTMS320C32 Addendum to the *TMS320C3x User's Guide* (literature number SPRU132B) for a detailed description of this memory mapping.
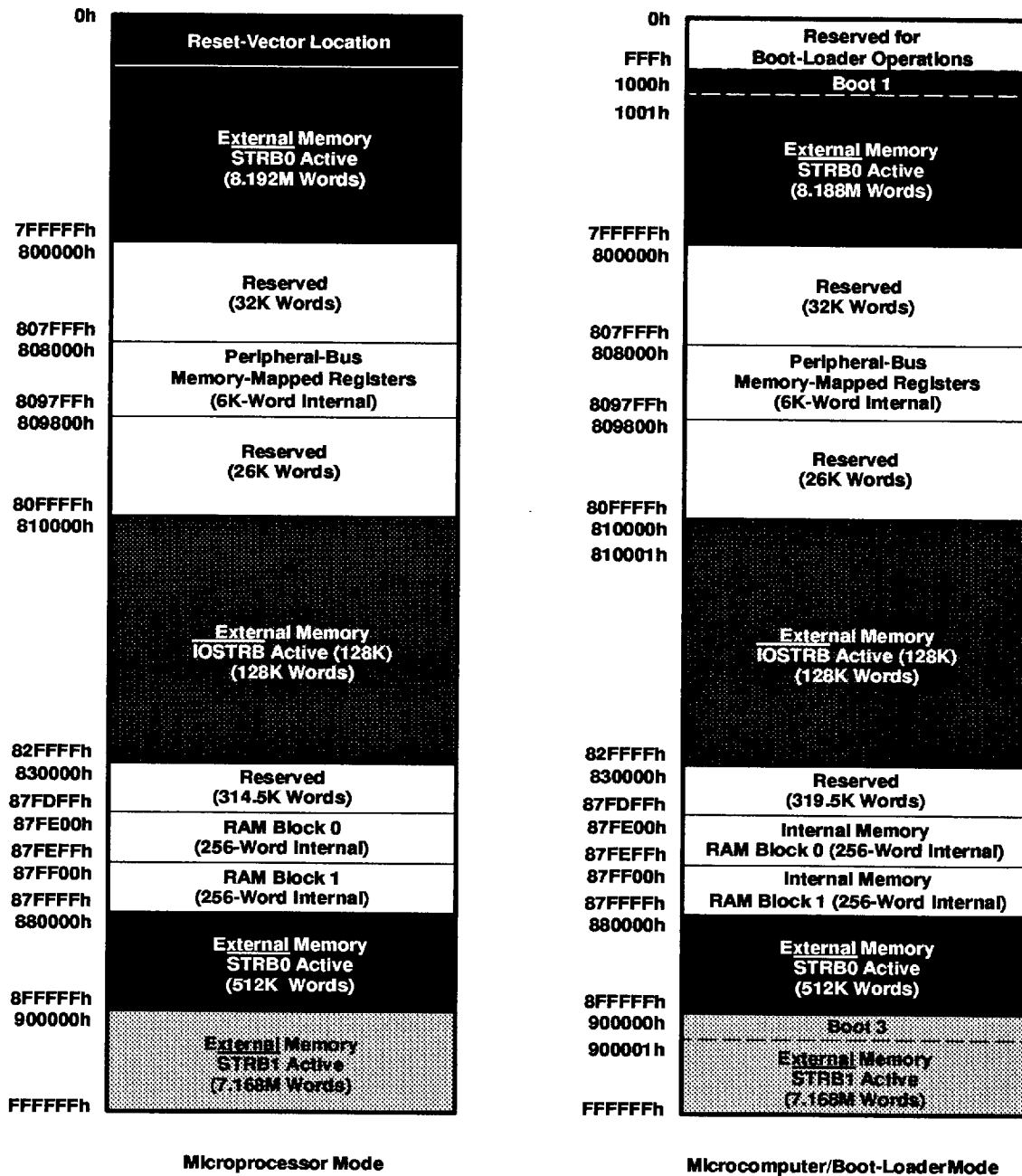

Figure 8. TMS320C32 Memory Map

power management

The TMS320C32 CPU has two power-management modes, IDLE2 and LOPOWER (low power). In IDLE2 mode, no instructions are executed and the CPU, peripherals, and memory retain their previous state while the external bus output pins are idle. During IDLE2 mode, the H1 clock signal is held high while the H3 clock signal is held low until one of the four external interrupts is asserted. In the LOPOWER mode, the CPU continues to execute instructions and the DMA continues to perform transfers, but at a reduced clock rate of the CLKIN frequency divided by 16 (that is, TMS320C32 with a 32-MHz CLKIN frequency performs the same as a 2-MHz TMS320C32 with an instruction cycle time of 1000 ns (1 MHz).

boot loader

The TMS320C32 flexible boot loader loads programs from the serial port, EPROM, or other standard non-volatile memory device. The boot-loader functionality of the TMS320C32 is equivalent to that of the TMS320C31, and has added modes to handle the data-type sizes and memory widths supported by the external memory interface. The memory-boot load supports data transfers with and without handshaking. The handshake mode allows synchronous transfer of programs by using two pins as data-acknowledge and data-ready signals.

peripherals

The TMS320C32 peripherals are comprised of one serial port, two timers, and two DMA channels. The serial port and timers are functionally identical to those in the TMS320C31 peripherals. The TMS320C32 two-channel DMA coprocessor has user-configurable priorities: CPU, DMA, or rotating between CPU and DMA.

14

: ▬ 8961722 0097553 275 ▬

peripherals (continued)

Figure 9 shows the TMS320C32's peripheral-bus control-register mapping.

Address	Register
808000h	DMA 0 Global Control
808004h	DMA 0 Source Address
808006h	DMA 0 Destination Address
808008h 808009h	DMA 0 Transfer Counter
808010h	DMA 1 Global Control
808014h	DMA 1 Source Address
808016h	DMA 1 Destination Address
808018h	DMA 1 Transfer Counter
808020h	Timer 0 Global Control
808024h	Timer 0 Counter
808028h	Timer 0 Period
808030h	Timer 1 Global Control
808034h	Timer 1 Counter
808038h	Timer 1 Period Register
808040h	Serial Port Global Control
808042h	FSX/DX/CLKX Port Control
808043h	FSR/DR/CLKR Port Control
808044h	R/X Timer Control
808045h	R/X Timer Counter
808046h	R/X Timer Period
808048h	Data Transmit
80804Ch	Data Receive
808050h 80805Fh	Reserved
808060h	IOSTRB-Bus Control
808064h	STRB0-Bus Control
808068h	STRB1-Bus Control
808069h 8097FFh	Reserved

Figure 9. Peripheral-Bus Memory-Mapped Registers

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251–1443

15

8961722 0097554 101

Interrupts

To reduce external logic and simplify the interface, the external interrupts can be either edge- or level-triggered. Unlike the fixed interrupt-trap vector-table location of the TMS320C30 and TMS320C31 devices, the TMS320C32 has a user-relocatable interrupt-trap vector table. The interrupt-trap vector table must start on a 256-word boundary. The interrupt and trap vector locations memory mapping is illustrated in Figure 10. The reset vector is fixed to address 0h as shown in Figure 8.

EA (ITTP) + 00h	Reserved
EA (ITTP) + 01h	INT0
EA (ITTP) + 02h	INT1
EA (ITTP) + 03h	INT2
EA (ITTP) + 04h	INT3
EA (ITTP) + 05h	XINT0
EA (ITTP) + 06h	RINT0
EA (ITTP) + 07h	Reserved
EA (ITTP) + 08h	Reserved
EA (ITTP) + 09h	TINT0
EA (ITTP) + 0Ah	TINT1
EA (ITTP) + 0Bh	DINT0
EA (ITTP) + 0Ch	DINT1
EA (ITTP) + 0Dh / EA (ITTP) + 1Fh	Reserved
EA (ITTP) + 20h	TRAP0
	. . .
EA (ITTP) + 3Bh	TRAP27
EA (ITTP) + 3Ch	TRAP28
EA (ITTP) + 3Dh	TRAP29
EA (ITTP) + 3Eh	TRAP30
EA (ITTP) + 3Fh	TRAP31

Figure 10. Reset, Interrupt, and Trap Vector/Branches Memory-Map Locations

TEXAS INSTRUMENTS

POST OFFICE BOX 1443 ● HOUSTON, TEXAS 77251–1443

16

8961722 0097555 048

absolute maximum ratings over specified temperature ranges (unless otherwise noted)†

	'C32	'LC32
Supply voltage range, V_{CC} (see Note 1)	−0.3 V to 7 V	−0.3 V to 5 V
Input voltage range	−0.3 V to 7 V	−0.3 V to 5 V
Output voltage range, V_O	−0.3 V to 7 V	−0.3 V to 5 V
Continuous power dissipation (see Note 2)	1.95 W	850 mW
Operating case temperature, T_C	0°C to 85°C	0°C to 85°C
Storage temperature range, T_{stg}	−55°C to 150°C	−55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to V_{SS}.
2. This value calculated for the 'C32-40. Actual operating power is less. This value was obtained under specially produced worst-case test conditions which are not sustained during normal device operation. These conditions consist of continuous parallel writes of a checkerboard pattern to the external bus at the maximum rate possible. See normal (I_{DD}) current specification in the electrical characteristics table and refer the *Calculation of TMS320C30 Power Dissipation Application Report* (literature number SPRA020).

recommended operating conditions (see Note 3)

			'320C32			'320LC32			UNIT
			MIN	NOM‡	MAX	MIN	NOM	MAX	
V_{DD}	Supply voltage (DV$_{DD}$, V$_{DDL}$)		4.75	5	5.25	3.13	3.3	3.47	V
V_{SS}	Supply voltage (CV$_{SS}$, V$_{SSL}$, IV$_{SS}$, DV$_{SS}$, V$_{SUBS}$)			0			0		V
V_{IH}	High-level input voltage	CLKIN	2.6		V_{DD} + 0.3§	2		V_{DD} + 0.3§	V
		All other inputs	2		V_{DD} + 0.3§	1.8		V_{DD} + 0.3§	V
V_{IL}	Low-level input voltage		−0.3§		0.8	−0.3§		0.6	V
I_{OH}	High-level output current				−300			−300	μA
I_{OL}	Low-level output current				2			2	mA
T_C	Operating case temperature		0		85	0		85	°C

‡ All nominal values are at V_{DD} = 5 V, T_A (ambient air temperature) = 25°C.
§ These values are derived from characterization and not tested.
NOTE 3: All input and output voltage levels are TTL compatible.

8961722 0097556 T84

electrical characteristics over recommended ranges of supply voltage (unless otherwise noted)†‡

PARAMETER		TEST CONDITIONS	'320C32			'320LC32			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{OH}	High-level output voltage	V_{DD} = MIN, I_{OH} = MAX	2.4	3		2.0	3		V
V_{OL}	Low-level output voltage	V_{DD} = MIN, I_{OL} = MAX		0.3	0.6§		0.3	0.4§	V
I_{OZ}	High-impedance state output current	V_{DD} = MAX	– 20		20	– 20		20	µA
I_I	Input current	V_I = V_{SS} to V_{DD}	– 10		10	– 10		10	µA
I_{DD}	Supply current (see Note 4)	f_X = 40 MHz		160	390		150	300	mA
		f_X = 50 MHz		200	425				
		f_X = 60 MHz		225	475				
		Standby		50			20		µA
C_I	Input capacitance	CLKIN			25			15	pF
		All other inputs			15¶			25¶	
C_O	Output capacitance				20¶			20¶	pF

Test conditions for I_{DD}: T_A = 25°C, V_{DD} = MAX, f_X = MAX‡. For Standby: IDLE2, CLKIN shut off.

† For 'C31, all nominal values are at V_{DD} = 5 V, T_A (ambient air temperature) = 25°C. For 'LC31, all nominal values are at V_{DD} = 3.3 V, T_A (ambient air temperature) = 25°C.
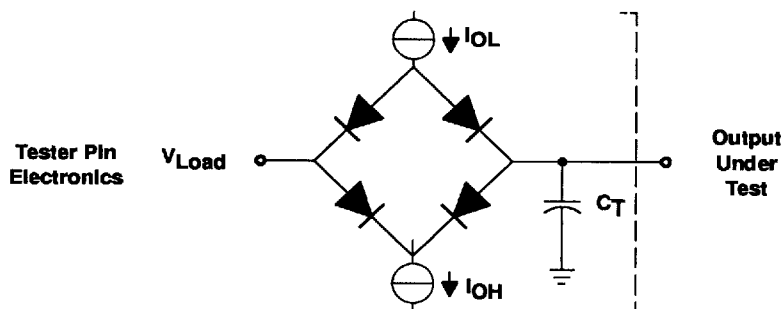‡ f_X is the input clock frequency.
§ V_{OL}(max) = 0.7 V for A(0:23)
¶ Assured by design but not tested
NOTE 4: Actual operating current is less than this maximum value (reference Note 2).

PARAMETER MEASUREMENT INFORMATION

Where: I_{OL} = 2 mA (all outputs)
         I_{OH} = 300 µA (all outputs)
         V_{Load} = 2.15 V
         C_T = 80-pF typical load-circuit capacitance

Figure 11. Test Load Circuit

8961722 0097557 910

PARAMETER MEASUREMENT INFORMATION (CONTINUED)

signal-transition levels for 'C32 (see Figure 12 and Figure 13)

TTL-level outputs are driven to a minimum logic-high level of 2.4 V and to a maximum logic-low level of 0.6 V. Output transition times are specified in the following paragraph.

For a high-to-low transition on an output signal, the level at which the output is said to be no longer high is 2 V and the level at which the output is said to be low is 1 V. For a low-to-high transition, the level at which the output is said to be no longer low is 1 V and the level at which the output is said to be high is 2 V (see Figure 12).
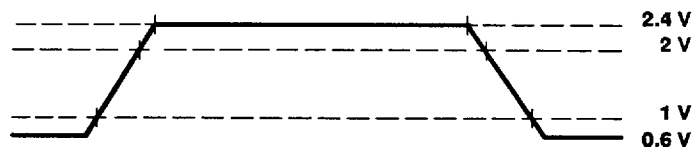

Figure 12. 'LC32 Output Levels

Transition times for TTL-compatible inputs are specified as follows. For a high-to-low transition on an input signal, the level at which the input is said to be no longer high is 2 V and the level at which the input is said to be low is 0.8 V. For a low-to-high transition on an input signal, the level at which the input is said to be no longer low is 0.8 V and the level at which the input is said to be high is 2 V (see Figure 13).

Figure 13. 'LC32 Input Levels

8961722 0097558 857

PARAMETER MEASUREMENT INFORMATION (CONTINUED)

signal transition levels for 'LC32 (see Figure 14 and Figure 15)

Outputs are driven to a minimum logic-high level of 2 V and to a maximum logic-low level of 0.4 V. Output transition times are specified as follows:

- For a high-to-low transition on an output signal, the level at which the output is said to be no longer high is 2 V and the level at which the output is said to be low is 1 V.

- For a low-to-high transition, the level at which the output is said to be no longer low is 1 V and the level at which the output is said to be high is 2 V.
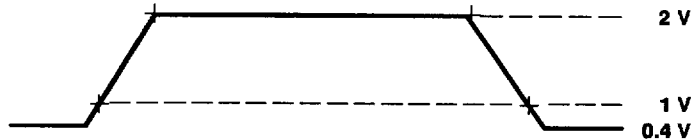

Figure 14. 'LC32 Output Levels

Transition times for inputs are specified as follows:

- For a high-to-low transition on an input signal, the level at which the input is said to be no longer high is 1.8 V and the level at which the input is said to be low is 0.6 V.

- For a low-to-high transition on an input signal, the level at which the input is said to be no longer low is 0.6 V and the level at which the input is said to be high is 1.8 V.

Figure 15. 'LC32 Input Levels

TEXAS
INSTRUMENTS
POST OFFICE BOX 1443 ● HOUSTON, TEXAS 77251–1443

20

∴ ▪ 8961722 0097559 793 ▪

PARAMETER MEASUREMENT INFORMATION (CONTINUED)

timing parameter symbology

Timing parameter symbols used in this document are in accordance with JEDEC Standard 100-A. Unless otherwise noted, in order to shorten the symbols, pin names and other related terminology have been abbreviated as follows:

A	A23–A0 when the physical-memory-width-bit field of the $\overline{\text{STRBx}}$ control register is set to 32 bits A23–A0 and $\overline{\text{STRBx\_B3}}/A_{-1}$ when the physical-memory-width-bit field of the $\overline{\text{STRBx}}$ control register is set to 16 bits A23–A0, $\overline{\text{STRBx\_B3}}/A_{-1}$, and $\overline{\text{STRBx\_B2}}/A_{-2}$ when the physical-memory-width-bit field of the $\overline{\text{STRBx}}$ control register is set to 8 bits
CI	CLKIN
RDY	$\overline{\text{RDY}}$
D	D(31–0)
H	H1, H3
IOS	$\overline{\text{IOSTRB}}$
P	$t_{c(H)}$
Q	$t_{c(CI)}$
RW	R/$\overline{\text{W}}$
S	$\overline{\text{STRBx\_B}(3-0)}$ when the physical-memory-width-bit field of the STRBx control register is set to 32 bits $\overline{\text{STRBx\_B}(1-0)}$ when the physical-memory-width-bit field of the STRBx control register is set to 16 bits $\overline{\text{STRBx\_B0}}$ when the physical-memory-width-bit field of the STRBx control register is set to 8 bits
XF	XF0 or XF1

8961722 0097560 405

operating characteristics for CLKIN, H1 and H3 [Q = t$_{c(CI)}$] (see Figure 16 and Figure 17)

NO.	PARAMETERS		TEST CONDITIONS	'C32-40 'LC32-40†		'C32-50		'C32-60		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
1	t$_{f(CI)}$‡	Fall time, CLKIN			5§		5§		4§	ns
2	t$_{w(CIL)}$‡	Pulse duration, CLKIN low	Q = min	9		7		6		ns
3	t$_{w(CIH)}$	Pulse duration, CLKIN high	Q = min	9‡§		8‡		6§		ns
4	t$_{r(CI)}$‡	Rise time, CLKIN			5§		5§		4§	ns
5	t$_{c(CI)}$‡	Cycle time, CLKIN		25	303	20	303	16.67	303	ns
6	t$_{f(H)}$	Fall time, H1/H3			3		3		3	ns
7	t$_{w(HL)}$	Pulse duration, H1/H3 low		Q-5		Q-5		Q-4		ns
8	t$_{w(HH)}$	Pulse duration, H1/H3 high		Q-6		Q-6		Q-5		ns
9	t$_{r(H)}$	Rise time, H1/H3			3		3		3	ns
9.1	t$_{d(HL-HH)}$	Delay time, H1/H3 low to H1/H3 high		0	4	0	4	0	4	ns
10	t$_{c(H)}$	Cycle time, H1/H3		50	606	40	606	33.33	606	ns

† 'LC32-40 data is preliminary
‡ Minimum CLKIN high-pulse duration at 3.3 MHz is 10 ns.
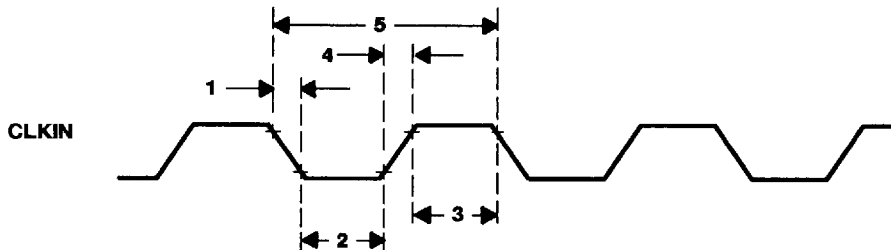§ Assured by design but not tested
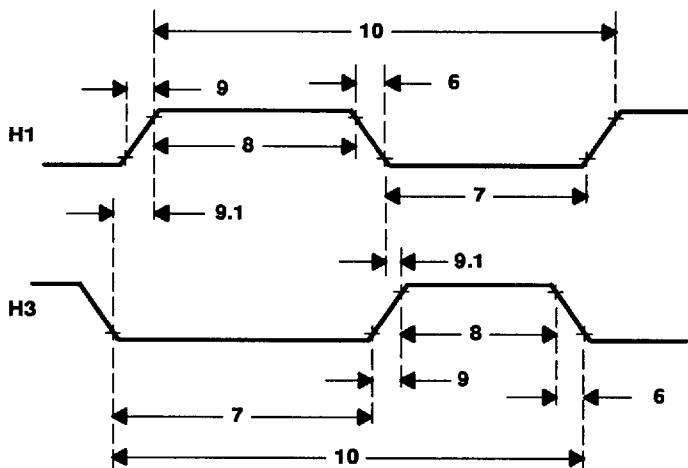

Figure 16. CLKIN Timing
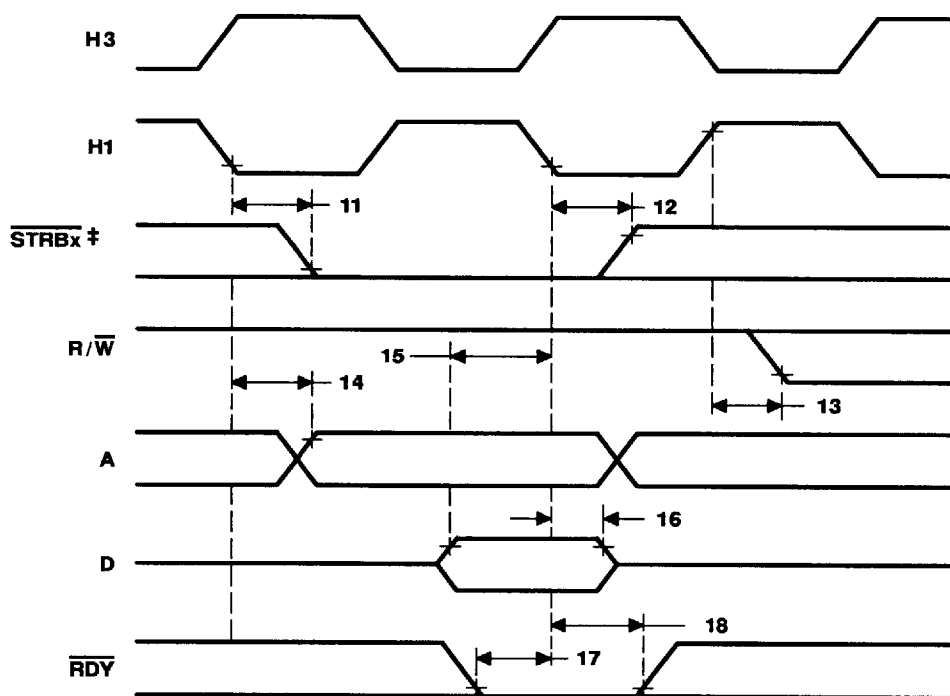

Figure 17. H1/H3 Timing

8961722 0097561 341

memory-read-cycle and memory-write-cycle timing (STRBx) (see Figure 18 and Figure 19)

NO.			'C32-40		'LC32-40		'C32-50		'C32-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
11	$t_{d(H1L-SL)}$	Delay time, H1 low to STRBx low	0†	11	0†	11	0†	9	0†	8	ns
12	$t_{d(H1L-SH)}$	Delay time, H1 low to STRBx high	0†	11	0†	11	0†	9	0†	8	ns
13	$t_{d(H1H-RWL)}$	Delay time, H1 high to R/W low (read)	0†	11	0†	11	0†	9	0†	8	ns
14	$t_{d(H1L-A)}$	Delay time, H1 low to A valid	0†	11	0†	11	0†	9	0†	8	ns
15	$t_{su(D)R}$	Setup time, D valid before H1 low (read)	13		14		10		9		ns
16	$t_{h(D)R}$	Hold time, D after H1 low (read)	0		0		0		0		ns
17	$t_{su(RDY)}$	Setup time, RDY before H1 low	21		21		19		17		ns
18	$t_{h(RDY)}$	Hold time, RDY after H1 low	0		0		0		0		ns
19	$t_{d(H1H-RWH)}$	Delay time, H1 high to R/W high (write)		11		11		9		8	ns
20	$t_{v(D)W}$	Valid time, D after H1 low (write)		17		17		14		12	ns
21	$t_{h(D)W}$	Hold time, D after H1 high (write)	0		0		0		0		ns
22	$t_{d(H1H-A)}$	Delay time, H1 high to A valid on back-to-back write cycles		11		11		9		8	ns

† Assured from characterization but not tested.

‡ STRBx remains low during back-to-back operations.

Figure 18. Memory-Read-Cycle Timing

8961722 0097562 288

memory-read-cycle and memory-write-cycle timing ($\overline{\text{STRBx}}$) (see Figure 18 and Figure 19) (continued)

Figure 19. Memory-Write-Cycle Timing
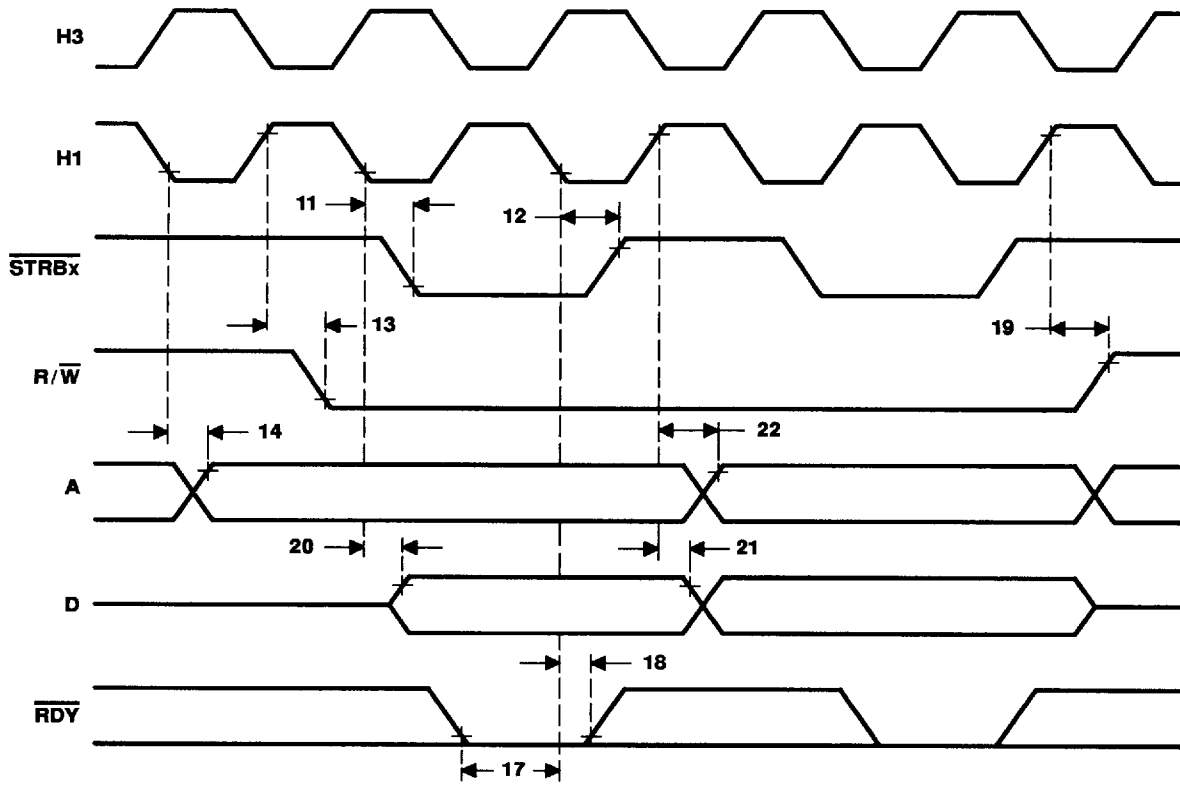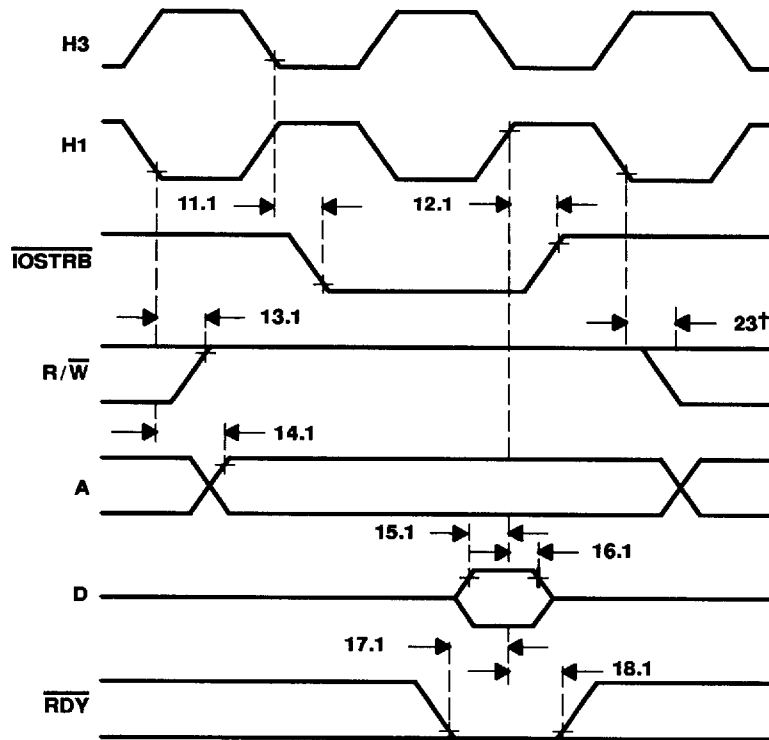
8961722 0097563 114

memory-read-cycle timing using IOSTRB (see Figure 20)

NO.			'C32-40 'LC32-40†		'C32-50		'C32-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
11.1	$t_{d(H3L-IOSL)}$	Delay time, H3 low to IOSTRB low	0‡	11	0‡	9	0‡	8	ns
12.1	$t_{d(H3L-IOSH)}$	Delay time, H3 low to IOSTRB high	0‡	11	0‡	9	0‡	8	ns
13.1	$t_{d(H1L-RWL)}$	Delay time, H1 low to R/W high	0‡	11	0‡	9	0‡	8	ns
14.1	$t_{d(H1L-A)}$	Delay time, H1 low to A valid	0‡	11	0‡	9	0‡	8	ns
15.1	$t_{su(D)R}$	Setup time, D before H1 high	13		10		9		ns
16.1	$t_{h(D)R}$	Hold time, D after H1 high	0		0		0		ns
17.1	$t_{su(RDY)}$	Setup time, RDY before H1 high	9		8		7		ns
18.1	$t_{h(RDY)}$	Hold time, RDY after H1 high	0		0		0		ns
23	$t_{d(H1L-RWH)}$	Delay time, H1 low to R/W low	0‡	11	0‡	9	0‡	8	ns

† 'LC32-40 data is preliminary
‡ Assured from characterization but not tested

† See Figure 21 and accompanying table

Figure 20. Memory-Read-Cycle Timing Using IOSTRB

8961722 0097564 050

memory-write-cycle timing using $\overline{\text{IOSTRB}}$ (see Figure 21)

NO.			'C32-40 'LC32-40†		'C32-50		'C32-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
11.1	$t_{d(H3L-IOSL)}$	Delay time, H3 low to $\overline{\text{IOSTRB}}$ low	0‡	11	0‡	9	0‡	8	ns
12.1	$t_{d(H3L-IOSH)}$	Delay time, H3 low to $\overline{\text{IOSTRB}}$ high	0‡	11	0‡	9	0‡	8	ns
13.1	$t_{d(H1L-RWL)}$	Delay time, H1 low to R/$\overline{\text{W}}$ high	0‡	11	0‡	9	0‡	8	ns
14.1	$t_{d(H1L-A)}$	Delay time, H1 low to A valid	0‡	11	0‡	9	0‡	8	ns
17.1	$t_{su(RDY)}$	Setup time, $\overline{\text{RDY}}$ before H1 high	9		8		7		ns
18.1	$t_{h(RDY)}$	Hold time, $\overline{\text{RDY}}$ after H1 high	0		0		0		ns
23	$t_{d(H1L-RWH)}$	Delay time, H1 low to R/$\overline{\text{W}}$ low	0‡	11	0‡	9	0‡	8	ns
24	$t_{v(D)W}$	Valid time, D after H1 high		17		14		12	ns
25	$t_{h(D)W}$	Hold time, D after H1 low	0		0		0		ns

† 'LC32-40 data is preliminary
‡ Assured from characterization but not tested
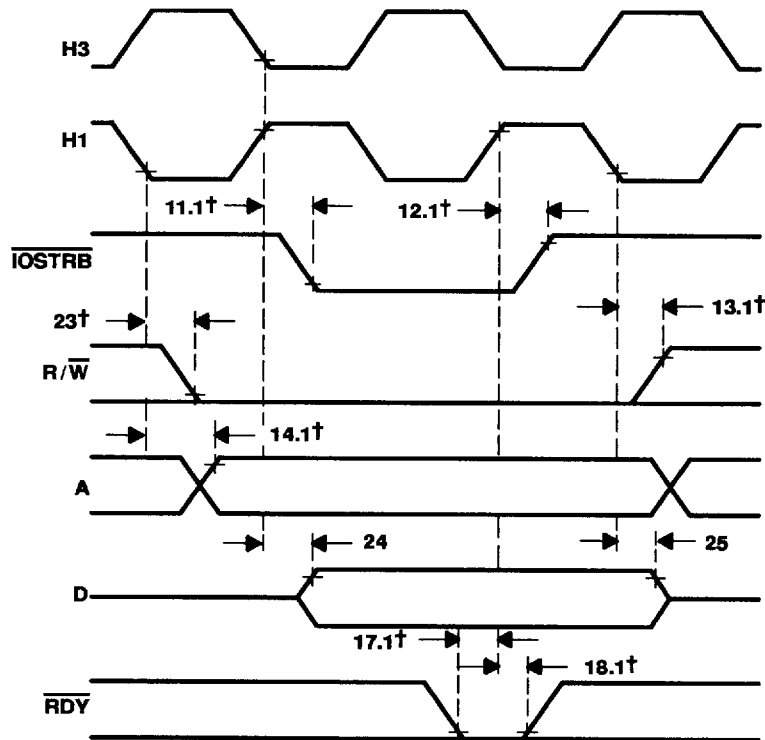
† See Figure 20 and accompanying table

Figure 21. Memory-Write-Cycle Timing Using $\overline{\text{IOSTRB}}$

timing for XF0 and XF1 when executing LDFI or LDII (see Figure 22)

NO.			'C32-40		'LC32-40		'C32-50		'C32-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
38	$t_{d(H3H-XF0L)}$	Delay time, H3 high to XF0 low		13		13		12		11	ns
39	$t_{su(XF1)}$	Setup time, XF1 before H1 low	9		10		9		8		ns
40	$t_{h(XF1)}$	Hold time, XF1 after H1 low	0		0		0		0		ns
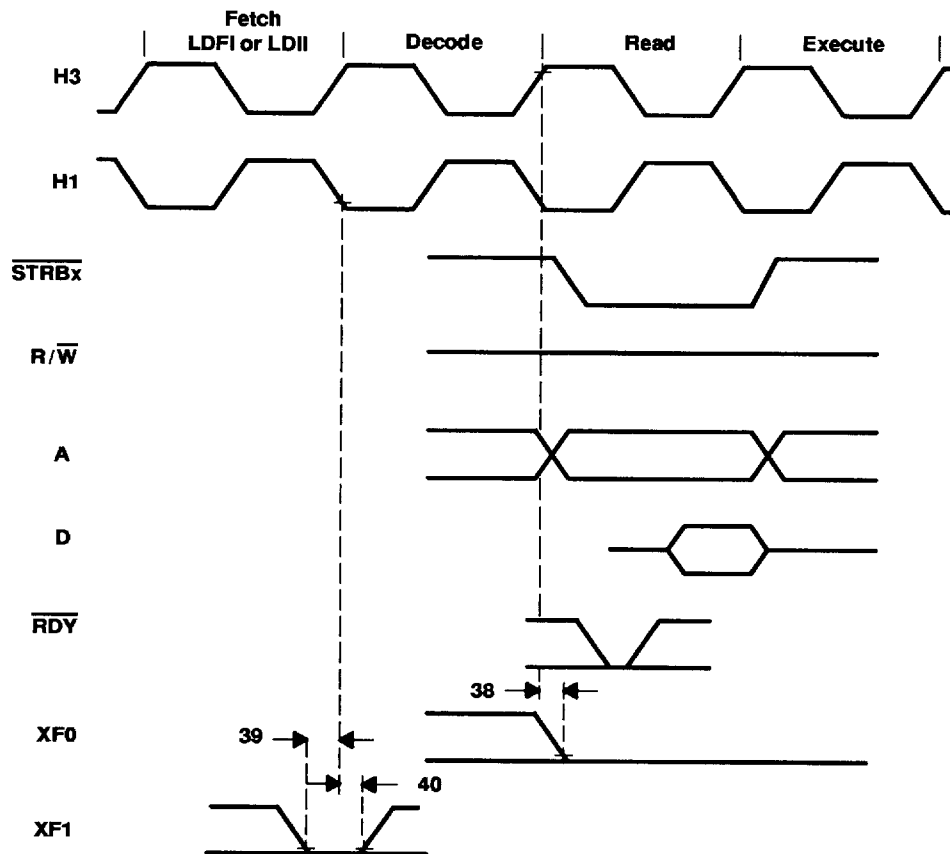
Figure 22. XF0 and XF1 When Executing LDFI or LDII

8961722 0097566 923

timing for XF0 when executing STFI or STII† (see Figure 23)

NO.		'C32-40 'LC32-40‡		'C32-50		'C32-60		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
41	$t_{d(H3H-XF0H)}$ Delay time, H3 high to XF0 high		13		12		11	ns

† XF0 is always set high at the beginning of the execute phase of the interlock-store instruction. When no pipeline conflicts occur, the address of the store is driven at the beginning of the execute phase of the interlock-store instruction. However, if a pipeline conflict prevents the store from executing, the address of the store is not driven until the store can execute.
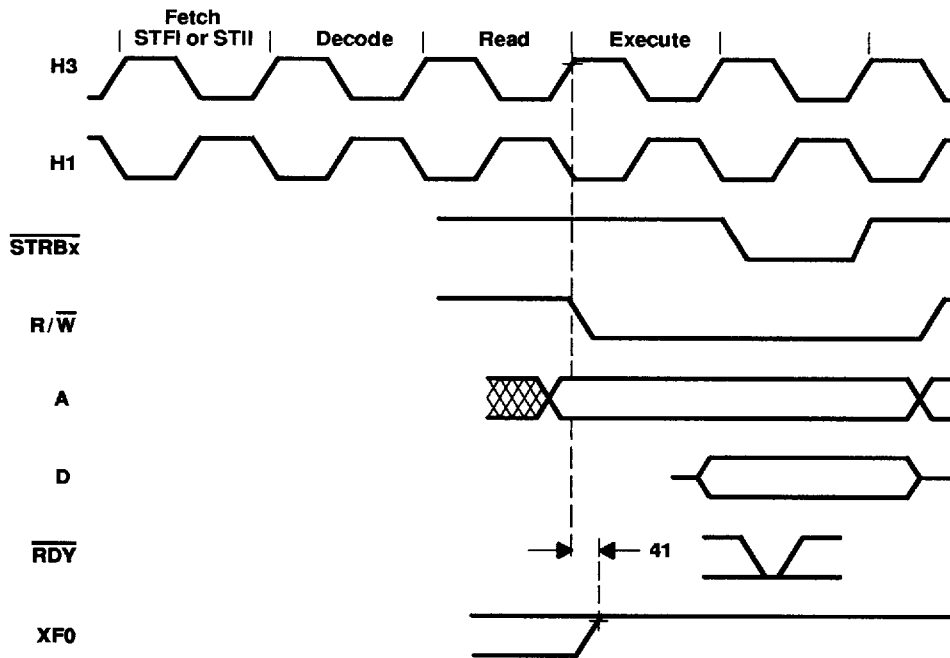
‡ 'LC32-40 data is preliminary

Figure 23. XF0 When Executing a STFI or STII

8961722 0097567 86T

timing for XF0 and XF1 when executing SIGI (see Figure 24)

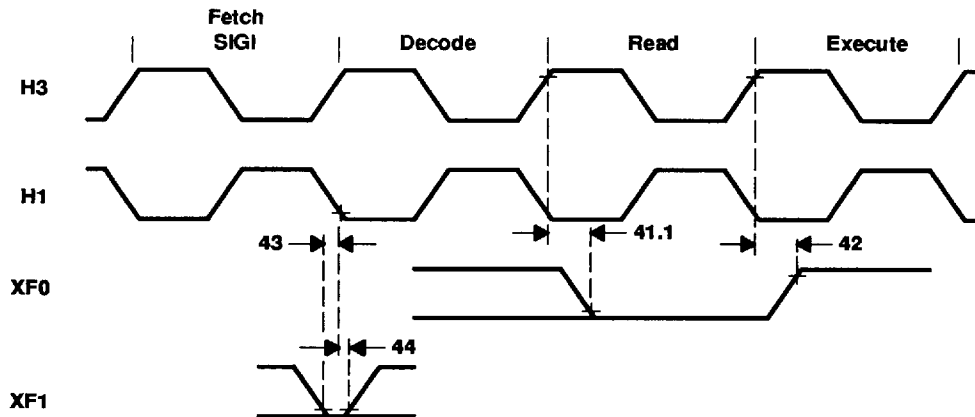| NO.			'C32-40		'LC32-40		'C32-50		'C32-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
41.1	$t_{d(H3H-XF0L)}$	Delay time, H3 high to XF0 low		13		13		12		11	ns
42	$t_{d(H3H-XF0H)}$	Delay time, H3 high to XF0 high		13		13		12		11	ns
43	$t_{su(XF1)}$	Setup time, XF1 before H1 low	9		10		9		8		ns
44	$t_{h(XF1)}$	Hold time, XF1 after H1 low	0		0		0		0		ns

Figure 24. XF0 and XF1 When Executing SIGI

timing for loading XF register when configured as an output pin (see Figure 25)

NO.			'C32-40		'C32-50		'C32-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
45	$t_{v(H3H-XF)}$	Valid time, H3 high to XF valid		13		12		11	ns
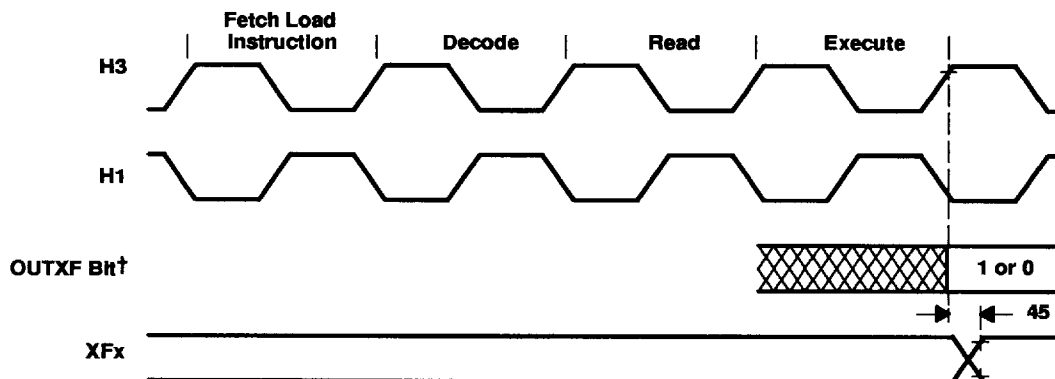
† OUTXFx represents either bit 2 or 6 of the IOF register.

Figure 25. Loading XF Register When Configured as an Output Pin

![Texas Instruments logo] **TEXAS INSTRUMENTS**

POST OFFICE BOX 1443 ● HOUSTON, TEXAS 77251–1443

29

: ■ 8961722 0097568 7T6 ■

timing of XF changing from output to input mode (see Figure 26)

NO.			'C32-40		'LC32-40		'C32-50		'C32-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
46	$t_{h(H3H-XF01)}$	Hold time, XF after H3 high		13†		13†		12†		11†	ns
47	$t_{su(XF)}$	Setup time, XF before H1 low	9		10		9		8		ns
48	$t_{h(XF)}$	Hold time, XF after H1 low	0		0		0		0		ns

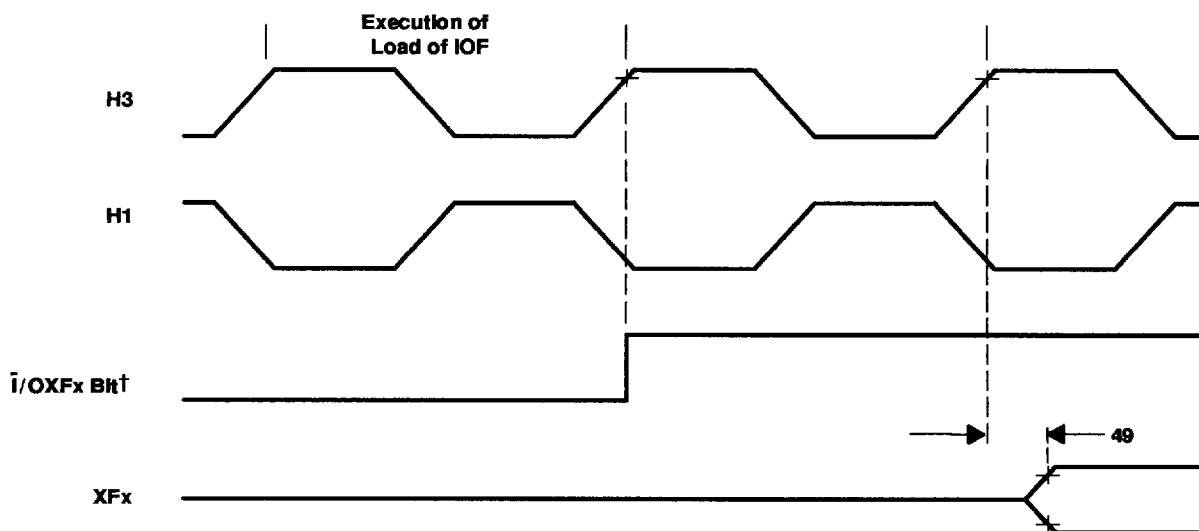† Assured from characterization but not tested
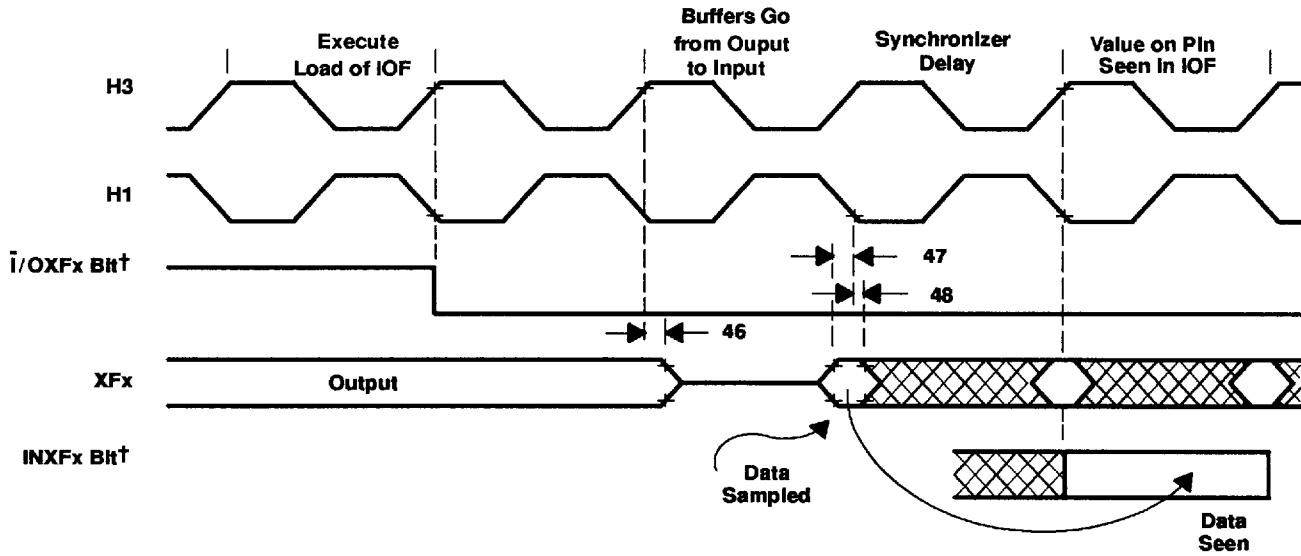
† I/OXFx represents either bit 1 or bit 5 of the IOF register, and INXFx represents either bit 3 or bit 7 of the IOF register.

Figure 26. Change of XF From Output to Input Mode

8961722 0097569 632

timing of XF changing from input to output mode (see Figure 27)

NO.			'C32-40 'LC32-40†		'C32-50		'C32-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
49	$t_{d(H3H-XFIO)}$	Delay time, H3 high to XF switching from input to output		17		17		15	ns

† 'LC32-40 data is preliminary

† Ī/OXFx represents either bit 1 or bit 5 of the IOF register.

Figure 27. Change of XF From Input to Output Mode

timing for $\overline{RESET}$ [Q = $t_{c(CI)}$] (see Figure 28)

NO.			'C32-40 'LC32-40[†]		'C32-50		'C32-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
50	$t_{su(RESET)}$	Setup time, $\overline{RESET}$ before CLKIN low	10	Q[‡]	10	Q[‡]	7	Q[‡]	ns
51	$t_{d(CLKINH-H1H)}$	Delay time, CLKIN high to H1 high	2	12	2	10	2	10	ns
52	$t_{d(CLKINH-H1L)}$	Delay time, CLKIN high to H1 low	2	12	2	10	2	10	ns
53	$t_{su(RESETH-H1L)}$	Setup time, $\overline{RESET}$ high before H1 low and after ten H1 clock cycles	9		7		6		ns
54	$t_{d(CLKINH-H3L)}$	Delay time, CLKIN high to H3 low	2	12	2	10	2	10	ns
55	$t_{d(CLKINH-H3H)}$	Delay time, CLKIN high to H3 high	2	12	2	10	2	10	ns
56	$t_{dis(H1H-D)}$	Disable time, H1 low to D in the high-impedance state		13[§]		12[§]		11[§]	ns
57	$t_{dis(H3HL-A)}$	Disable time, H3 low to A in the high-impedance state		9[§]		8[§]		7[§]	ns
58.1	$t_{d(H3H-CONTROLH)}$	Delay time, H3 high to control signals high		9[§]		8[§]		7[§]	ns
58.2	$t_{d(H1H-RWH)}$	Delay time, H1 low to R/$\overline{W}$ high		9[§]		8[§]		7[§]	ns
59	$t_{d(H1H-IACKH)}$	Delay time, H1 high to $\overline{IACK}$ high		9[§]		8[§]		7[§]	ns
60	$t_{dis(RESETL-ASYNCH)}$	Disable time, $\overline{RESET}$ low to asynchronous reset signals in the high-impedance state		21[§]		17[§]		14[§]	ns

[†] 'LD32-40 data is preliminary
[‡] Assured by design but not tested
[§] Assured from characterization but not tested.

8961722 0097571 290
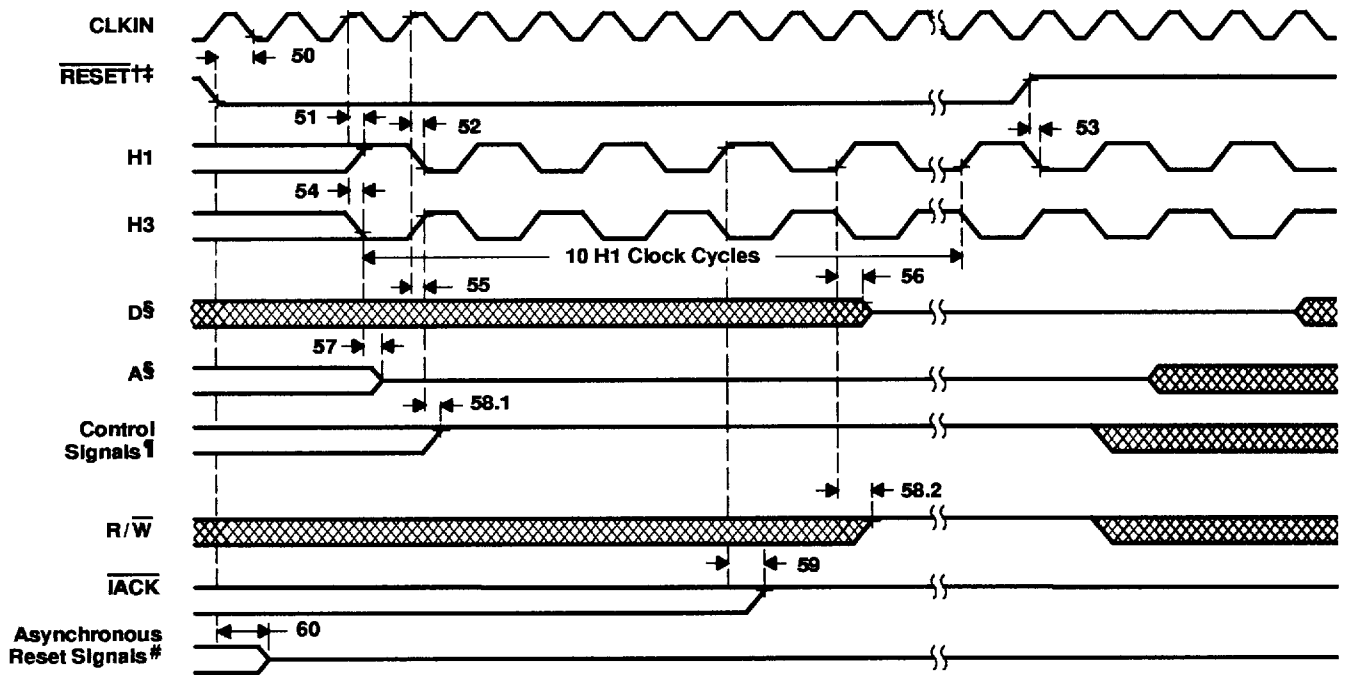
timing for $\overline{\text{RESET}}$ [Q = $t_{c(CI)}$] (continued)

Figure 28. $\overline{\text{RESET}}$ Timing

† $\overline{\text{RESET}}$ is an asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown occurs; otherwise, an additional delay of one clock cycle can occur.

‡ The R/$\overline{\text{W}}$ output is placed in the high-impedance state during reset and can be provided with a resistive pullup, nominally 18 – 22 kΩ, if undesirable spurious writes can occur when these outputs go low.

§ In microprocessor mode (MCBL/$\overline{\text{MP}}$ = 0), reset vector is fetched twice with seven software wait states each. In microcomputer mode (MCBL/$\overline{\text{MP}}$ = 1), the reset vector is fetched two times, with no software wait states.

¶ Control signals include $\overline{\text{STRBx}}$ and $\overline{\text{IOSTRB}}$.

Asynchronous reset signals include XF0/1, CLKX0, DX0, FSX0, CLKR0, DR0, FSR0, and TCLKx.

timing for $\overline{\text{INT3}}-\overline{\text{INT0}}$ interrupt response [P = $t_{c(H)}$] (see Figure 29)

NO.			'C32-40 'LC32-40†		'C32-50		'C32-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
61	$t_{su(INT)}$	Setup time, INT3–INT0 before H1 low	13		10		8		ns
62.1	$t_{w(INT)}$	Pulse duration of interrupt to assure only one interrupt seen for level-triggered interrupts	P	2P‡	P	2P‡	P	2P‡	ns
62.2	$t_{w(INT)}$	Pulse duration of interrupt for edge-triggered interrupts	P‡		P‡		P‡		ns

† 'LC32-40 data is preliminary
‡ Assured from characterization but not tested.
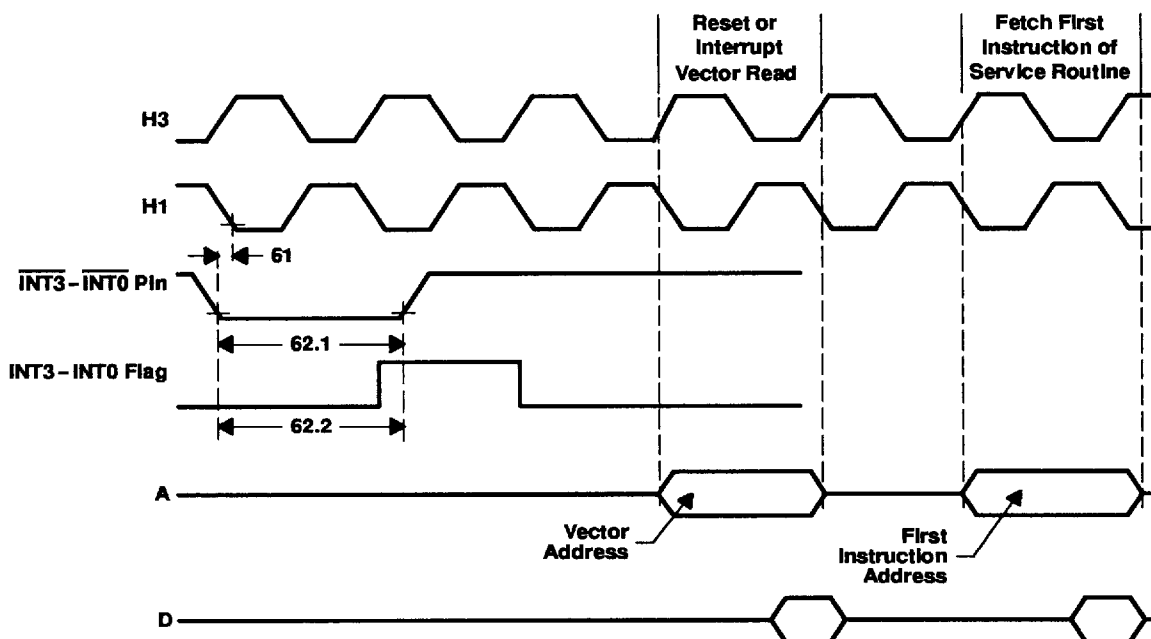
Figure 29. $\overline{\text{INT3}}$–$\overline{\text{INT0}}$ Interrupt-Response Timing

8961722 0097573 063

timing for $\overline{\text{IACK}}$ (see Notes 5, 6, and Figure 30)

NO.			'C32-40 'LC32-40†		'C32-50		'C32-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
63	$t_{d(H1H\text{-}IACKL)}$	Delay time, H1 high to $\overline{\text{IACK}}$ low		9		7		6	ns
64	$t_{d(H1H\text{-}IACKH)}$	Delay time, H1 high to $\overline{\text{IACK}}$ high		9		7		6	ns

† 'LC32-40 data is preliminary

NOTES: 5. $\overline{\text{IACK}}$ is active for the entire duration of the bus cycle and is extended if the bus cycle utilizes wait states.
6. $\overline{\text{IACK}}$ goes active on the first half-cycle (H1 rising) of the decode phase of the IACK instruction and goes inactive at the first half-cycle (H1 rising) of the read phase of the IACK instruction. Because of pipeline conflicts, $\overline{\text{IACK}}$ remains low for one cycle even if the decode phase of the IACK instruction is extended.
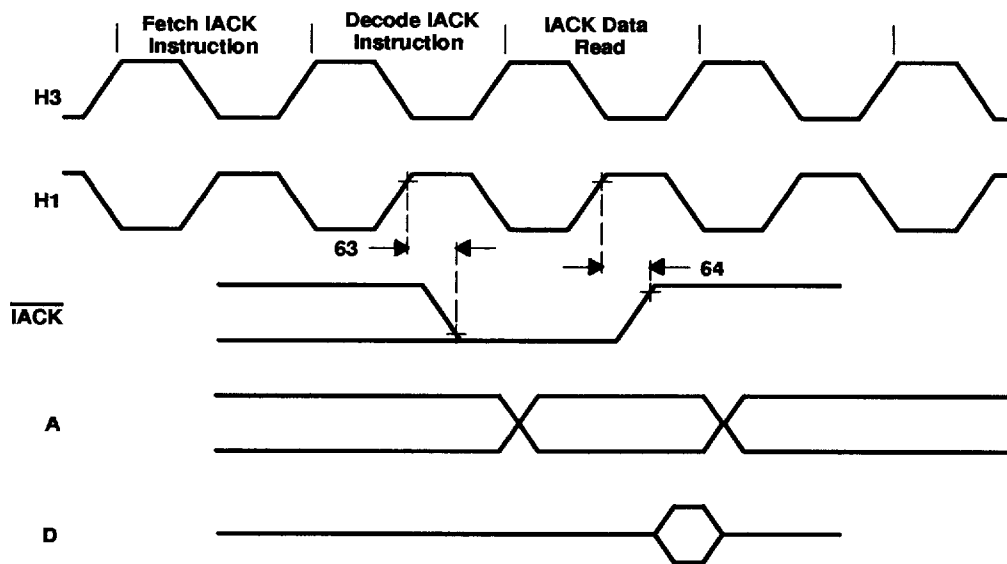

Figure 30. $\overline{\text{IACK}}$ Timing

8961722 0097574 TTT

serial-port timing [P = $t_{c(H)}$] (see Figure 31 and Figure 32)

| NO.				'C32-40 'LC32-40† MIN	MAX	'C32-50 MIN	MAX	'C32-60 MIN	MAX	UNIT
65	$t_{d(H1-SCK)}$	Delay time, H1 high to internal CLKX/R high/low			13		10		8	ns
66	$t_{c(SCK)}$	Cycle time, CLKX/R	CLKX/R ext	2.6P		2.6P		2.6P		ns
			CLKX/R int	2P	$(2^{32})P$	2P	$(2^{32})P$	2P	$(2^{32})P$	
67	$t_{w(SCK)}$	Pulse duration, CLKX/R high/low	CLKX/R ext	P + 10		P + 10		P + 10		ns
			CLKX/R int	$[t_{c(SCK)}/2] - 5$	$[t_{c(SCK)}/2] + 5$	$[t_{c(SCK)}/2] - 5$	$[t_{c(SCK)}/2] + 5$	$[t_{c(SCK)}/2] - 5$	$[t_{c(SCK)}/2] + 5$	
68	$t_{r(SCK)}$	Rise time, CLKX/R			7		6		5	ns
69	$t_{f(SCK)}$	Fall time, CLKX/R			7		6		5	ns
70	$t_{d(DX)}$	Delay time, CLKX to DX valid	CLKX ext		30		24		20	ns
			CLKX int		17		16		15	
71	$t_{su(DR)}$	Setup time, DR before CLKR low	CLKR ext	9		9		8		ns
			CLKR int	21		17		15		
72	$t_{h(DR)}$	Hold time, DR from CLKR low	CLKR ext	9		7		6		ns
			CLKR int	0		0		0		
73	$t_{d(FSX)}$	Delay time, CLKX to internal FSX high/low	CLKX ext		27		22		20	ns
			CLKX int		15		15		14	
74	$t_{su(FSR)}$	Setup time, FSR before CLKR low	CLKR ext	9		7		6		ns
			CLKR int	9		7		6		
75	$t_{h(FS)}$	Hold time, FSX/R input from CLKX/R low	CLKX/R ext	9		7		6		ns
			CLKX/R int	0		0		0		
76	$t_{su(FSX)}$	Setup time, external FSX before CLKX high	CLKX ext	8 – P‡	$[t_{c(SCK)}/2]-10‡$	8 – P‡	$[t_{c(SCK)}/2]-10‡$	8 – P‡	$[t_{c(SCK)}/2]-10‡$	ns
			CLKX int	21 – P‡	$t_{c(SCK)}/2‡$	21 – P‡	$t_{c(SCK)}/2‡$	21 – P‡	$t_{c(SCK)}/2‡$	
77	$t_{d(CH-DX)V}$	Delay time, CLKX to first DX bit, FSX precedes CLKX high	CLKX ext		30‡		24‡		20‡	ns
			CLKX int		18‡		14‡		12‡	
78	$t_{d(FSX-DX)V}$	Delay time, FSX to first DX bit, CLKX precedes FSX			30‡		24‡		20‡	ns
79	$t_{d(DXZ)}$	Delay time, CLKX high to DX in the high-impedance state following last data bit			17‡		14‡		12‡	ns

† LC32-40 data is preliminary
‡ Assured from characterization but not tested

8961722 0097575 936

serial-port timing [P = t_{C(H)}] (see Figure 31 and Figure 32) (Continued)
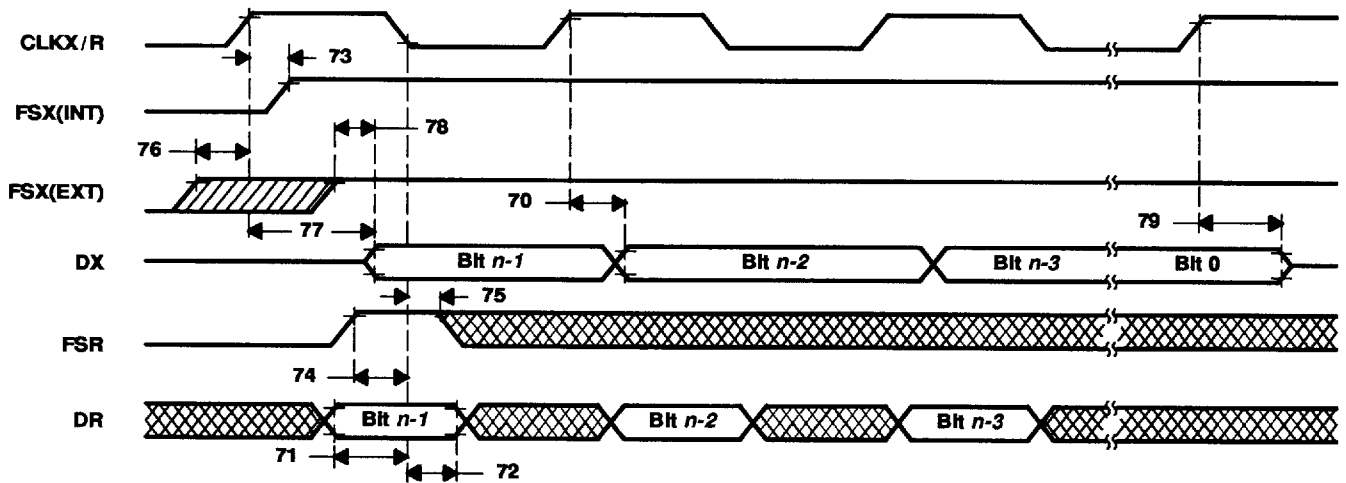
serial-port timing [P = $t_{C(H)}$] (see Figure 31 and Figure 32) (Continued)
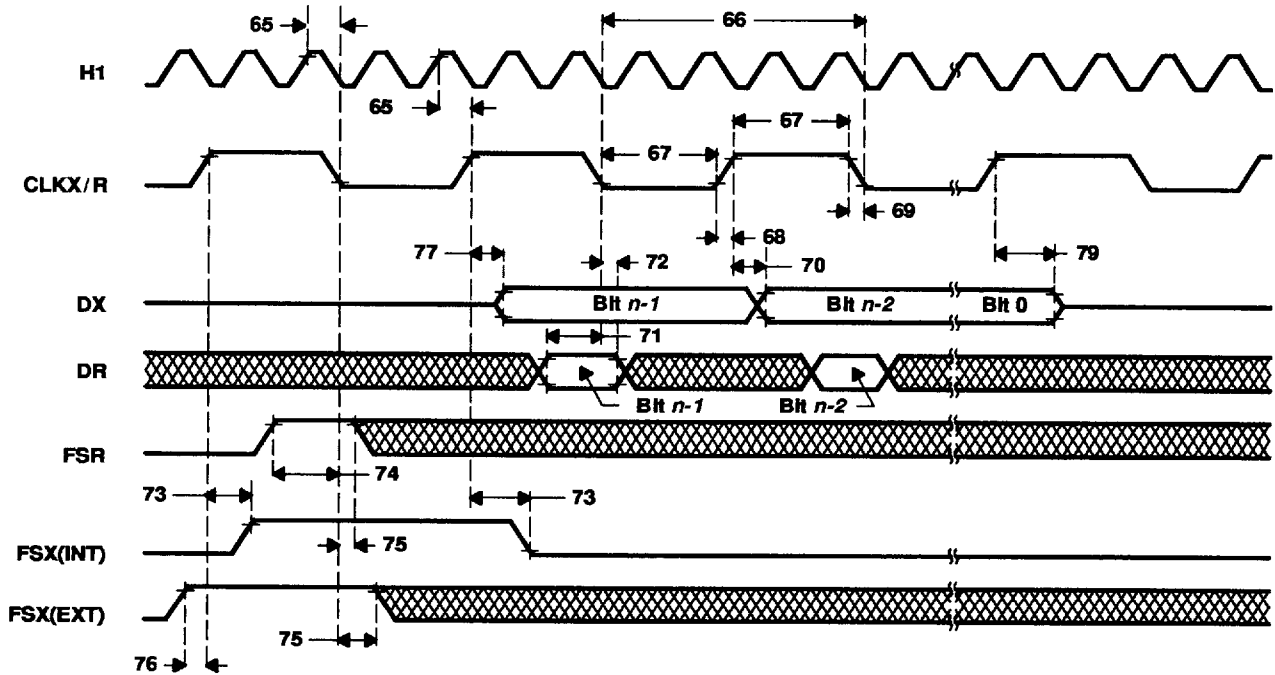
NOTES: A. Timing diagrams show operations with CLKXP = CLKRP = FSXP = FSRP = 0.
B. Timing diagrams depend upon the length of the serial-port word, where n = 8, 16, 24, or 32 bits, respectively.

Figure 31. Fixed Data-Rate-Mode Timing

NOTES: A. Timing diagrams show operation with CLKXP = CLKRP = FSXP = FSRP = 0.
B. Timing diagrams depend upon the length of the serial-port word, where n = 8, 16, 24, or 32 bits, respectively.
C. The timings that are not specified expressly for the variable data-rate mode are the same as those that are specified for the fixed data-rate mode.

Figure 32. Variable Data-Rate-Mode Timing

8961722 0097576 872

timing for $\overline{\text{HOLD}}/\overline{\text{HOLDA}}$ [P = $t_{c(H)}$] (see Note 7 and Figure 33)

NO.			'C32-40 'LC32-40†		'C32-50		'C32-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
80	$t_{su(HOLD)}$	Setup time, HOLD before H1 low	13		10		8		ns
81	$t_{v(HOLDA)}$	Valid time, HOLDA after H1 low	0‡	9	0‡	7	0‡	6	ns
82	$t_{w(HOLD)}$	Pulse duration, HOLD low	2P		2P		2P		ns
83	$t_{w(HOLDA)}$	Pulse duration, HOLDA low	P–5‡		P–5‡		P–5‡		ns
84	$t_{d(H1L-SH)H}$	Delay time, H1 low to STRBx high for a HOLD	0§	9	0§	7	0§	6	ns
84.1	$t_{d(H1H-IOS)H}$	Delay time, H1 high to IOSTRB high for a HOLD	0§	9	0§	7	0§	6	ns
85	$t_{dis(H1L-S)}$	Disable time, H1 low to STRBx or IOSTRB (in the high-impedance state)	0§	9‡	0§	8‡	0§	7‡	ns
86	$t_{en(H1L-S)}$	Enable time, H1 low to STRBx or IOSTRB active	0§	9	0§	7	0§	6	ns
87	$t_{dis(H1L-RW)}$	Disable time, H1 low to R/W in the high-impedance state	0‡	9‡	0‡	8‡	0‡	7‡	ns
88	$t_{en(H1L-RW)}$	Enable time, H1 low to R/W (active)	0‡	9	0‡	7	0‡	6	ns
89	$t_{dis(H1L-A)}$	Disable time, H1 low to A in the high-impedance state	0§	10‡	0§	8‡	0§	7‡	ns
90	$t_{en(H1L-A)}$	Enable time, H1 low to A valid	0§	13	0§	12	0§	11	ns
91	$t_{dis(H1H-D)}$	Disable time, H1 high to D disabled in the high-impedance state	0§	9‡	0§	8‡	0§	7‡	ns

† 'LC32-40 data is preliminary
‡ Assured from characterization but not tested
§ Not tested
NOTE 7: $\overline{\text{HOLD}}$ is an asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown occurs; otherwise, an additional delay of one clock cycle can occur. The NOHOLD bit of the primary-bit-control register overwrites the $\overline{\text{HOLD}}$ signal.

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 ● HOUSTON, TEXAS 77251–1443

8961722 0097577 709

timing for $\overline{\text{HOLD}}/\overline{\text{HOLDA}}$ [P = $t_{c(H)}$] (see Note 7 and Figure 33) (Continued)
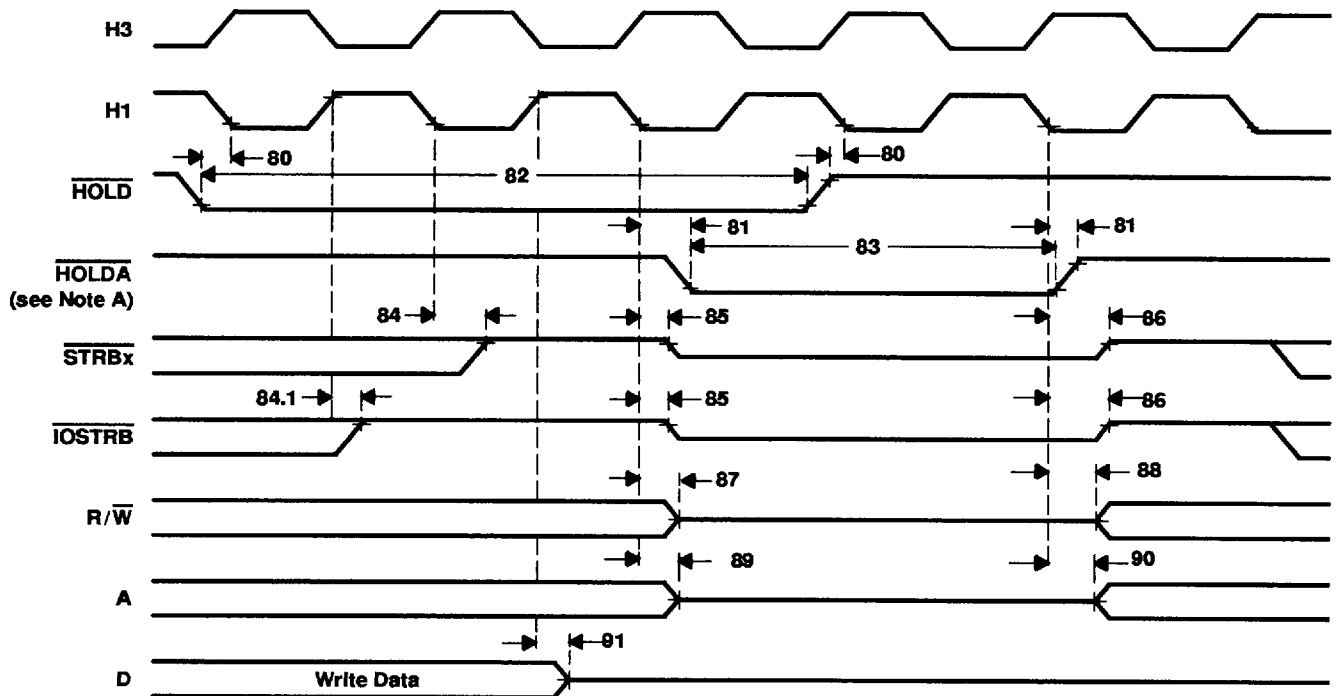
NOTE A: $\overline{\text{HOLDA}}$ goes low in response to $\overline{\text{HOLD}}$ going low and continues to remain low until one H1 cycle after $\overline{\text{HOLD}}$ goes back high.

Figure 33. $\overline{\text{HOLD}}/\overline{\text{HOLDA}}$ Timing

8961722 0097578 645

timing of peripheral pin configured as general-purpose I/O (see Figure 34)

| NO.			'C32-40 'LC32-40†		'C32-50		'C32-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
92	$t_{su(GPIOH1L)}$	Setup time, general-purpose input before H1 low	10		9		8		ns
93	$t_{h(GPIOH1L)}$	Hold time, general-purpose input after H1 low	0		0		0		ns
94	$t_{d(GPIOH1H)}$	Delay time, general-purpose output after H1 high		13		10		8	ns

† 'LC32-40 data is preliminary
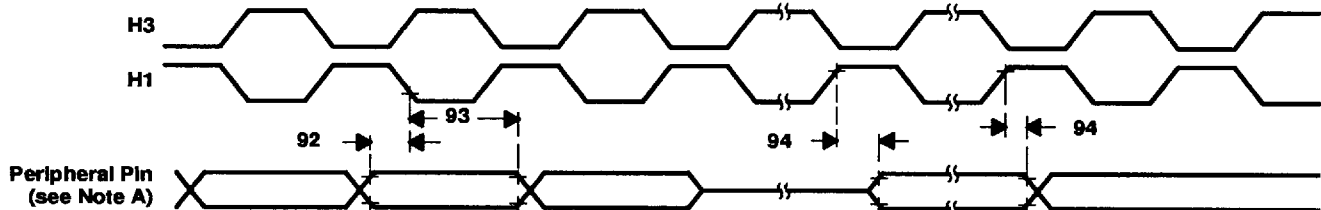
NOTE A: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLKx. The modes of these pins are defined by the contents of internal control registers associated with each peripheral.

Figure 34. Peripheral-Pin General-Purpose I/O Timing

timing of peripheral pin changing from general-purpose output to input mode (see Figure 35)

NO.			'C32-40 'LC32-40†		'C32-50		'C32-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
95	$t_{h(H1H)}$	Hold time, after H1 high		13		12		11	ns
96	$t_{su(GPIOH1L)}$	Setup time, peripheral pin before H1 low	10		9		8		ns
97	$t_{h(GPIOH1L)}$	Hold time, peripheral pin after H1 low	0		0		0		ns
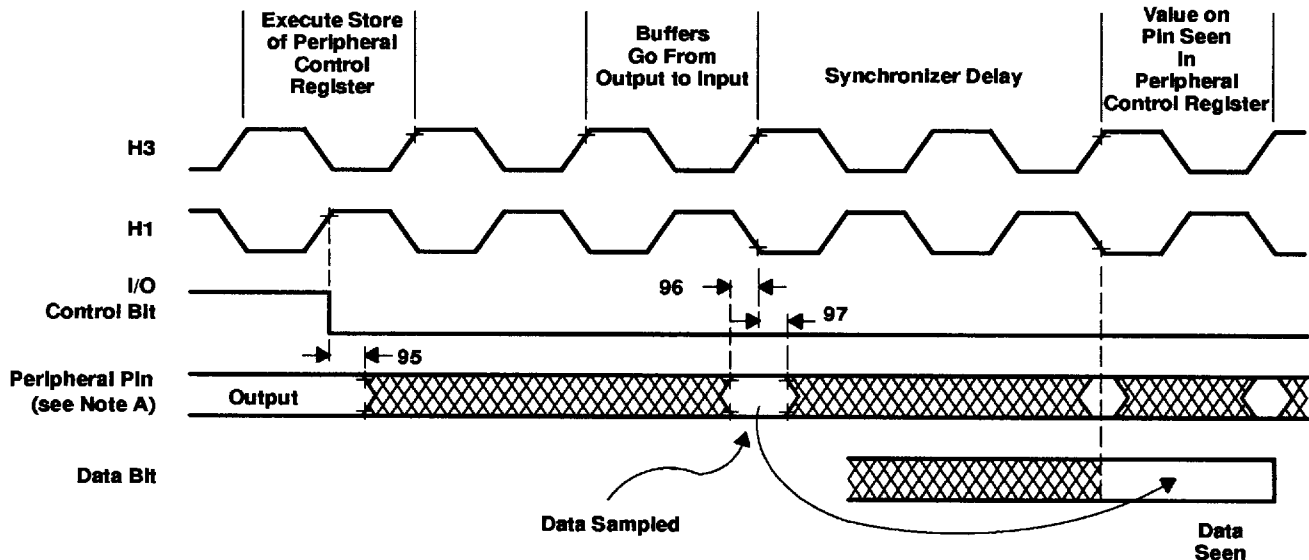
† 'LC32-40 data is preliminary

NOTE A: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLKx. The modes of these pins are defined by the contents of internal control registers associated with each peripheral.

Figure 35. Timing of Peripheral Pin Changing From General-Purpose Output to Input-Mode
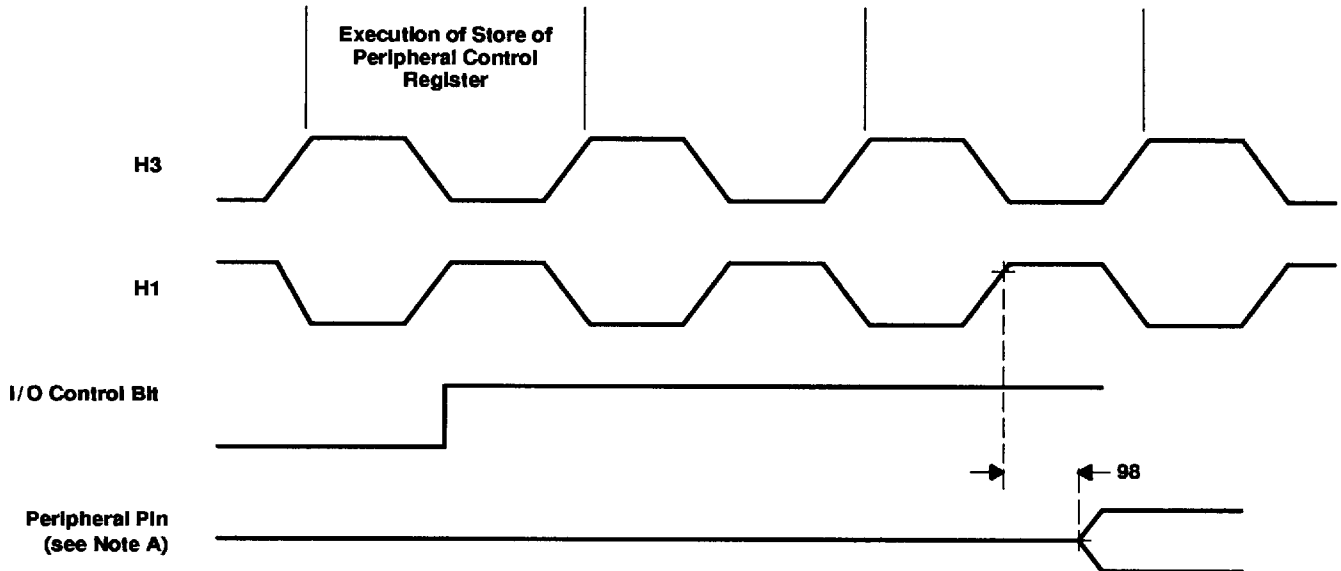
: ■ 8961722 0097579 581 ■

timing of peripheral pin changing from general-purpose input to output mode (see Figure 36)

NO.			'C32-40 'LC32-40†		'C32-50		'C32-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
98	$t_{d(GPIOH1H)}$	Delay time, H1 high to peripheral pin switching from input to output		13		10		8	ns

† 'LC32-40 data is preliminary

NOTE A: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLKx. The modes of these pins are defined by the contents of internal control registers associated with each peripheral.

Figure 36. Timing of Peripheral Pin Changing From General-Purpose Input to Output-Mode

8961722 0097580 2T3

timing for timer pin [P = $t_{c(H)}$] (see Figure 37)[†]

NO.				'C32-40 'LC32-40[‡]		UNIT
				MIN	MAX	
99	$t_{su(TCLKH1L)}$	Setup time, TCLK external before H1 low		10		ns
100	$t_{h(TCLKH1L)}$	Hold time, TCLK external after H1 low		0		ns
101	$t_{d(TCLKH1H)}$	Delay time, H1 high to TCLK internal valid			9	ns
102	$t_{c(TCLK)}$	Cycle time, TCLK	TCLK external	2.6P		ns
			TCLK internal	2P	(2^{32})P§	
103	$t_{w(TCLK)}$	Pulse duration, TCLK high / low	TCLK external	P + 10		ns
			TCLK internal	$[t_{c(TCLK)}/2]-5$	$[t_{c(TCLK)}/2]+5$	

[†] Timing parameters 99 and 100 are applicable for a synchronous input clock. Timing parameters 102 and 103 are applicable for an asynchronous input clock.
[‡] 'LC32-40 data is preliminary
§ Assured by design but not tested

NO.				'C32-50		UNIT
				MIN	MAX	
99	$t_{su(TCLKH1L)}$	Setup time, TCLK external before H1 low		8		ns
100	$t_{h(TCLKH1L)}$	Hold time, TCLK external after H1 low		0		ns
101	$t_{d(TCLKH1H)}$	Delay time, H1 high to TCLK internal valid			9	ns
102	$t_{c(TCLK)}$	Cycle time, TCLK cycle time	TCLK external	2.6P		ns
			TCLK internal	2P	(2^{32})P‡	
103	$t_{w(TCLK)}$	Pulse duration, TCLK high / low	TCLK external	P + 10		ns
			TCLK internal	$[t_{c(TCLK)}/2]-5$	$[t_{c(TCLK)}/2]+5$	

[†] Timing parameters 99 and 100 are applicable for a synchronous input clock. Timing parameters 102 and 103 are applicable for an asynchronous input clock.
[‡] Assured by design but not tested

NO.				'C32-60		UNIT
				MIN	MAX	
99	$t_{su(TCLKH1L)}$	Setup time, TCLK external before H1 low		6		ns
100	$t_{h(TCLKH1L)}$	Hold time, TCLK external after H1 low		0		ns
101	$t_{d(TCLKH1H)}$	Delay time, H1 high to TCLK internal valid			8	ns
102	$t_{c(TCLK)}$	Cycle time, TCLK cycle time	TCLK external	2.6P		ns
			TCLK internal	2P	(2^{32})P‡	
103	$t_{w(TCLK)}$	Pulse duration, TCLK high / low	TCLK external	P + 10		ns
			TCLK internal	$[t_{c(TCLK)}/2]-5$	$[t_{c(TCLK)}/2]+5$	

[†] Timing parameters 99 and 100 are applicable for a synchronous input clock. Timing parameters 102 and 103 are applicable for an asynchronous input clock.
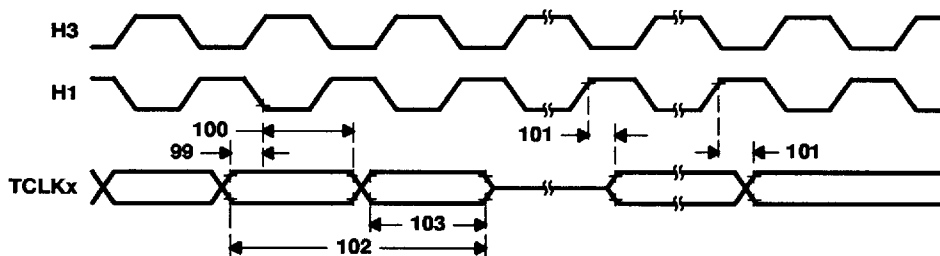[‡] Assured by design but not tested

Figure 37. Timing for Timer Pin

8961722 0097581 13T

timing for $\overline{SHZ}$ pin [Q = $t_{c(CI)}$] (see Figure 38)

NO.			'LC32-40 'C32-50†		'C32-60		UNIT
			MIN	MAX	MIN	MAX	
104	$t_{dis(SHZ)}$	Disable time, $\overline{SHZ}$ low to all O, I/O pins in the high-impedance state	0‡	2Q‡	0‡	2Q‡	ns

† 'LC32-40 data is preliminary
‡ Assured by characterization but not tested
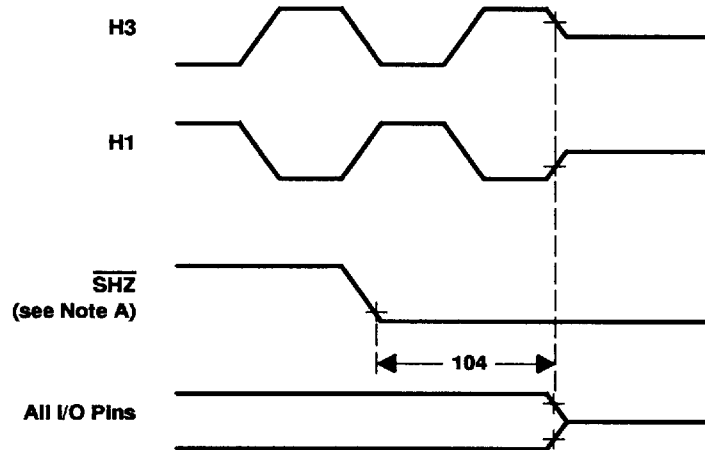
NOTE A: Enabling $\overline{SHZ}$ destroys 'C32 register and memory contents. Assert $\overline{SHZ}$ = 1 and reset the 'C32 to restore it to a known condition.

Figure 38. $\overline{SHZ}$ Pin Timing

Table 1. Thermal Resistance Characteristics for PCM package

PARAMETER		MIN	MAX	UNIT
$R_{\Theta JA}$	Junction-to-free-air		39	°C/W
$R_{\Theta JC}$	Junction-to-case		10.0	°C/W

Table 2. Thermal Resistance Characteristics for PCE package

PARAMETER		MIN	MAX	UNIT
$R_{\Theta JA}$	Junction-to-free-air		47.5	°C/W
$R_{\Theta JC}$	Junction-to-case		10.0	°C/W

8961722 0097582 076

TMS320C32, TMS320LC32, TMX320C32
DIGITAL SIGNAL PROCESSOR

MECHANICAL DATA

PCM(S-PQFP-G*)**   **PLASTIC QUAD FLATPACK**

144 PIN SHOWN
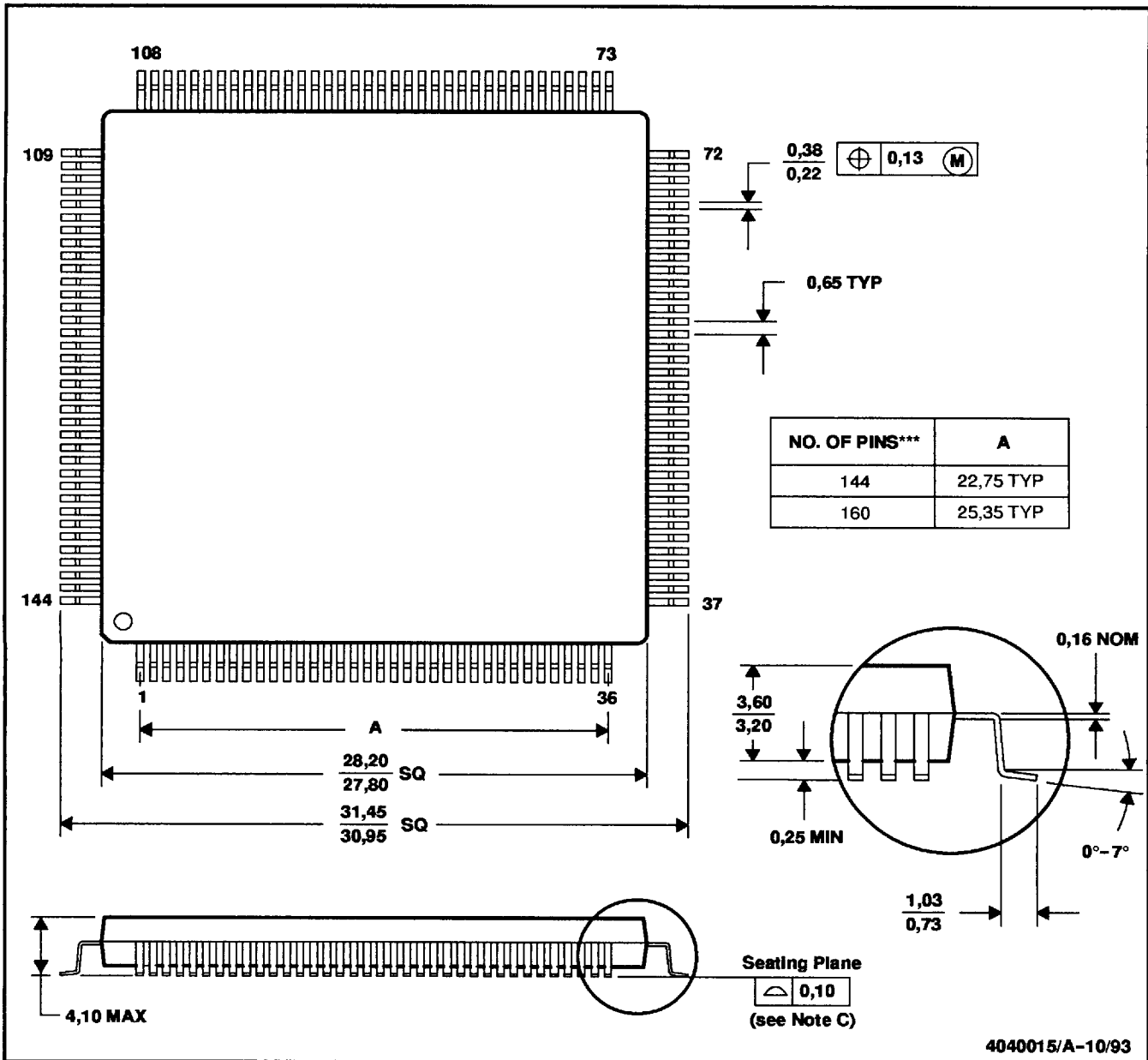
NO. OF PINS***	A
144	22,75 TYP
160	25,35 TYP

4040015/A–10/93

NOTES: A. All linear dimensions are in millimeters.
   B. This drawing is subject to change without notice.
   C. Falls within JEDEC MS-022
   D. The 144PCM is identical to 160PCM except that 4 leads per corner are removed.
   E. Foot length is measured from lead tip to a position on backside of lead 0,25 mm above seating plane (gage plane)
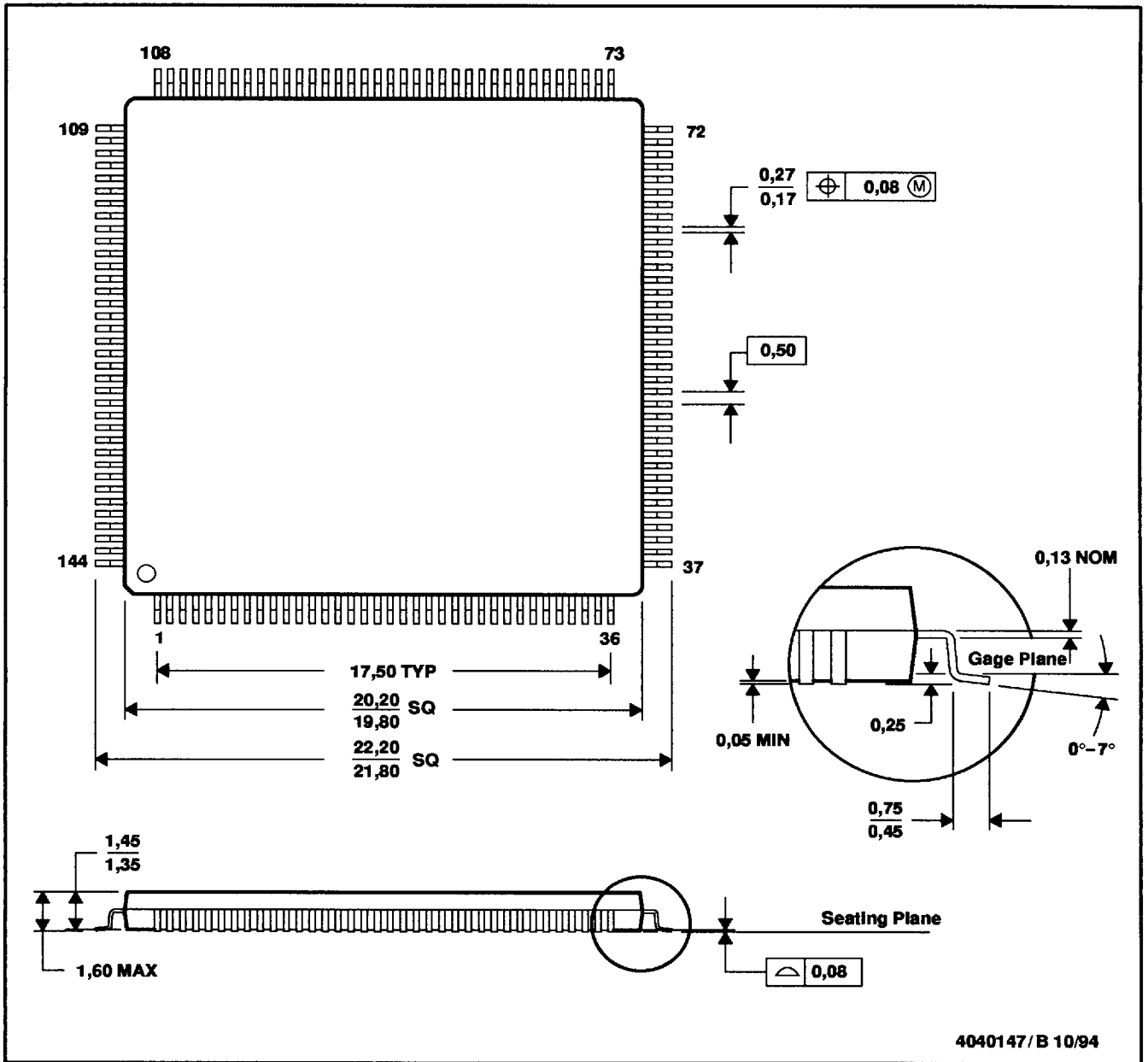   F. Preliminary drawing

![Texas Instruments logo] **TEXAS INSTRUMENTS**

POST OFFICE BOX 1443 ● HOUSTON, TEXAS 77251-1443

8961722 0097583 T02

MECHANICAL DATA

PGE (S-PQFP-G144)   **PLASTIC QUAD FLATPACK**

4040147 / B 10/94

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Falls within JEDEC MO-136

45

8961722 0097584 949