

T-46-13-25



Am27X512

65,536 x 8-Bit CMOS ExpressROM™ Device

Advanced
Micro
Devices

DISTINCTIVE CHARACTERISTICS

- **As an OTP EPROM alternative:**
 - Factory optimized programming
 - Fully tested and guaranteed
 - Lower cost
- **As a Mask ROM alternative:**
 - Shorter leadtime
 - Lower volume per code
- **Compatible with JEDEC-approved EPROM pinout**
- **High noise immunity**
- **High performance CMOS technology**
 - Fast access time — 120 ns
 - Low power dissipation
100 μ A maximum standby current
- **Available in plastic DIP and plastic leaded chip carrier (PLCC), and in DIE form**
- **Latch-up protected to 100 mA from -1 V to $V_{cc} + 1$ V**

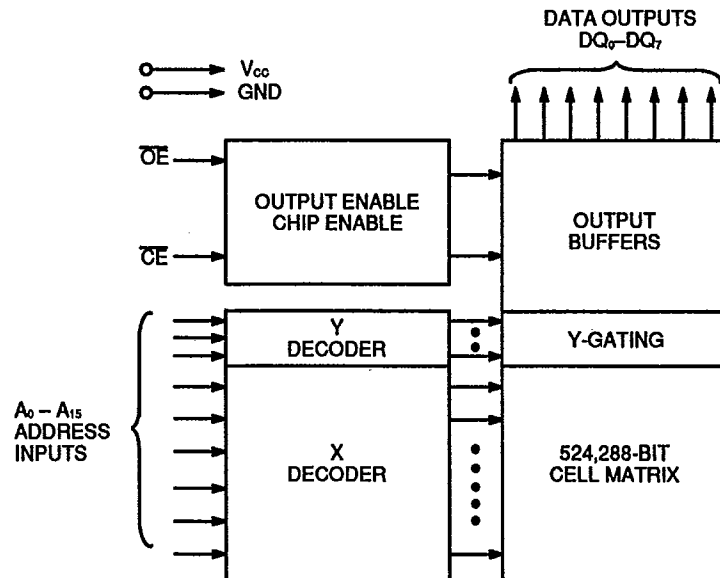
GENERAL DESCRIPTION

The Am27X512 is a wafer-level programmed EPROM with a standard topside for plastic packaging. It is organized as 65,536 by 8 bits and is available in plastic DIP as well as plastic leaded chip carrier (PLCC) packages. ExpressROM Devices provide a board-ready memory solution for medium to high volume codes with short leadtimes. This offers manufacturers a cost-effective and flexible alternative to OTP EPROMs and mask programmed ROMs.

Access times as fast as 120 ns allow operation with high-performance microprocessors with reduced WAIT states. The Am27X512 offers separate Output Enable (\overline{OE}) and Chip Enable (\overline{CE}) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 250 μ W in standby mode.

BLOCK DIAGRAM



12081B-001

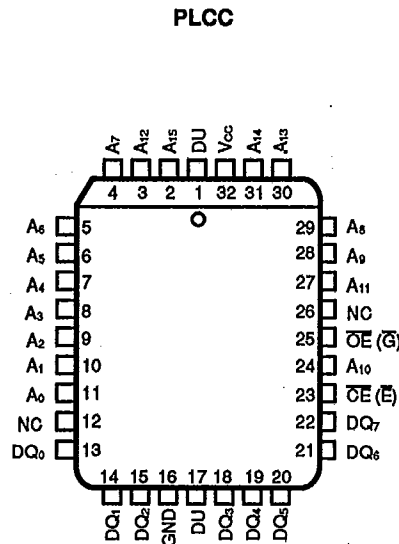
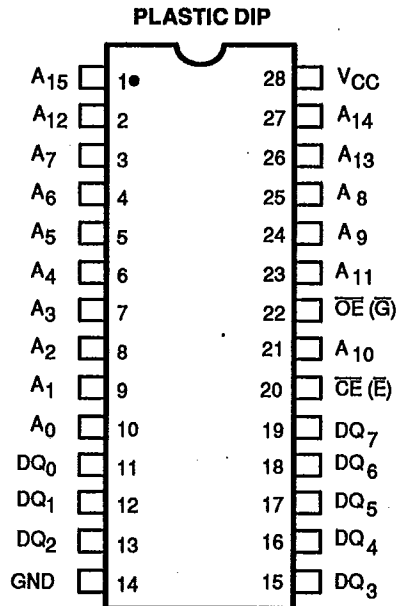
PRODUCT SELECTOR GUIDE

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Family Part No.	Am27X512			
Ordering part No: ±5% VCC Tolerance ±10% VCC Tolerance	-125	-155		
	—	-150	-200	-250
Max Access Time (ns)	120	150	200	250
\overline{CE} (\overline{E}) Access (ns)	120	150	200	250
\overline{OE} (\overline{G}) Access (ns)	50	50	75	100

CONNECTION DIAGRAMS

Top View

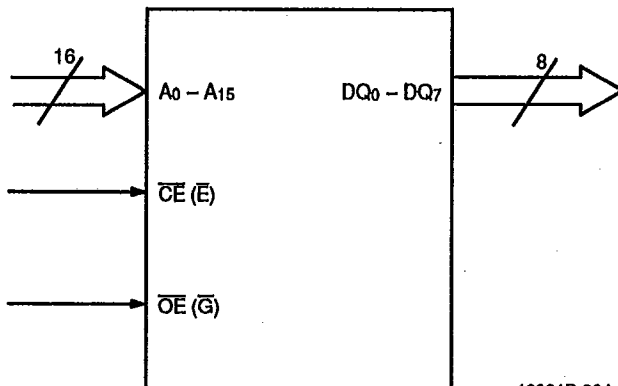


12081B-002

11557-003A

Note: JEDEC nomenclature is in parentheses.

LOGIC SYMBOL



12081B-004

PIN DESCRIPTION

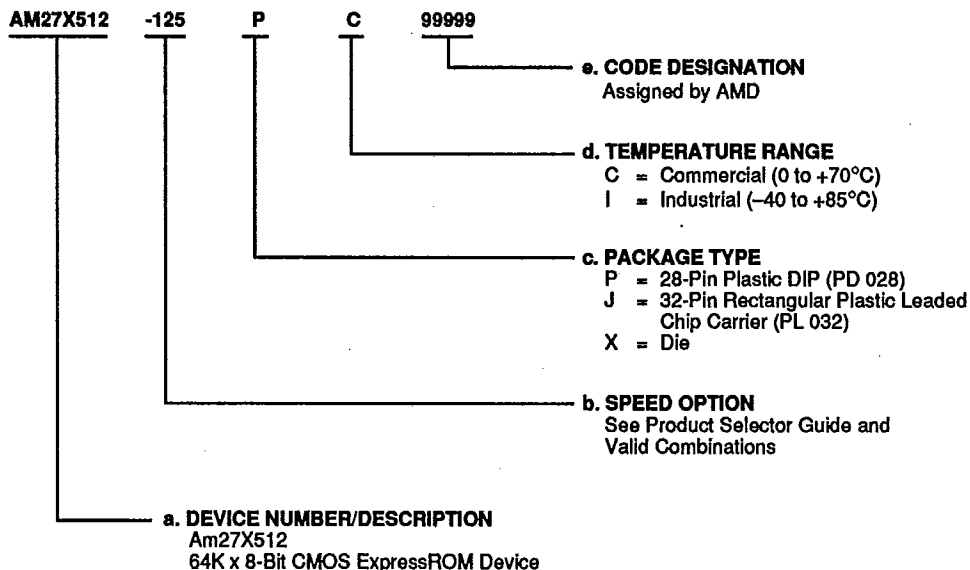
- A₀ - A₁₅ = Address Inputs
- \overline{CE} (\overline{E}) = Chip Enable Input
- DQ₀ - DQ₇ = Data Outputs
- \overline{OE} (\overline{G}) = Output Enable Input
- V_{cc} = V_{cc} Supply Voltage
- GND = Ground
- NC = No Internal Connection
- DU = No External Connection (Do Not Use)

ORDERING INFORMATION
Standard Products

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AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option
- c. Package Type
- d. Temperature Range
- e. Code Designation



Valid Combinations	
AM27X512-125	PC, JC, XC, PI, JI
AM27X512-150	
AM27X512-155	
AM27X512-200	
AM27X512-250	

Valid Combinations
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

Read Mode

The Am27X512 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable (\overline{CE}) is the power control and should be used for device selection. Output Enable (\overline{OE}) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{acc}) is equal to the delay from \overline{CE} to output (t_{ce}). Data is available at the outputs t_{oe} after the falling edge of \overline{OE} , assuming that \overline{CE} has been LOW and addresses have been stable for at least $t_{acc} - t_{oe}$.

Standby Mode

The Am27X512 has a CMOS standby mode which reduces the maximum V_{cc} current to 100 μA . It is placed in CMOS-standby when \overline{CE} is at $V_{cc} \pm 0.3 V$. The Am27X512 also has a TTL-standby mode which reduces the maximum V_{cc} current to 1.0 mA. It is placed in TTL-standby when \overline{CE} is at V_{IH} . When in standby mode, the outputs are in a high-impedance state, independent of the \overline{OE} input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that \overline{CE} be decoded and used as the primary device-selecting function, while \overline{OE} be made a common connection to all devices in the array and connected to the READ line from the system control bus.

This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 μF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{cc} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on ExpressROM Device arrays, a 4.7 μF bulk electrolytic capacitor should be used between V_{cc} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

Mode Select Table			
Mode \ Pins	\overline{CE}	\overline{OE}	Outputs
Read	V_{IL}	V_{IL}	DOUR
Output Disable	V_{IL}	V_{IH}	High Z
Standby (TTL)	V_{IH}	X	High Z
Standby (CMOS)	$V_{cc} \pm 0.3 V$	X	High Z

Note: X can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65 to +125°C
Ambient Temperature with Power Applied	-55 to +125°C
Voltage with Respect to Ground:	
All pins except Vcc	-0.6 to Vcc+0.6 V
Vcc	-0.6 to +7.0 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Note:

During transitions, the input may overshoot GND to -2.0 V for periods of up to 20 ns. Maximum DC voltage on input and output may overshoot to Vcc +2.0 V for periods of up to 20 ns.

OPERATING RANGES

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Commercial (C) Devices

Case Temperature (Tc) 0 to +70°C

Industrial (I) Devices

Case Temperature (Tc) -40 to +85°C

Supply Read Voltages:

Vcc for Am27X512-XX5 +4.75 to +5.25 V

Vcc for Am27X512-XX0 +4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified
(Notes 3, 4 & 6)

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Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
TTL and NMOS					
V _{OH}	Output HIGH Voltage	I _{OH} = -400 μA	2.4		V
V _{OL}	Output LOW Voltage	I _{OL} = 2.1 mA		0.45	V
V _{IH}	Input HIGH Voltage		2.0	V _{CC} + 0.5	V
V _{IL}	Input LOW Voltage		-0.5	+0.8	V
I _{LI}	Input Load Current	V _{IN} = 0 V to +V _{CC}		1.0	μA
I _{LO}	Output Leakage Current	V _{OUT} = 0 V to +V _{CC}		5	μA
I _{CC1}	V _{CC} Active Current (Note 4)	$\overline{CE} = V_{IL}$, f = 10 MHz, I _{OUT} = 0 mA (Open Outputs)		40	mA
I _{CC2}	V _{CC} Standby Current	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$		1	mA
CMOS					
V _{OH}	Output HIGH Voltage	I _{OH} = -400 μA	2.4		V
V _{OL}	Output LOW Voltage	I _{OL} = 2.1 mA		0.45	V
V _{IH}	Input HIGH Voltage		V _{CC} - 0.3	V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage		-0.5	+0.8	V
I _{LI}	Input Load Current	V _{IN} = 0 V to +V _{CC}		1.0	μA
I _{LO}	Output Leakage Current	V _{OUT} = 0 V to +V _{CC}		5	μA
I _{CC1}	V _{CC} Active Current (Note 4)	$\overline{CE} = V_{IL}$, f = 10 MHz, I _{OUT} = 0 mA (Open Outputs)		40	mA
I _{CC2}	V _{CC} Standby Current	$\overline{CE} = V_{CC} \pm 0.3$ V		100	μA

CAPACITANCE (Notes 1, 2 & 5)

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Parameter Symbol	Parameter Description	Test Conditions	Max.	Unit
C _{IN1}	Address Input Capacitance	V _{IN} = 0 V	10	pF
C _{IN2}	\overline{OE} Input Capacitance	V _{IN} = 0 V	12	pF
C _{IN3}	\overline{CE} Input Capacitance	V _{IN} = 0 V	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0 V	10	pF

Notes:

1. Typical values are for nominal supply voltages.
2. This parameter is only sampled and not 100% tested.
3. **Caution:** The Am27X512 must not be removed from, or inserted into, a socket or board when V_{cc} is applied.
4. I_{cc1} is tested with $\overline{OE} = V_{IH}$ to simulate open outputs.
5. T_A = 25°C, f = 1 MHz.
6. During transitions, the input may overshoot GND to -2.0 V for periods of up to 20 ns.
Maximum DC voltage on input and output may overshoot to V_{cc} + 2.0 V for periods of up to 20 ns.

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 2 & 3)

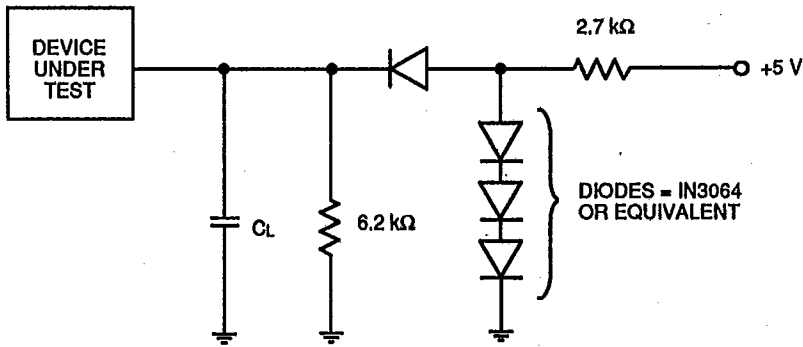
Parameter Symbol		Parameter Description	Test Conditions					Unit	
JEDEC	Standard			-125	-155 -150	-200	-250		
t _{AVQV}	t _{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$	Min.				ns	
				Max.	120	150	200		250
t _{ELQV}	t _{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Min.				ns	
				Max.	120	150	200		250
t _{GLQV}	t _{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$	Min.				ns	
				Max.	50	65	75		100
t _{EHQZ} t _{GHQZ}	t _{DF} (Note 1)	Output Enable HIGH to Output Float		Min.				ns	
				Max.	30	30	30		30
t _{AXQX}	t _{OH}	Output Hold from Addresses, \overline{CE} , or \overline{OE} , whichever occurred first		Min.	0	0	0	0	ns
				Max.					

Notes:

1. This parameter is only sampled and not 100% tested.
2. **Caution:** The Am27X512 must not be removed from, or inserted into, a socket or board when V_{cc} is applied.
3. Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: 20 ns
Input Pulse Levels: 0.45 to 2.4 V
Timing Measurement Reference Level—Inputs: 0.8 V and 2 V
Outputs: 0.8 V and 2 V

SWITCHING TEST CIRCUIT

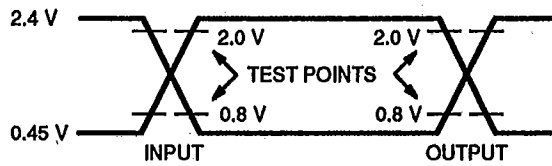
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10205-004A

$C_L = 100 \text{ pF}$ including jig capacitance

SWITCHING TEST WAVEFORM

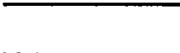



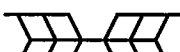


10205-009A

AC Testing: Inputs are driven at 2.4 V for a Logic "1" and 0.45 V for a Logic "0". Input pulse rise and fall times are $\leq 20\text{ns}$.

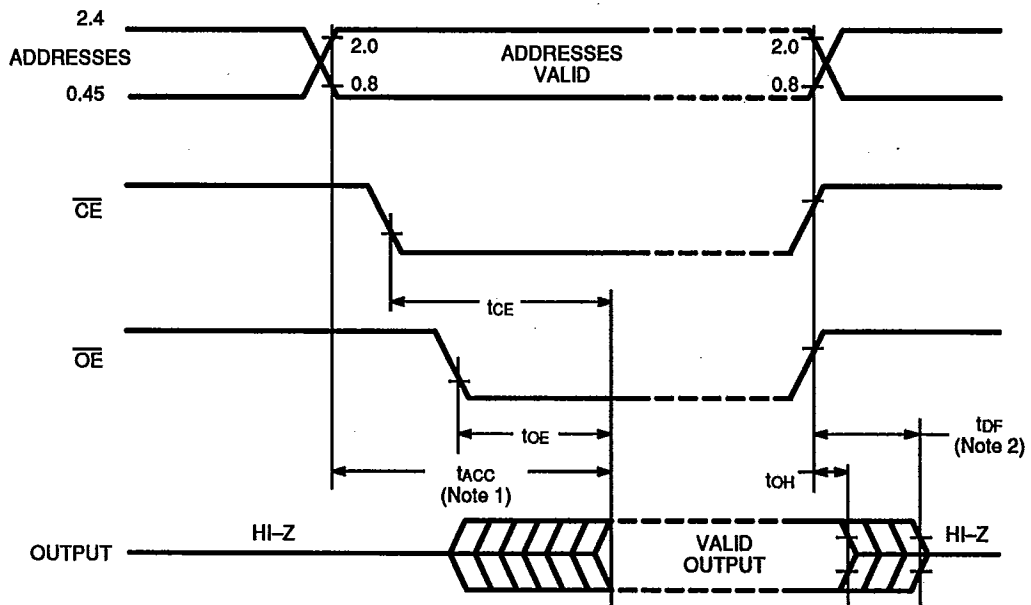
KEY TO SWITCHING WAVEFORMS

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WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORMS



10205-005A

Note:

- \overline{OE} may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of \overline{OE} without impact on t_{acc} .
- t_{DF} is specified from \overline{OE} or \overline{OEB} , whichever occurs first.