# MCP2025

## LIN Transceiver with Voltage Regulator

### Features

- The MCP2025 is compliant with:
  - LIN Bus Specifications Version 1.3, and 2.x
  - SAE J2602-2
- Supports Baud Rates up to 20 kBaud
- 43V Load Dump Protected
- Maximum Continuous Input Voltage of 30V
- Wide LIN Compliant Supply Voltage: 6.0-18.0V
- Extended Temperature Range: -40 to +125°C
- Interface to PIC® EUSART and Standard USARTs
- Wake-up on LIN Bus Activity or Local Wake Input
- LIN Bus Pin
  - Internal Pull-up Termination Resistor and Diode for Slave Node
  - Protected Against $V_{BAT}$ Shorts
  - Protected Against Loss of Ground
  - High Current Drive
- TXD and LIN Bus Dominant Time-out Function
- Two Low-power Modes
  - TRANSMITTER-OFF: 90 µA (typical)
  - POWER-DOWN mode: 4.5 µA (typical)
- MCP2025 On-chip Voltage Regulator
  - Output Voltage of 5.0V or 3.3V 70 mA Capability with Tolerances of ±3% Over Temperature Range.
  - Internal Short Circuit Current Limit
  - Only External Filter and Load Capacitors Needed
- Automatic Thermal Shutdown
- High Electromagnetic Immunity (EMI), Low Electromagnetic Emission (EME)
- Robust ESD Performance: ±15 kV for LBUS and VBB Pin (IEC61000-4-2)
- Transient Protection for LBUS and VBB pins in Automotive Environment (ISO7637)
- Meets stringent automotive design requirements including “OEM Hardware Requirements for LIN, CAN and FlexRay Interfaces in Automotive Applications”, Version 1.2, March 2011
- Multiple Package Options Including Small 4x4 mm DFN

### Description

The MCP2025 provides a bidirectional, half-duplex communication physical interface to meet the LIN bus specification Revision 2.1 and SAE J2602-2. The device incorporates a voltage regulator with 5V or 3.3V 70 mA regulated power supply output.

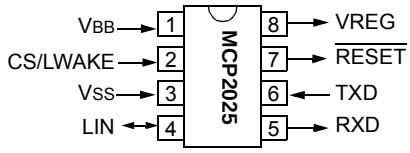
The device has been designed to meet the stringent quiescent current requirements of the automotive industry and will survive +43V load dump transients, and double battery jumps.

MCP2025 family members include:

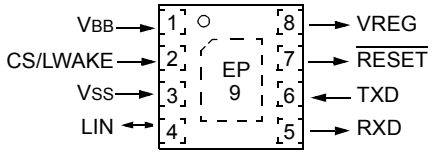
- MCP2025-500, 8-pin, LIN driver with 5.0V regulator
- MCP2025-330, 8-pin, LIN driver with 3.3V regulator

### Package Types (Top View)

PDIP, SOIC

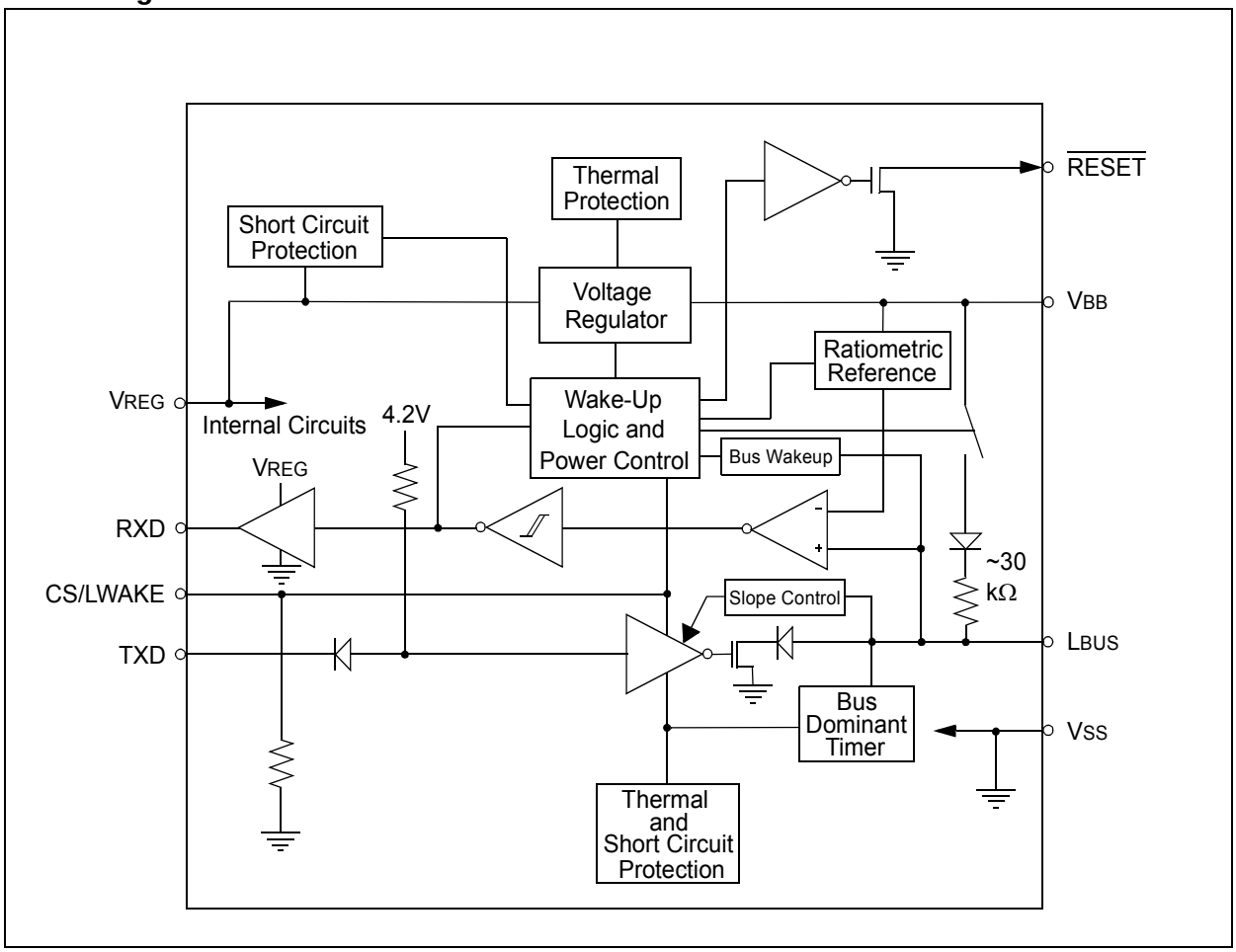



4x4 DFN




LOCAL INTERCONNECT NETWORK

## Block Diagram



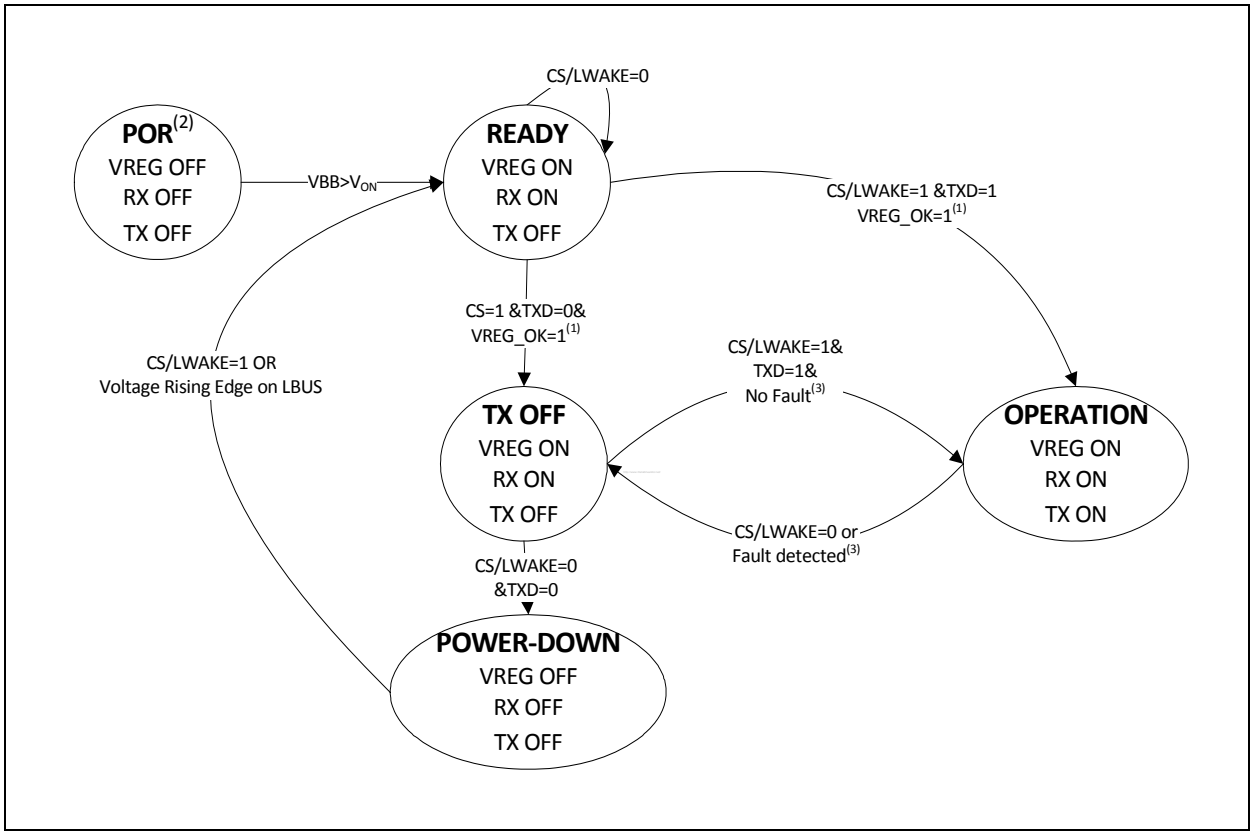
## 1.0 FUNCTION DESCRIPTION

The MCP2025 provides a physical interface between a microcontroller and a LIN half-duplex bus. It is intended for automotive and industrial applications with serial bus baud rates up to 20 kbaud. This device will translate the CMOS/TTL logic levels to LIN logic levels, and vice versa. The device offers optimum EMI and ESD performance; it can withstand high voltage on the LIN bus. The device supports two low-power modes to meet automotive industry power consumption requirements. The MCP2025 also provides a +5V or 3.3V 70 mA regulated power output.

### 1.1 Modes of Operation

The MCP2025 works in five modes: POWER-ON-RESET mode, POWER-DOWN mode, READY mode, OPERATION mode, and TRANSMITTER-OFF mode. For an overview of all operational modes, please refer to Table 1-1. For the operational mode transition, please refer to Figure 1-1.

**FIGURE 1-1: STATE DIAGRAM**




**Note 1:** VREG_OK : Regulator Output Voltage > 0.8$V_{REG_NOM}$.

**2:** If the voltage on pin VBB falls below $V_{OFF}$, the device will enter POWER-ON RESET mode from all other modes, which is not shown in the figure.

**3:** Faults include TXD/LBUS permanent dominant, LBUS short to VBB, thermal protection, and VREG_OK is false.

#### 1.1.1 POWER-ON-RESET MODE

Upon application of $V_{BB}$, or whenever the voltage on VBB is below the threshold of regulator turn off voltage $V_{OFF}$ (typically 4.50V), the device enters POWER-ON-RESET mode (POR). During this mode, the device maintains the digital section in a reset mode and waits until the voltage on pin VBB rises above the threshold of regulator turn on voltage $V_{ON}$ (typically 5.75V) to enter READY mode. In POWER-ON-RESET mode, the LIN physical layer and voltage regulator are disabled, and the $\overline{RESET}$ pin is switched to ground.

### 1.1.2 READY MODE

The device enters READY mode from POR mode after the voltage on $V_{BB}$ rises above the threshold of regulator turn on voltage $V_{ON}$ or from POWER-DOWN mode when a remote or local wake-up event happens.

Upon entering READY mode, the voltage regulator and receiver section of the transceiver are powered up. The transmitter remains in an off state. The device is ready to receive data but not to transmit. In order to minimize the power consumption, the regulator operates in a reduced power mode. It has a lower GBW product and thus is slower. However, the 70 mA drive capability is unchanged.

The device stays in READY mode until the output of the voltage regulator has stabilized and CS/LWAKE pin is HIGH ('1').

### 1.1.3 OPERATION MODE

If the CS/LWAKE pin changes to high while $V_{REG}$ is OK ($V_{REG}$ > 0.8*$V_{REG\_NOM}$) and TXD pin is HIGH, the part enters OPERATION mode from either READY or TRANSMITTER-OFF mode.

In this mode, all internal modules are operational. The internal pull-up resistor between LBUS and VBB is connected only in this mode.

The device goes to TRANSMITTER-OFF mode at the falling edge on the CS/LWAKE pin or when a fault is detected.

| **Note:** | The TXD pin needs to be set high before setting the CS/LWAKE pin to low in order to jump and stay in TRANSMITTER-OFF mode. If the TXD pin is set or maintained low before setting the CS/LWAKE pin to low, the part will transit to TRANSMITTER-OFF mode and then jump to POWER-DOWN mode after a deglitch delay of about 20 µs. |
|---|---|

### 1.1.4 TRANSMITTER OFF MODE

If $V_{REG}$ is OK ($V_{REG}$ > 0.8*$V_{REG\_NOM}$), the TRANSMITTER-OFF mode can be reached by setting CS/LWAKE to HIGH when TXD pin is LOW from READY mode; or by pulling down CS/LWAKE to low from OPERATION mode.

In TRANSMITTER-OFF mode, the receiver is enabled but the $L_{BUS}$ transmitter is off. It is a lower power mode.

In order to minimize the power consumption, the regulator operates in a reduced power mode. It has a lower GBW product and thus is slower. However, the 70 mA drive capability is unchanged.

The transmitter is also turned off whenever the voltage regulator is unstable or recovering from a fault. This prevents unwanted disruption on the bus during times of uncertain operation.

### 1.1.5 POWER-DOWN MODE

POWER-DOWN mode is entered by pulling down both the CS/LWAKE pin and TXD to low from TRANSMITTER-OFF mode. In POWER-DOWN mode, the transceiver and the voltage regulator are both off. Only the Bus Wake-up section and the CS/LWAKE pin wake-up circuits are in operation. This is the lowest power mode.

If any bus activity (e.g. a BREAK character) occurs or CS/LWAKE is set to HIGH during POWER-DOWN mode, the device will immediately enter READY mode and enable the voltage regulator. Then, once the regulator output has stabilized (approximately 0.3 ms to 1.2 ms) it can go to either the OPERATION mode or TRANSMITTER-OFF mode. Refer to **Section 1.1.6 "Remote Wake-up"** for more details.

### 1.1.6 REMOTE WAKE-UP

The remote wake-up sub module observes the $L_{BUS}$ in order to detect bus activity. In POWER-DOWN mode, the normal LIN recessive/dominant threshold is disabled, and the LIN bus Wake-Up Voltage Threshold $V_{WK(LBUS)}$ is used to detect bus activities. Bus activity is detected when the voltage on the $L_{BUS}$ falls below the LIN bus Wake-Up Voltage Threshold $V_{WK(LBUS)}$ (approximately 3.4V) for at least $t_{BDB}$ (a typical duration of 80 µs ) followed by a rising edge. Such a condition causes the device to leave POWER-DOWN mode.

**TABLE 1-1: OVERVIEW OF OPERATIONAL MODES**

| State | Transmitter | Receiver | Internal Wake Module | Voltage Regulator | Operation | Comments |
|---|---|---|---|---|---|---|
| POWER-ON-RESET | OFF | OFF | OFF | OFF | Transfer to READYmode after $V_{BB}$ > $V_{ON}$ | |
| READY | OFF | ON | OFF | ON | If CS/LWAKE is high, then proceed to OPERATION or TRANSMITTER-OFF mode | Bus Off state |
| OPERATION | ON | ON | OFF | ON | If CS/LWAKE is low level, then TRANSMITTER-OFF mode | Normal operation mode |
| POWER-DOWN | OFF | OFF | ON Activity Detect | OFF | On LIN bus rising edge or CS/LWAKE high level, go to READY mode | Lowest power mode |
| TRANSMITTER-OFF | OFF | ON | OFF | ON | If TXD and CS/LWAKE low level, then POWER-DOWN<br>If TXD and CS/LWAKE high level, then OPERATION | Bus Off state, lower power mode |

## 1.2 Pin Descriptions

Please refer to Table 1-2 for the pinout overview.

### 1.2.1 VBB

Battery Positive Supply Voltage pin. An external diode is connected in series to prevent the device from being reversely powered (refer to Figure 1-9).

### 1.2.2 VREG

Positive Supply Voltage Regulator Output pin. An on-chip Low Dropout Regulator (LDO) gives +5.0 or +3.3V 70 mA regulated voltage on this pin.

### 1.2.3 VSS

Ground pin.

### 1.2.4 TXD

Transmit data input pin (TTL level, HV compliant, adaptive pull-up). The transmitter reads the data stream on the TXD pin and sends it to the LIN bus. The LBUS pin is low (dominant) when TXD is low, and high (recessive) when TXD is high.

The Transmit Data Input pin has an internal adaptive pull-up to an internally-generated 4.2V (approximately). When TXD is '0', a weak pull-up (~900 kΩ) is used to reduce current. When TXD is '1' a stronger pull-up (~300 kΩ) is used to maintain the logic level. A series reverse-blocking diode allows applying TXD input voltages greater than the internally generated 4.2V and renders the TXD pin HV compliant up to 30V (see Block Diagram).

### 1.2.5 RXD

Receive Data Output pin. The RXD pin is a standard CMOS output pin and it follows the state of the LBUS pin.

### 1.2.6 LBUS

LIN Bus pin. LBUS is a bidirectional LIN bus Interface pin and is controlled by the signal TXD. It has an open collector output with a current limitation. To reduce ElectroMagnetic Emission, the slopes during signal changes are controlled, and the LBUS pin has corner-rounding control for both falling and rising edges.

The internal LIN receiver observes the activities on the LIN bus, and generates the output signal RXD that follows the state of the LBUS. A first degree 160 KHz, low-pass input filter optimizes ElectroMagnetic immunity.

### 1.2.7 CS/LWAKE

Chip Select and Local Wake-up Input pin (TTL level, high voltage tolerant). This pin controls the device state transition. Refer to Figure 1-1.

An internal pull-down resistor will keep the CS/LWAKE pin low to ensure that no disruptive data will be present on the bus while the microcontroller is executing a POWER-ON RESET and I/O initialization sequence. When CS/LWAKE is '1', a weak pull-down (~600 KΩ) is used to reduce current. When CS/LWAKE is '0' a stronger pull-down (~300 KΩ) is used to maintain the logic level.

This pin may also be used as a local wake-up input (See Figure 1-9). The microcontroller will set the I/O pin to control the CS/LWAKE. An external switch, or other source, can then wake-up both the transceiver and the microcontroller.

| **Note:** | CS/LWAKE should NOT be tied directly to pin VREG as this could force the MCP2025 into OPERATION mode before the microcontroller is initialized. |
|---|---|

### 1.2.8 $\overline{\text{RESET}}$

RESET OUTPUT pin. This is an open drain output pin. It indicates the internal voltage has reached a valid, stable level. As long as the internal voltage is valid (above 0.8VREG), this pin will present high impedance; otherwise the $\overline{\text{RESET}}$ pin switches to ground.

**TABLE 1-2: PINOUT OVERVIEW**

| PIN Name | PIN Number | PIN Type | Function |
|---|---|---|---|
| VREG | 8 | Output | Voltage regulator output |
| VSS | 3 | Power | Ground |
| VBB | 1 | Power | Battery |
| TXD | 6 | Input, HV-tolerant | Transmit data input |
| RXD | 5 | Output | Receive data output |
| LBUS | 4 | I/O, HV | LIN Bus |
| CS/LWAKE | 2 | TTL Input, HV-tolerant | Chip Select and Local Wake-up input |
| $\overline{\text{RESET}}$ | 7 | Open Drain Output, HV-tolerant | Reset output |

## 1.3 Fail-Safe Features

### 1.3.1 GENERAL FAIL-SAFE FEATURES

- An internal pull-down resistor on the CS/LWAKE pin disables the transmitter if the pin is floating.
- An internal pull-up resistor on the TXD pin places TXD in HIGH, thus the LBUS is recessive if the TXD pin is floating.
- High-impedance and low leakage current on LBUS during loss of power or ground.
- The current limit on LBUS protects the transceiver from being damaged if the pin is shorted to VBB.

### 1.3.2 THERMAL PROTECTION

The thermal protection circuit monitors the die temperature and is able to shut down the LIN transmitter and voltage regulator.

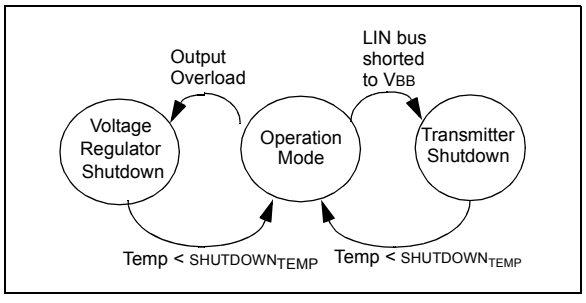
There are three causes for a thermal overload. A thermal shut down can be triggered by any one, or a combination of, the following thermal overload conditions:

- Voltage regulator overload
- LIN bus output overload
- Increase in die temperature due to increase in environment temperature

The recovery time from the thermal shutdown is equal to adequate cooling time.

Driving the TXD and checking the RXD pin makes it possible to determine whether there is a bus contention (TXD = high, RXD = low) or a thermal overload condition (TXD = low, RXD = high).

**FIGURE 1-2: THERMAL SHUTDOWN STATE DIAGRAMS**




### 1.3.3 TXD/LBUS TIME-OUT TIMER

The LIN bus can be driven to a dominant level either from the TXD pin or externally. An internal timer deactivates the LBUS transmitter if a dominant status (LOW) on the LIN bus lasts longer than Bus Dominant Time-out Time $t_{TO(LIN)}$ (approximately 20 milliseconds); at the same time, RXD output is put in recessive (HIGH) and the internal pull-up resistor between LBUS and VBB is disconnected. The timer is reset on any recessive LBUS status or POR mode. The recessive status on LBUS can be caused either by the bus being externally pulled up or by the TXD pin being returned high.

## 1.4 Internal Voltage Regulator

The MCP2025 has a positive regulator capable of supplying +5.00 or +3.30 VDC ±3% at up to 70mA of load current over the entire operating temperature range of -40°C to +125°C. The regulator uses an LDO design, is short-circuit-protected and will turn the regulator output off if its output falls below the Shutdown Voltage Threshold $V_{SD}$.

With a load current of 70mA, the minimum input to output voltage differential required for the output to remain in regulation is typically +0.5V (+1V maximum over the full operating temperature range). Quiescent current is less than 100 µA with a full 70mA load current when the input to output voltage differential is greater than +3.00V.

Regarding the correlation between VBB, $V_{REG}$ and IDD, please refer to Figure 1-6 and Figure 1-7. When the input voltage (VBB) drops below the differential needed to provide stable regulation, the voltage regulator output $V_{REG}$ will track the input down to approximately $V_{OFF}$. The regulator will turn off the output at this point. This will allow PIC microcontrollers, with internal POR circuits, to generate a clean arming of the POWER-ON RESET trip point. The MCP2025 will then monitor VBB and turn on the regulator when VBB is above the threshold of regulator turn on voltage $V_{ON}$.

Under specific ambient temperature and battery voltage range, the voltage regulator can output as high as 150 mA current. For current load capability of the voltage regulator, refer to Figure 1-4 and Figure 1-5.

In POWER-DOWN mode, the VBB monitor is turned off (see **Section 1.1.5 "Power-down Mode"** for details).

| **Note:** | The regulator overload current limit is approximately 250 mA. The regulator output voltage $V_{REG}$ is monitored. If output voltage $V_{REG}$ is lower than $V_{SD}$, the voltage regulator will turn off. After a recovery time of about 3mS, the $V_{REG}$ will be checked again. If there is no short circuit, ($V_{REG}$ > $V_{SD}$) then the voltage regulator remains on. |
|---|---|

The regulator requires an external output bypass capacitor for stability. See **FIGURE 2-1: "ESR Curves For Load Capacitor Selection"** for correct capacity and ESR for stable operation.

**FIGURE 1-3: VOLTAGE REGULATOR BLOCK DIAGRAM**

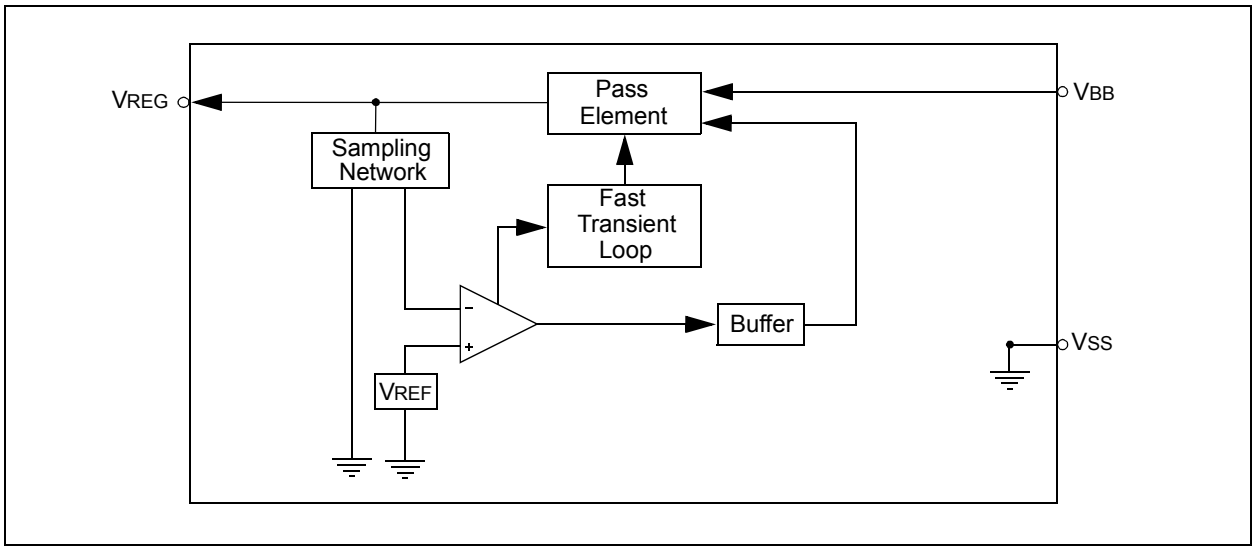



**FIGURE 1-4: 5.0V $V_{REG}$ VS. $I_{REG}$ AT $V_{BB}$ = 12V**

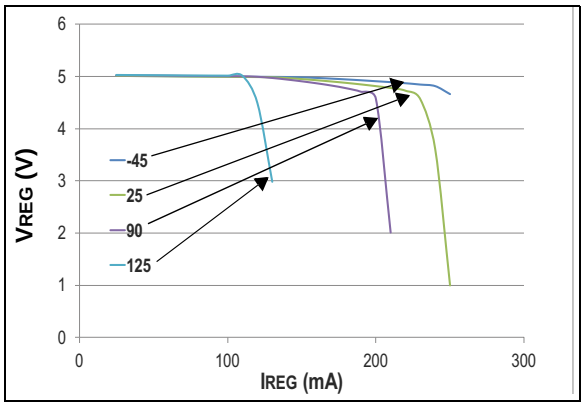



**FIGURE 1-5: 3.3V $V_{REG}$ VS. $I_{REG}$ AT $V_{BB}$ = 12V**

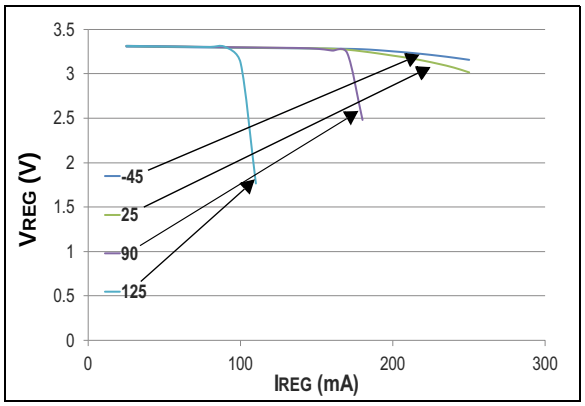
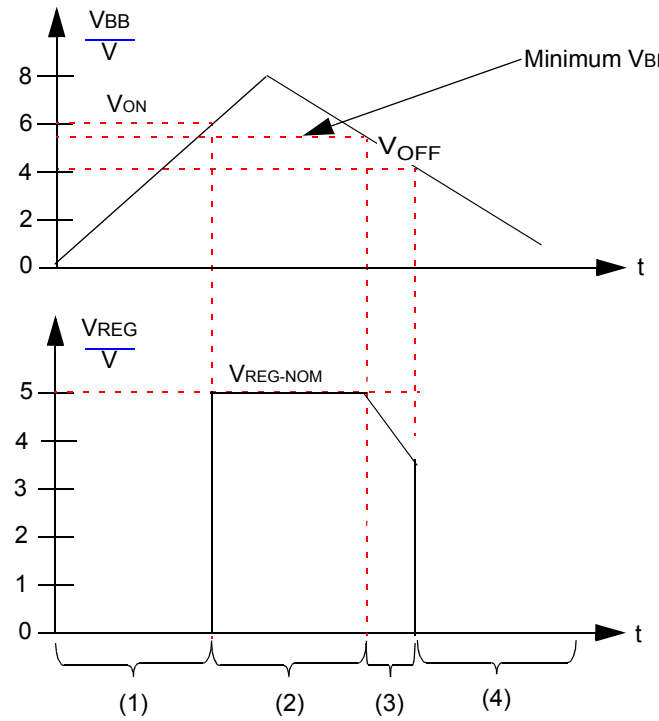


**FIGURE 1-6: VOLTAGE REGULATOR OUTPUT ON POWER-ON RESET**



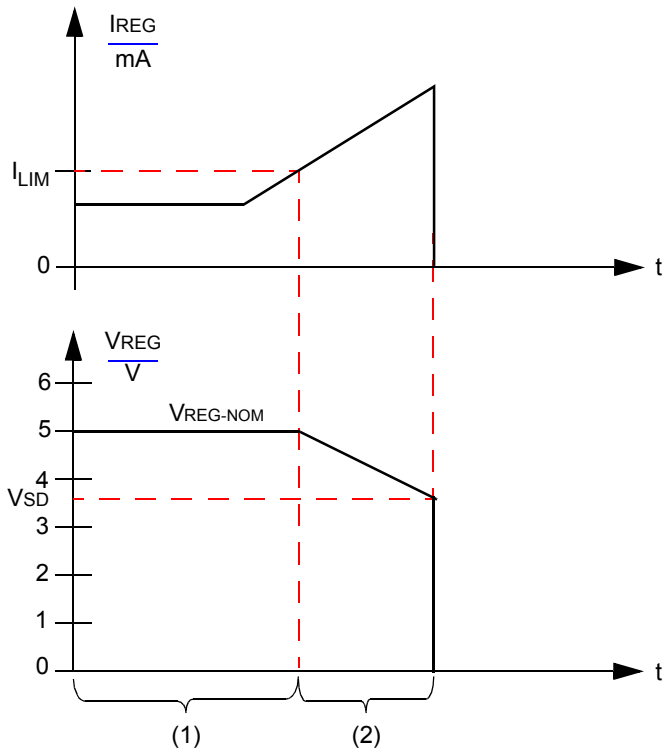

**Note 1:** Start-up, $V_{BB} < V_{ON}$, regulator off

**2:** $V_{BB} > V_{ON}$, regulator on

**3:** $V_{BB} \leq$ Minimum $V_{BB}$ to maintain regulation

**4:** $V_{BB} < V_{OFF}$, regulator will turn off

**FIGURE 1-7: VOLTAGE REGULATOR OUTPUT ON OVER CURRENT SITUATION**




**Note 1:** $I_{REG}$ less than $I_{LIM}$, regulator on

**2:** After $I_{REG}$ exceeds $I_{LIM}$, voltage regulator output will be reduced until voltage regulator shutdown voltage $V_{SD}$ is reached.

## 1.5 Optional External Protection

### 1.5.1 REVERSE BATTERY PROTECTION

An external reverse-battery-blocking diode should be used to provide polarity protection (see Figure 1-9).

### 1.5.2 TRANSIENT VOLTAGE PROTECTION (LOAD DUMP)

An external 43V transient suppressor (TVS) diode, between $V_{BB}$ and ground, with a transient protection resistor ($R_{TP}$) in series with the battery supply and the $V_{BB}$ pin protects the device from power transients and ESD events greater than 43V (see Figure 1-9). The maximum value for the $R_{TP}$ protection resistor depends upon two parameters: the minimum voltage the part will start at, and the impacts of this $R_{TP}$ resistor on the $V_{BB}$ value, thus on the Bus recessive level and slopes.

This leads to a set of three equations to fulfill.

Equation 1-1 provides a max $R_{TP}$ value, according to the minimum battery voltage the user wants the part to start with.

Equation 1-2 provides a max $R_{TP}$ value according to the maximum error on the recessive level, thus $V_{BB}$, since the part uses $V_{BB}$ as the reference value for the recessive level.

Equation 1-3 provides a max $R_{TP}$ value according to the maximum relative variation the user can accept on the slope when $I_{REG}$ varies.

Since both Equation 1-1 and Equation 1-2 must be fulfilled, the maximum allowed value for RTP is the smaller of the two values found when solving Equation 1-1 and Equation 1-2.

Usually, Equation 1-1 gives the higher constraint (smaller value) for $R_{TP}$ as shown in the example where $V_{BATmin}$ is 8V.

However, the user needs to verify that the value found in Equation 1-1 also satisfies Equation 1-2 and Equation 1-3.

While this protection is optional, it should be considered as good engineering practice.

**EQUATION 1-1:**

$$R_{TP} \leq \frac{V_{BATmin} - 5.5V}{250mA}$$

$$5.5V = V_{OFF} + 1.0V$$

*250 mA is the peak current at power-on when $V_{BB}$ = 5.5V*

Assume that $V_{BATmin}$ = 8V. Equation 1-1 gives 10Ω.

**EQUATION 1-2:**

*$R_{TP}$ <= $\Delta V_{RECCESSIVE}$ / $I_{REGMAX}$.*
*$\Delta V_{RECCESSIVE}$ is the maximum variation tolerated on the recessive level*

Assume that $\Delta V_{RECCESSIVE}$ = 1V and $I_{REGMAX}$=50 mA. Equation 1-2 gives 20Ω.

**EQUATION 1-3:**

$$R_{TP} \leq \frac{\Delta Slope \times (V_{BATmin} - 1V)}{I_{regmax}}$$

*ΔSlope is the maximum variation tolerated on the slope level and $I_{regmax}$ is the maximum current the regulator will provide to the load.*
*$V_{BATmin}$>$V_{OFF}$ + 1.0V,*

Assume that ΔSlope =15%, $V_{BATmin}$=8V and $I_{REGMAX}$ = 50 mA. Equation 1-3 gives 20Ω.

### 1.5.3 CBAT CAP

Selecting CBAT = 10* CREG is recommended, however this leads to a high value cap. Lower values for CBAT cap can be used, but certain rules must be followed. In any case, the voltage at the VBB pin should remain above VOFF when the device is turned on.

The current peak at start-up (due to the fast charge of the CREG and CBAT capacitor) may induce a significant drop on the VBB pin. This drop is proportional to the impedance of the VBAT connection (see Figure 1-9).

Let's assume that the VBAT connection is mainly inductive and resistive, and that the customer knows the resistive and inductive values of the connection.

The following formula gives an indication of the minimum value the customer should use for CBAT:

**EQUATION 1-4:**

$$\frac{C_{BAT}}{C_{REG}} = \sqrt{\frac{100L^2 + R_{tot}^2}{1 + L^2 + \frac{R_{tot}^2}{100}}}$$

where L is in mH and RTOT in Ω.
RTOT = RLINE + RTP

Equation 1-4 allows lower CBAT/CREG values than the 10* ratio we recommend.

Assumee that we have a good quality connection with RTOT = 0.1Ω and L = 0.1 mH.

Solving the equation results in CBAT/CREG = 1.

If RTOT is increased to 1Ω, the result becomes CBAT/CREG = 1.4

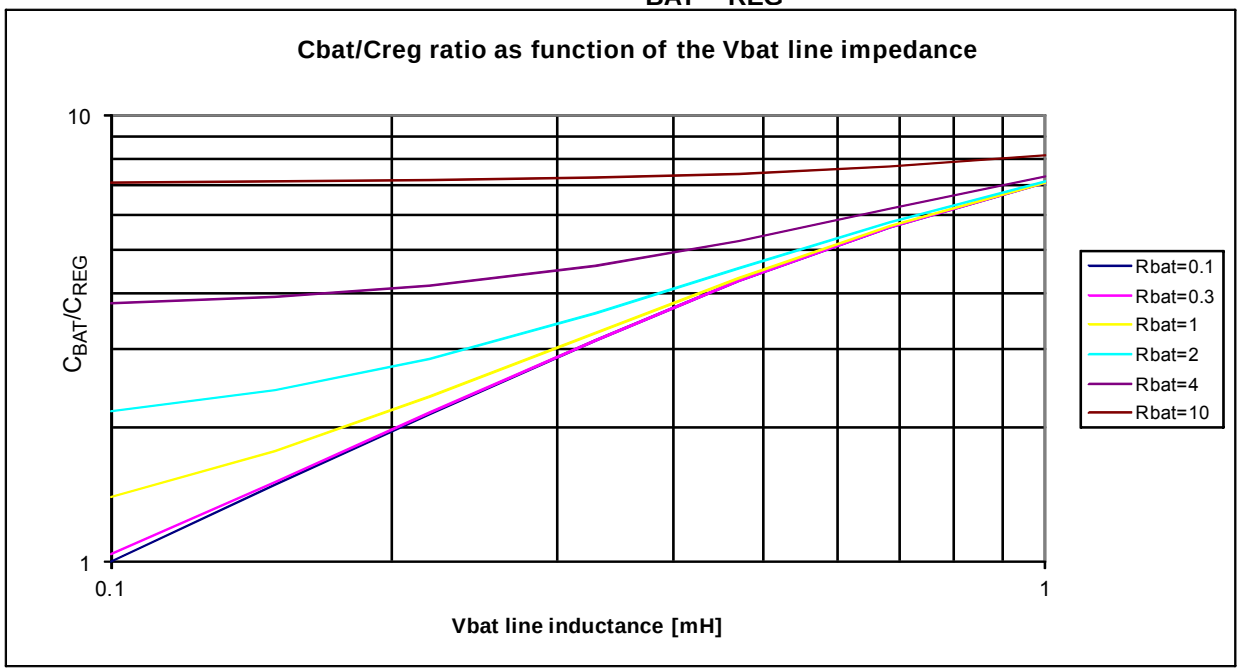
But if the connection is highly resistive or highly inductive (poor connection), the CBAT/CREG ratio greatly increases.

For a highly inductive connection: RTOT = 0.1Ω and L = 1 mH; the CBAT/CREG ratio increases to 7.

For a highly resistive connection: RTOT = 10Ω and L = 0.1 mH: again, the CBAT/CREG ratio increases to 7.

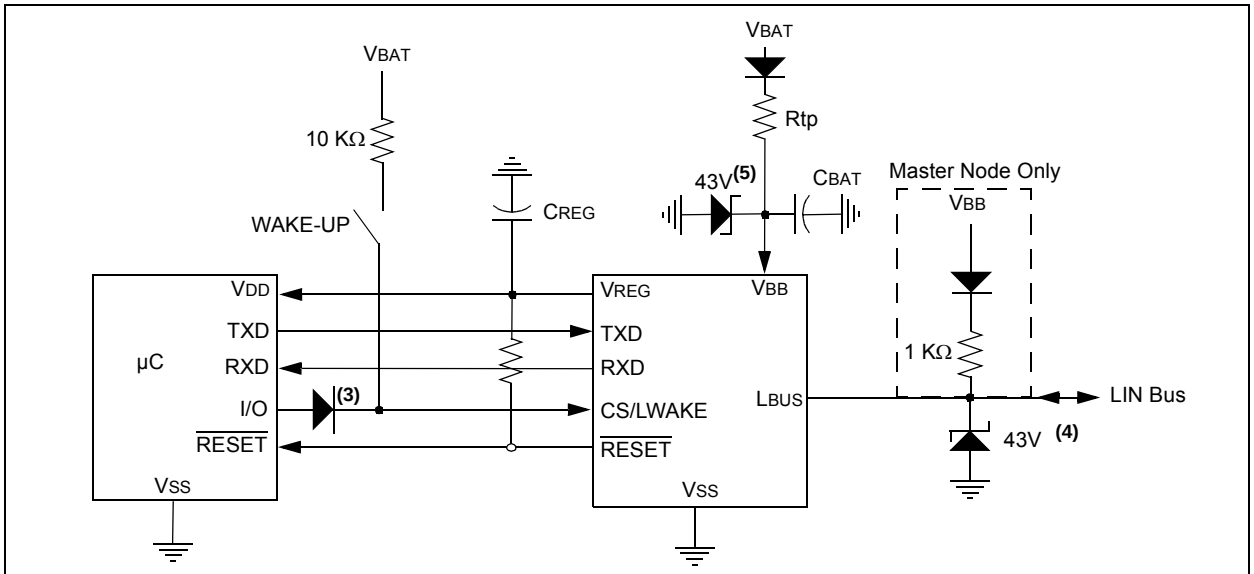
Figure 1-8 shows the minimum recommended CBAT/CREG ratio as a function of the impedance of the VBAT connection.

**FIGURE 1-8: Minimum Recommended $C_{BAT}/C_{REG}$ Ratio**



## 1.6 Typical Applications

**FIGURE 1-9: TYPICAL APPLICATION CIRCUIT**




**Note 1:** CREG, the load capacitor, should be ceramic or tantalum-rated for extended temperatures, 1.0-22 µF. See Figure 2-1 for selecting correct ESR.

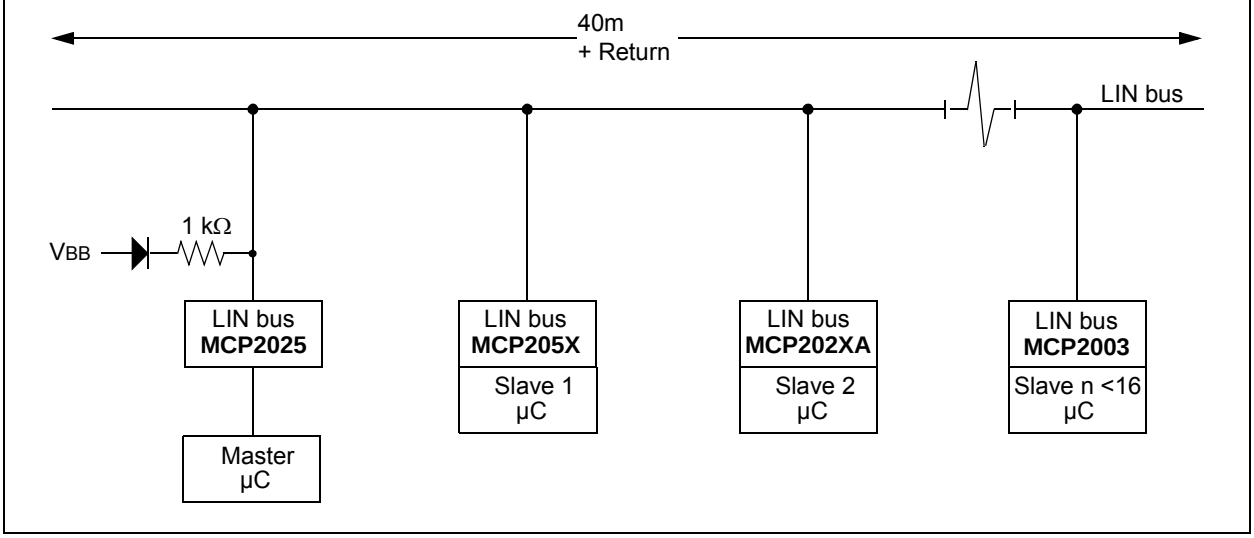
**2:** CBAT is the filter capacitor for the external voltage supply. Typically 10 * CREG with no ESR restriction. See Figure 1-8 to select the minimum recommended value for CBAT. The RTP value is added to the line resistance.

**3:** This diode is only needed if CS/LWAKE is connected to VBAT supply.

**4:** Transient suppressor diode. Vclamp L = 43V.

**5:** This component is for additional load dump protection.

**FIGURE 1-10: TYPICAL LIN NETWORK CONFIGURATION**



# 2.0 ELECTRICAL CHARACTERISTICS

## 2.1 Absolute Maximum Ratings†

$V_{IN}$ DC Voltage on RXD, and $\overline{RESET}$ ..... -0.3V to $V_{REG}$+0.3
$V_{IN}$ DC Voltage on TXD, CS/LWAKE ..... -0.3 to +40V
$V_{BB}$ Battery Voltage, continuous, non-operating (**Note 1**) ..... -0.3 to +40V
$V_{BB}$ Battery Voltage, non-operating (LIN bus recessive, no regulator load, t < 60s) (**Note 2**) ..... -0.3 to +43V
$V_{BB}$ Battery Voltage, transient ISO 7637 Test 1 ..... -100V
$V_{BB}$ Battery Voltage, transient ISO 7637 Test 2a ..... +75V
$V_{BB}$ Battery Voltage, transient ISO 7637 Test 3a ..... -150V
$V_{BB}$ Battery Voltage, transient ISO 7637 Test 3b ..... +100V
$V_{LBUS}$ Bus Voltage, continuous ..... -18 to +30V
$V_{LBUS}$ Bus Voltage, transient (**Note 3**) ..... -27 to +43V
$I_{LBUS}$ Bus Short Circuit Current Limit ..... 200 mA
ESD protection on LIN, $V_{BB}$ (IEC 61000-4-2) (**Note 4**) ..... ±15 kV
ESD protection on LIN, $V_{BB}$ (Human Body Model) (**Note 5**) ..... ±8 kV
ESD protection on all other pins (Human Body Model) (**Note 5**) ..... ±4 kV
ESD protection on all pins (Charge Device Model) (**Note 6**) ..... ±1500V
ESD protection on all pins (Machine Model) (**Note 7**) ..... ±200V
Maximum Junction Temperature ..... 150°C
Storage Temperature ..... -65 to +150°C

**Note 1:** LIN 2.x compliant specification.

**2:** SAE J2602 compliant specification.

**3:** ISO 7637 immunity against transients (t < 500 ms).

**4:** According to IEC 61000-4-2, 330Ω, 150 pF and Transceiver EMC Test Specifications [2] to [4].

**5:** According to AEC-Q100-002 / JESD22-A114.

**6:** According to AEC-Q100-011B.

**7:** According to AEC-Q100-003 / JESD22-A115.

† **NOTICE**: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

## 2.2 Nomenclature Used in this Document

Some terms and names used in this data sheet deviate from those referred to in the LIN specifications. Equivalent values are shown below.

| LIN 2.1 Name | Term used in the following tables | |
|---|---|---|
| $V_{BAT}$ | *not used* | ECU operating voltage |
| $V_{SUP}$ | $V_{BB}$ | Supply voltage at device pin |
| $V_{BUS\_LIM}$ | $I_{SC}$ | Current limit of driver |
| $V_{BUSREC}$ | $V_{IH(LBUS)}$ | Recessive state |
| $V_{BUSDOM}$ | $V_{IL(LBUS)}$ | Dominant state |

## 2.3 DC Specifications

| DC Specifications | **Electrical Characteristics:**<br>Unless otherwise indicated, all limits are specified for:<br>$V_{BB}$ = 6.0V to 18.0V<br>$T_A$ = -40°C to +125°C | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Sym.** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| **Power** | | | | | | |
| $V_{BB}$ Quiescent Operating Current | $I_{BBQ}$ | — | — | 200 | µA | $I_{OUT}$ = 0 mA, LBUS recessive $V_{REG}$ = 5.0V |
| | | — | — | 200 | µA | $I_{OUT}$ = 0 mA, LBUS recessive $V_{REG}$ = 3.3V |
| $V_{BB}$ Ready Current | $I_{BBRD}$ | — | — | 100 | µA | $I_{OUT}$ = 0 mA, LBUS recessive $V_{REG}$ = 5.0V |
| | | — | — | 100 | µA | $I_{OUT}$ = 0 mA, LBUS recessive $V_{REG}$ = 3.3V |
| $V_{BB}$ Transmitter-off Current with Watchdog Disabled | $I_{BBTO}$ | — | — | 100 | µA | With voltage regulator on, transmitter off, receiver on, CS = $V_{IH}$,$V_{REG}$ = 5.0V |
| | | — | — | 100 | µA | With voltage regulator on, transmitter off, receiver on, CS = $V_{IH}$,$V_{REG}$ = 3.3V |
| $V_{BB}$ Power-down Current | $I_{BBPD}$ | — | 4.5 | 8 | µA | With voltage regulator powered off, receiver on and transmitter off, CS = $V_{IL}$. |
| $V_{BB}$ Current with $V_{SS}$ Floating | $I_{BBNOGND}$ | -1 | — | 1 | mA | $V_{BB}$ = 12V, GND to $V_{BB}$, $V_{LIN}$ = 0-18V |
| **Microcontroller Interface** | | | | | | |
| High-level Input Voltage (TXD) | $V_{IH}$ | 2.0 | — | 30 | V | |
| Low-level Input Voltage (TXD) | $V_{IL}$ | -0.3 | — | 0.8 | V | |
| High-level Input Current (TXD) | $I_{IH}$ | -2.5 | — | 0.4 | µA | Input voltage = 4.0V. ~800 kΩ internal adaptive pull-up |
| Low-level Input Current (TXD) | $I_{IL}$ | -10 | — | — | µA | Input voltage = 0.5V. ~800 kΩ internal adaptive pull-up |
| High-level Input Voltage (CS/LWAKE) | $V_{IH}$ | 2 | — | 30 | V | Through a current-limiting resistor |
| Low-level Input Voltage (CS/LWAKE) | $V_{IL}$ | -0.3 | — | 0.8 | V | |
| High-level Input Current (CS/LWAKE) | $I_{IH}$ | — | — | 8.0 | µA | Input voltage = 0.8$V_{REG}$ ~1.3 MΩ internal pull-down to $V_{SS}$ |
| Low-level Input Current (CS/LWAKE) | $I_{IL}$ | — | — | 5.0 | µA | Input voltage = 0.2$V_{REG}$ ~1.3 MΩ internal pull-down to $V_{SS}$ |
| Low-level Output Voltage (RXD) | $V_{OLRXD}$ | — | — | 0.2$V_{REG}$ | V | $I_{OL}$ = 2 mA |
| High-level Output Voltage (RXD) | $V_{OHRXD}$ | 0.8 $V_{REG}$ | — | — | V | $I_{OH}$ = 2 mA |

**Note 1:** Internal current limited. 2.0 ms maximum recovery time ($R_{LBUS}$ = 0Ω, TX = 0, $V_{LBUS}$ = $V_{BB}$).

**2:** For design guidance only, not tested.

**3:** In POWER-DOWN mode, normal LIN recessive/dominant threshold is disabled; $V_{WK(LBUS)}$ is used to detect bus activities.

## 2.3 DC Specifications (Continued)

| DC Specifications | **Electrical Characteristics:**<br>Unless otherwise indicated, all limits are specified for:<br>$V_{BB}$ = 6.0V to 18.0V<br>$T_A$ = -40°C to +125°C | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Sym.** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| **Bus Interface (DC specifications are for a $V_{BB}$ range of 6.0 to 18.0V)** | | | | | | |
| High-level Input Voltage | $V_{IH(LBUS)}$ | 0.6 $V_{BB}$ | — | — | V | Recessive state |
| Low-level Input Voltage | $V_{IL(LBUS)}$ | -8 | — | 0.4 $V_{BB}$ | V | Dominant state |
| Input Hysteresis | $V_{HYS}$ | — | — | 0.175 $V_{BB}$ | V | $V_{IH(LBUS)} – V_{IL(LBUS)}$ |
| Low-level Output Current | $I_{OL(LBUS)}$ | 40 | — | 200 | mA | Output voltage = 0.1 $V_{BB}$, $V_{BB}$ = 12V |
| Pull-up Current on Input | $I_{PU(LBUS)}$ | -180 | — | -72 | µA | ~30 kΩ internal pull-up @ $V_{IH}$ ($L_{BUS}$) = 0.7 $V_{BB}$, $V_{BB}$=12V |
| Short Circuit Current Limit | $I_{SC}$ | 50 | — | 200 | mA | **(Note 1)** |
| High-level Output Voltage | $V_{OH(LBUS)}$ | 0.8 $V_{BB}$ | — | $V_{BB}$ | V | |
| Driver Dominant Voltage | V_LOSUP | — | — | 1.1 | V | $V_{BB}$ = 7.3V, $R_{LOAD}$ = 1000Ω |
| Driver Dominant Voltage | V_HISUP | — | — | 1.2 | V | $V_{BB}$ = 18V, $R_{LOAD}$ = 1000Ω |
| Input Leakage Current (at the receiver during dominant bus level) | $I_{BUS\_PAS\_DOM}$ | -1 | — | — | mA | Driver off, $V_{BUS}$ = 0V, $V_{BB}$ = 12V |
| Input Leakage Current (at the receiver during recessive bus level) | $I_{BUS\_PAS\_REC}$ | -20 | — | 20 | µA | Driver off, 8V < $V_{BB}$ < 18V 8V < $V_{BUS}$ < 18V $V_{BUS} \geq V_{BB}$ |
| Leakage Current (disconnected from ground) | $I_{BUS\_NO\_GND}$ | -10 | — | +10 | µA | $GND_{DEVICE}$ = $V_{BB}$, 0V < $V_{BUS}$ < 18V, $V_{BB}$ = 12V |
| Leakage Current (disconnected from $V_{BB}$) | $I_{BUS\_NO\_PWR}$ | -10 | — | +10 | µA | $V_{BB}$ = GND, 0 < $V_{BUS}$ < 18V |
| Receiver Center Voltage | $V_{BUS\_CNT}$ | 0.475 $V_{BB}$ | 0.5 $V_{BB}$ | 0.525 $V_{BB}$ | V | $V_{BUS\_CNT}$ = ($V_{IL}$ ($L_{BUS}$) + $V_{IH}$ ($L_{BUS}$))/2 |
| Slave Termination | $R_{SLAVE}$ | 20 | 30 | 47 | kΩ | (**Note 2**) |
| Capacitance of slave node | $C_{SLAVE}$ | | | 50 | pF | (**Note 2**) |
| Wake-Up Voltage Threshold on LIN Bus | $V_{WK(LBUS)}$ | — | — | 3.4 | V | Wake up from POWER-DOWN mode (**Note 3**) |

**Note 1:** Internal current limited. 2.0 ms maximum recovery time ($R_{LBUS}$ = 0Ω, TX = 0, $V_{LBUS}$ = $V_{BB}$).

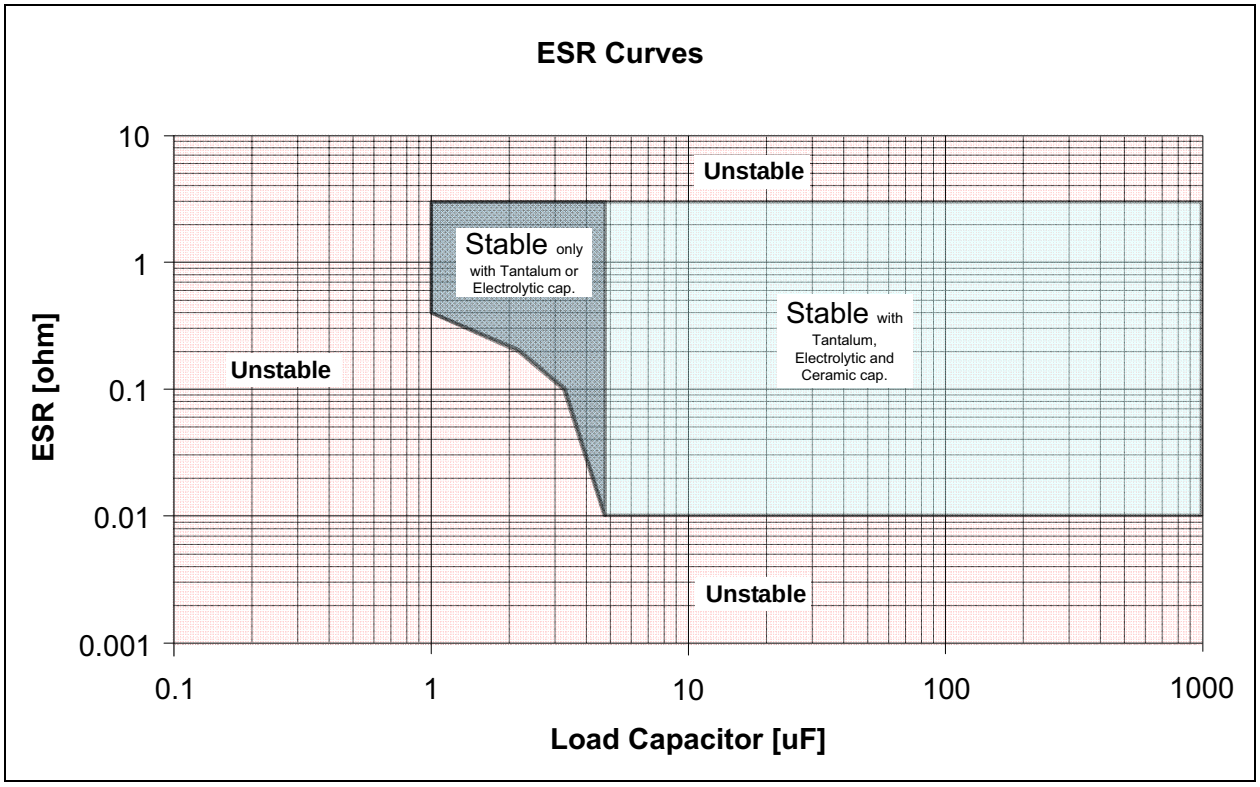
**2:** For design guidance only, not tested.

**3:** In POWER-DOWN mode, normal LIN recessive/dominant threshold is disabled; $V_{WK(LBUS)}$ is used to detect bus activities.

## 2.3 DC Specification (Continued)

| DC Specifications | **Electrical Characteristics:**<br>Unless otherwise indicated, all limits are specified for:<br>$V_{BB}$ = 6.0V to 18.0V<br>$T_A$ = -40°C to +125°C<br>$C_{LOADREG}$ = 10 µF | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Sym.** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| **Voltage Regulator - 5.0V** | | | | | | |
| Output Voltage Range | $V_{REG}$ | 4.85 | 5.00 | 5.15 | V | 0 mA < $I_{OUT}$ < 70 mA |
| Line Regulation | $\Delta V_{OUT}1$ | — | 10 | 50 | mV | $I_{OUT}$ = 1 mA,<br>6.0V < $V_{BB}$ < 18V |
| Load Regulation | $\Delta V_{OUT}2$ | — | 10 | 50 | mV | 5 mA < $I_{OUT}$ <70 mA<br>6.0V < $V_{BB}$ < 12V |
| Power Supply Ripple Reject | PSRR | — | — | 50 | dB | 1 $V_{PP}$ @10-20 kHz<br>$I_{LOAD}$ = 20 mA |
| Output Noise Voltage | eN | — | — | 100 | µ$V_{RMS}$ | 10 Hz – 40 MHz<br>$C_{FILTER}$ = 10 µf,<br>$C_{BP}$ = 0.1 µf, $I_{LOAD}$ = 20 mA |
| Shutdown Voltage Threshold | $V_{SD}$ | 3.5 | — | 4.0 | V | See Figure 1-7 (**Note 1**) |
| Input Voltage to Turn-off Output | $V_{OFF}$ | 3.9 | — | 4.5 | V | |
| Input Voltage to Turn-on Output | $V_{ON}$ | 5.25 | — | 6.0 | V | |
| **Voltage Regulator - 3.3V** | | | | | | |
| Output Voltage | $V_{REG}$ | 3.20 | 3.30 | 3.40 | V | 0 mA < $I_{OUT}$ < 70 mA |
| Line Regulation | $\Delta V_{OUT}1$ | — | 10 | 50 | mV | $I_{OUT}$ = 1 mA,<br>6.0V < $V_{BB}$ < 18V |
| Load Regulation | $\Delta V_{OUT}2$ | — | 10 | 50 | mV | 5 mA < $I_{OUT}$ < 70 mA,<br>6.0V < $V_{BB}$ < 12V |
| Power Supply Ripple Reject | PSRR | — | 50 | — | dB | 1 $V_{PP}$ @10-20 kHz ,<br>$I_{LOAD}$ = 20 mA |
| Output Noise Voltage | eN | — | — | 100 | µ$V_{RMS}$ /$\sqrt{Hz}$ | 10 Hz – 40 MHz<br>$C_{FILTER}$ = 10 µF,<br>$C_{BP}$ = 0.1 µF, $I_{LOAD}$= 20 mA |
| Shutdown Voltage | $V_{SD}$ | 2.5 | — | 2.7 | V | See Figure 1-7 (Note 2) |
| Input Voltage to Turn-off Output | $V_{OFF}$ | 3.9 | — | 4.5 | V | |
| Input Voltage to Turn-on Output | $V_{ON}$ | 5.25 | — | 6 | V | |

**FIGURE 2-1: ESR CURVES FOR LOAD CAPACITOR SELECTION**



## 2.4 AC Specification

| AC CHARACTERISTICS | $V_{BB}$ = 6.0V to 18.0V; $T_A$ = -40°C to +125°C | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Sym.** | **Min.** | **Typ.** | **Max.** | **Units** | **Test Conditions** |
| **Bus Interface - Constant Slope Time Parameters (DC specifications are for a $V_{BB}$ range of 6.0 to 18.0V)** | | | | | | |
| Slope rising and falling edges | $t_{SLOPE}$ | 3.5 | — | 22.5 | µs | 7.3V <= $V_{BB}$ <= 18V |
| Propagation Delay of Transmitter | $t_{TRANSPD}$ | — | — | 6.0 | µs | $t_{TRANSPD}$ = max ($t_{TRANSPDR}$ or $t_{TRANSPDF}$) |
| Propagation Delay of Receiver | $t_{RECPD}$ | — | — | 6.0 | µs | $t_{RECPD}$ = max ($t_{RECPDR}$ or $t_{RECPDF}$) |
| Symmetry of Propagation Delay of Receiver rising edge w.r.t. falling edge | $t_{RECSYM}$ | -2.0 | — | 2.0 | µs | trecsym = max (trecpdf – trecpdr)<br>$R_{RXD}$ 2.4KΩ to $V_{CC}$, $C_{RXD}$ 20pF |
| Symmetry of Propagation Delay of Transmitter rising edge w.r.t. falling edge | $t_{TRANSSYM}$ | -2.0 | — | 2.0 | µs | $t_{TRANSSYM}$ = max ($t_{TRANSPDF}$ - $t_{TRANSPDR}$) |
| Bus dominant time-out time | $t_{TO(LIN)}$ | — | 25 | — | mS | |
| Duty Cycle 1 @20.0 kbit/sec | | .396 | — | — | %$t_{BIT}$ | $C_{BUS}$;$R_{BUS}$ conditions:<br>1 nF; 1 kΩ \| 6.8 nF; 660Ω \| 10 nF; 500Ω<br>$TH_{REC(MAX)}$ = 0.744 x $V_{BB}$,<br>$TH_{DOM(MAX)}$ = 0.581 x $V_{BB}$,<br>$V_{BB}$ =7.0V - 18V; $t_{BIT}$ = 50 µs.<br>D1 = $t_{BUS\_REC(MIN)}$ / 2 x $t_{BIT}$) |
| Duty Cycle 2 @20.0 kbit/sec | | — | — | .581 | %$t_{BIT}$ | $C_{BUS}$;$R_{BUS}$ conditions:<br>1 nF; 1 kΩ \| 6.8 nF; 660Ω \| 10 nF; 500Ω<br>$TH_{REC(MAX)}$ = 0.284 x $V_{BB}$,<br>$TH_{DOM(MAX)}$ = 0.422 x $V_{BB}$,<br>$V_{BB}$ =7.6V - 18V; $t_{BIT}$ = 50 µs.<br>D2 = $t_{BUS\_REC(MAX)}$ / 2 x $t_{BIT}$) |
| Duty Cycle 3 @10.4 kbit/sec | | .417 | — | — | %$t_{BIT}$ | $C_{BUS}$;$R_{BUS}$ conditions:<br>1 nF; 1 kΩ \| 6.8 nF; 660Ω \| 10 nF; 500Ω<br>$TH_{REC(MAX)}$ = 0.778 x $V_{BB}$,<br>$TH_{DOM(MAX)}$ = 0.616 x $V_{BB}$,<br>$V_{BB}$ =7.0V - 18V; $t_{BIT}$ = 96 µs.<br>D3 = $t_{BUS\_REC(MIN)}$ / 2 x $t_{BIT}$) |
| Duty Cycle 4 @10.4 kbit/sec | | — | — | .590 | %$t_{BIT}$ | $C_{BUS}$;$R_{BUS}$ conditions:<br>1 nF; 1 kΩ \| 6.8 nF; 660Ω \| 10 nF; 500Ω<br>$TH_{REC(MAX)}$ = 0.251 x $V_{BB}$,<br>$TH_{DOM(MAX)}$ = 0.389 x $V_{BB}$,<br>$V_{BB}$ =7.6V - 18V; $t_{BIT}$ = 96 µs.<br>D4 = $t_{BUS\_REC(MAX)}$ / 2 x $t_{BIT}$) |

**Note 1:** Time depends on external capacitance and load. Test condition: $C_{REG}$ = 4.7uF, no resistor load.

**2:** For design guidance only, not tested.

## 2.4 AC Specification (Continued)

| AC CHARACTERISTICS | $V_{BB}$ = 6.0V to 18.0V; $T_A$ = -40°C to +125°C | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Sym.** | **Min.** | **Typ.** | **Max.** | **Units** | **Test Conditions** |
| **Voltage Regulator** | | | | | | |
| Bus Activity Debounce time | $t_{BDB}$ | 30 | 80 | 250 | µs | |
| Bus Activity to Voltage Regulator Enabled | $t_{BACTIVE}$ | 35 | — | 200 | µs | |
| Voltage Regulator Enabled to Ready | $t_{VEVR}$ | 300 | — | 1200 | µs | **(Note 1)** |
| Chip Select to Ready Mode | tCSR | — | — | 230 | µs | **(Note 2)** |
| Chip Select to Power-down | tCSPD | — | — | 300 | µs | **(Note 2)** |
| Short circuit to shut-down | tSHUTDOWN | 20 | — | 100 | µs | |
| **$\overline{\text{RESET}}$ Timing** | | | | | | |
| $V_{REG}$ OK detect to $\overline{\text{RESET}}$ inactive | tRPU | — | — | 60.0 | µs | **(Note 2)** |
| $V_{REG}$ not OK detect to $\overline{\text{RESET}}$ active | tRPD | — | — | 60.0 | µs | **(Note 2)** |

**Note 1:** Time depends on external capacitance and load. Test condition: $C_{REG}$ = 4.7uF, no resistor load.

**2:** For design guidance only, not tested.

## 2.5 Thermal Specifications

| THERMAL CHARACTERISTICS | | | | | |
|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Typ.** | **Max.** | **Units** | **Test Conditions** |
| Recovery Temperature | θRECOVERY | +140 | — | °C | |
| Shutdown Temperature | θSHUTDOWN | +150 | — | °C | |
| Short Circuit Recovery Time | tTHERM | 1.5 | 5.0 | ms | |
| **Thermal Package Resistances** | | | | | |
| Thermal Resistance, 8-PDIP | θJA | 89.3 | — | °C/W | |
| Thermal Resistance, 8-SOIC | θJA | 149.5 | — | °C/W | |
| Thermal Resistance, 8-QFN | θJA | 48.0 | — | °C/W | |

**Note 1:** The maximum power dissipation is a function of $T_{JMAX}$, ΘJA and ambient temperature $T_A$. The maximum allowable power dissipation at an ambient temperature is $P_D = (T_{JMAX} - T_A)$ ΘJA. If this dissipation is exceeded, the die temperature will rise above 150°C and the MCP2025 will go into thermal shutdown.

## 2.6 Timing Diagrams and Specifications

**FIGURE 2-2: BUS TIMING DIAGRAM**

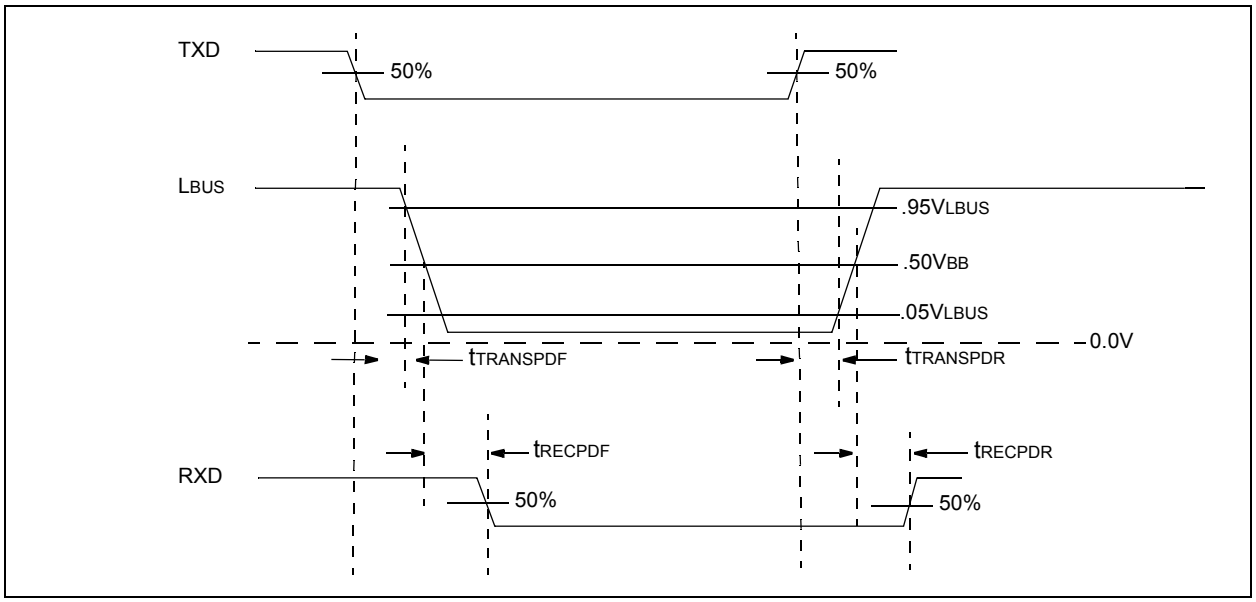



**FIGURE 2-3: REGULATOR BUS WAKE TIMING DIAGRAM**

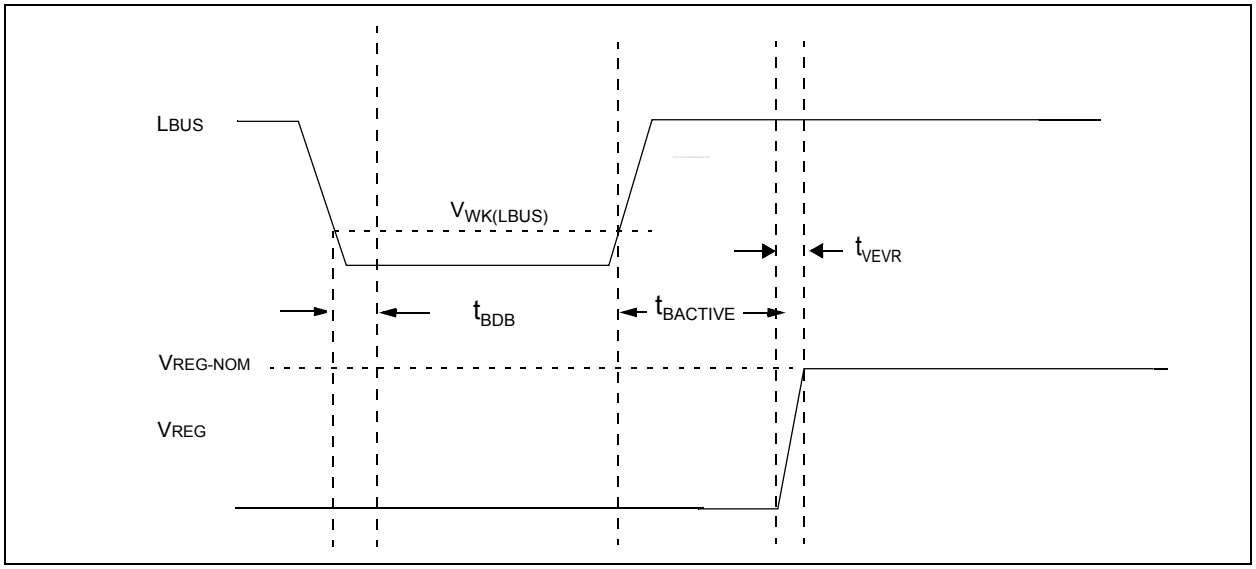


**FIGURE 2-4: CS/LWAKE, REGULATOR AND $\overline{\text{RESET}}$ TIMING DIAGRAM**

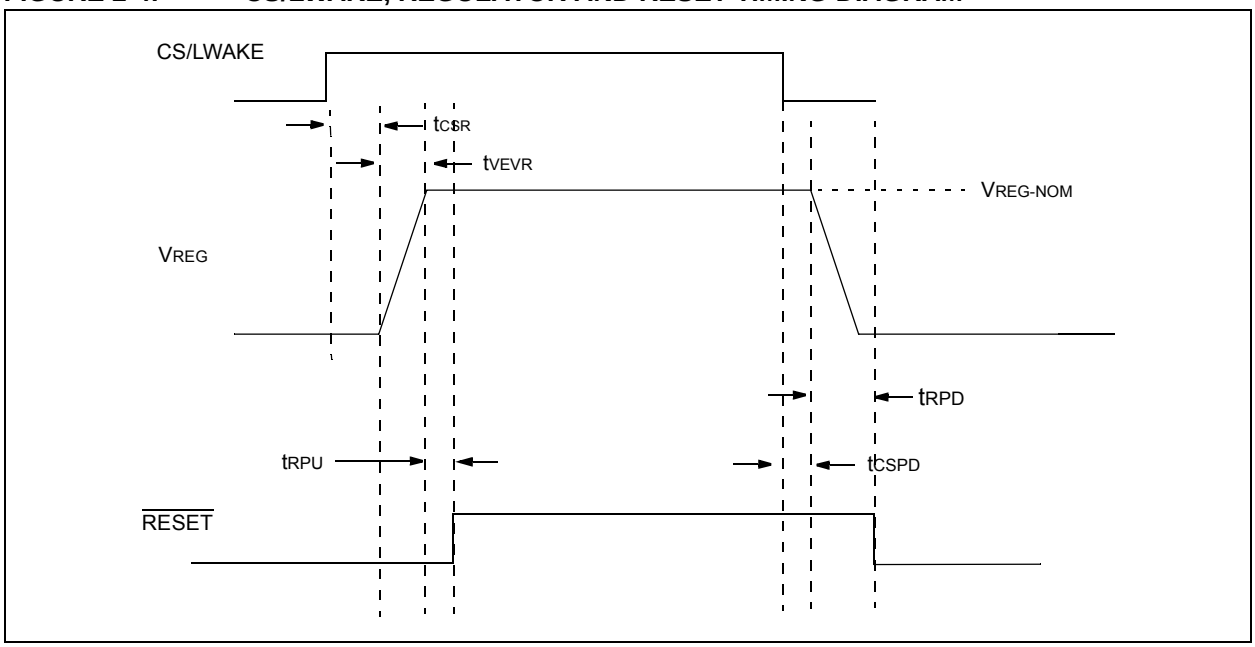



**FIGURE 2-5: TYPICAL $I_{BBQ}$ VS. TEMPERATURE - 5.0V**

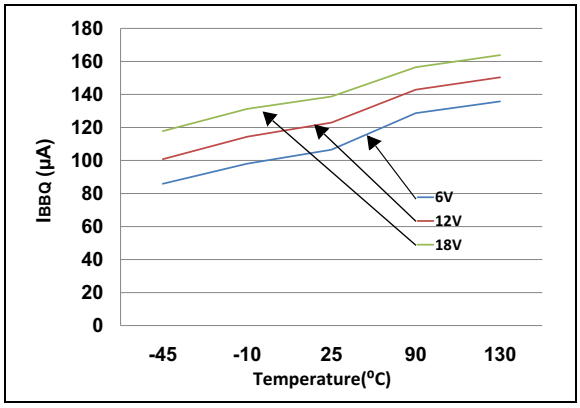



**FIGURE 2-6: $I_{BBQ}$ TRANS-OFF VS. TEMPERATURE - 5.0V**

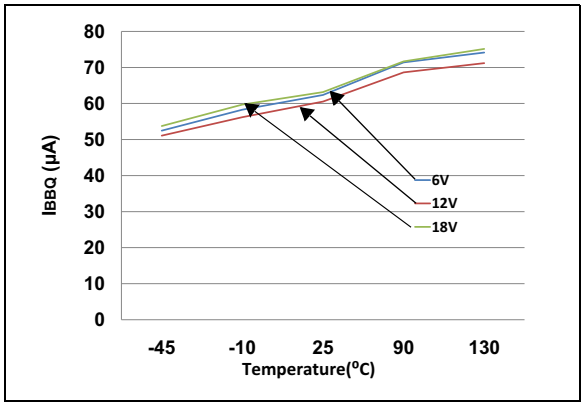



**FIGURE 2-7: $I_{BBQ}$ POWER-DOWN VS. TEMPERATURE - 5.0V**

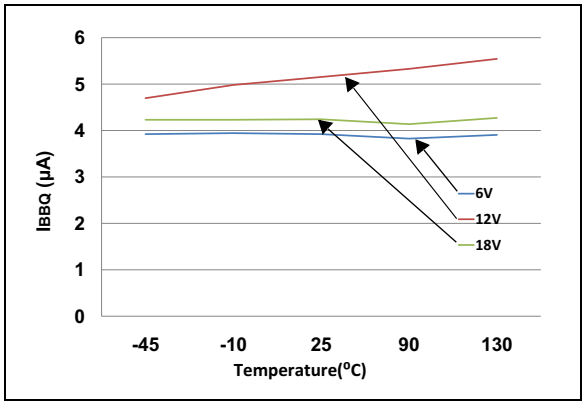


**FIGURE 2-8: TYPICAL $I_{BBQ}$ VS. TEMPERATURE - 3.3V**

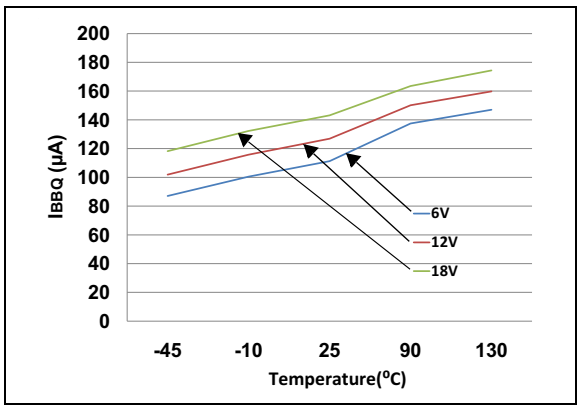



**FIGURE 2-9: $I_{BBQ}$ TRANS-OFF VS. TEMPERATURE - 3.3V**

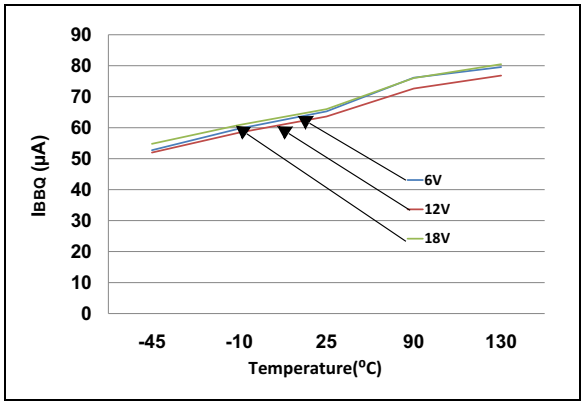
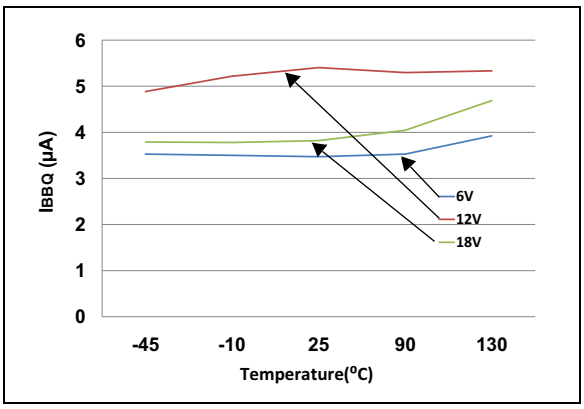


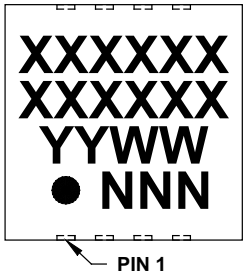

**FIGURE 2-10: $I_{BBQ}$ POWER-DOWN VS. TEMPERATURE - 3.3V**



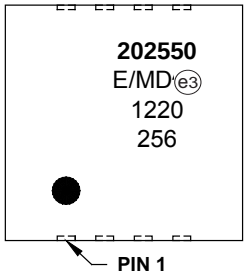
## 3.0 PACKAGING INFORMATION

### 3.1 Package Marking Information

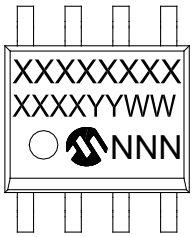
8-Lead DFN (4x4x0.9 mm)



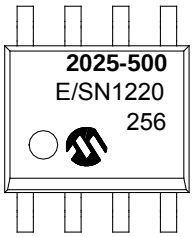

Example



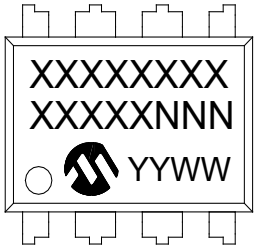

8-Lead SOIC (150 mil)



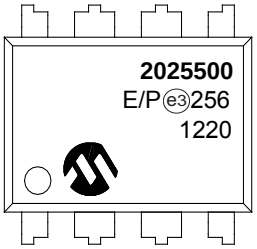

Example:




8-Lead PDIP (300 mil)




Example

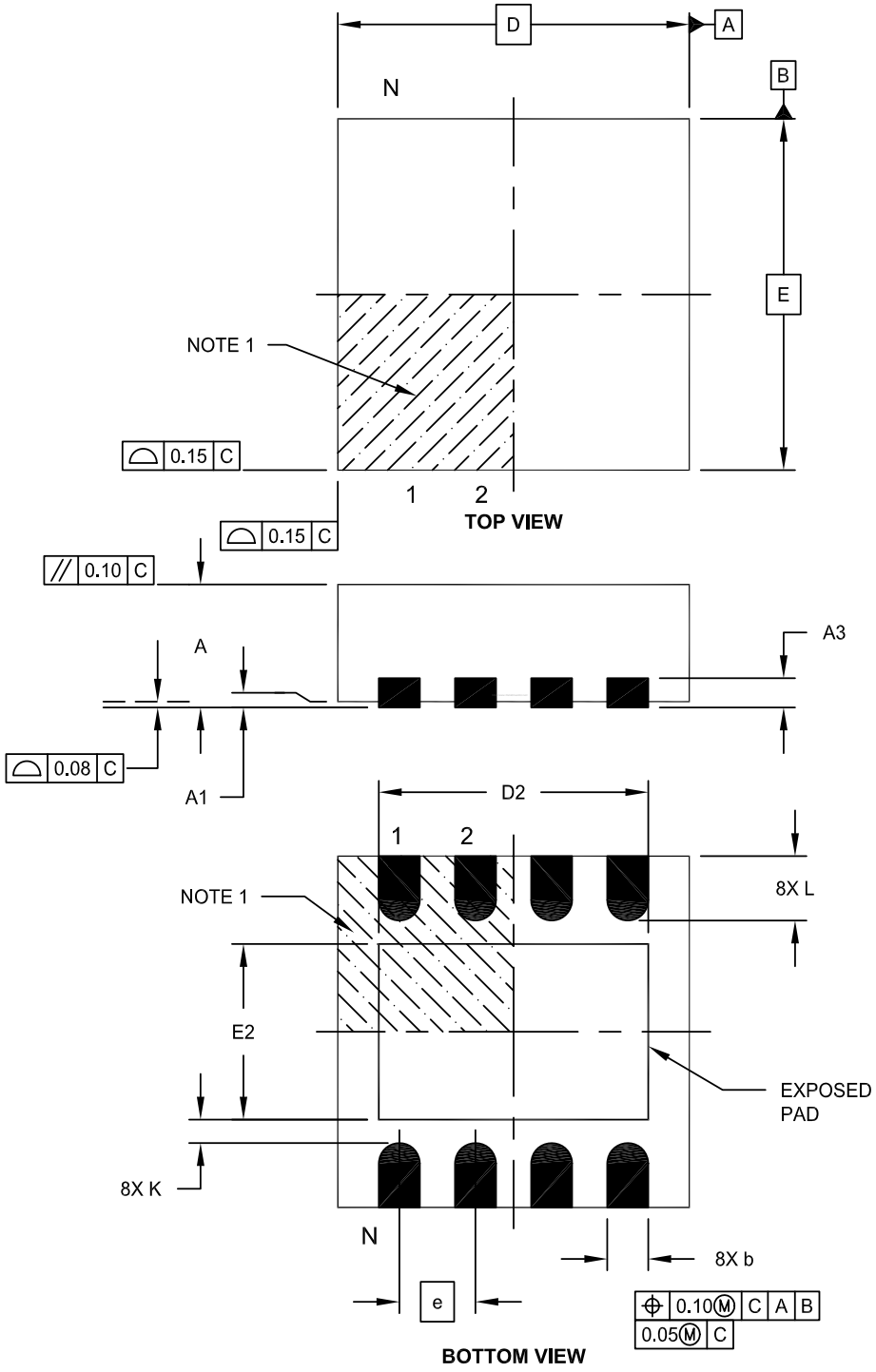



| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

## 8-Lead Plastic Dual Flat, No Lead Package (MD) – 4x4x0.9 mm Body [DFN]

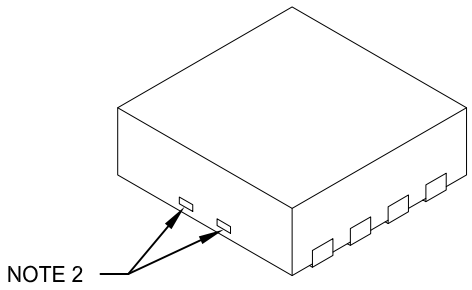
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing C04-131E Sheet 1 of 2

## 8-Lead Plastic Dual Flat, No Lead Package (MD) – 4x4x0.9 mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 0.80 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | | 0.20 REF | |
| Overall Length | D | | 4.00 BSC | |
| Exposed Pad Width | E2 | 2.60 | 2.70 | 2.80 |
| Overall Width | E | | 4.00 BSC | |
| Exposed Pad Length | D2 | 3.40 | 3.50 | 3.60 |
| Contact Width | b | 0.25 | 0.30 | 0.35 |
| Contact Length | L | 0.30 | 0.40 | 0.50 |
| Contact-to-Exposed Pad | K | 0.20 | - | - |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

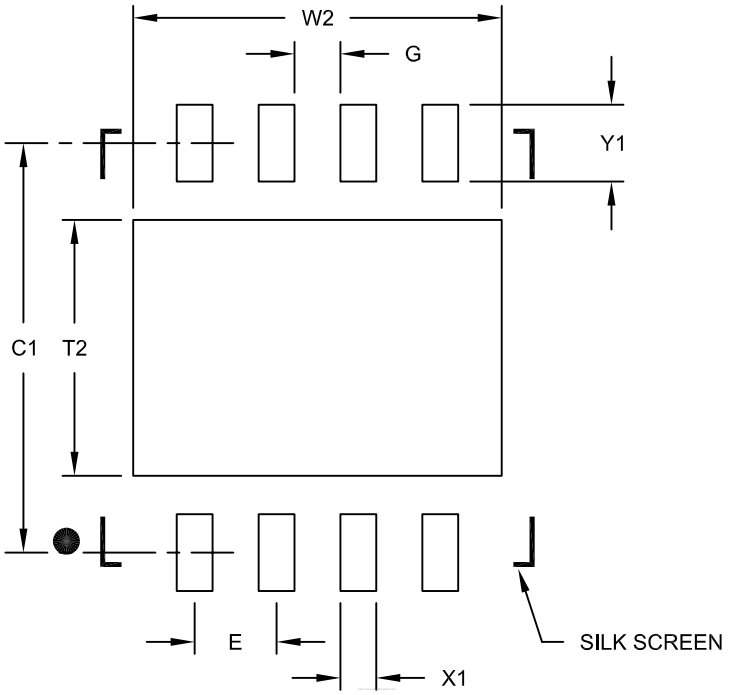
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-131E Sheet 2 of 2

8-Lead Plastic Dual Flat, No Lead Package (MD) - 4x4x0.9 mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.80 BSC | |
| Optional Center Pad Width | W2 | | | 3.60 |
| Optional Center Pad Length | T2 | | | 2.50 |
| Contact Pad Spacing | C1 | | 4.00 | |
| Contact Pad Width (X8) | X1 | | | 0.35 |
| Contact Pad Length (X8) | Y1 | | | 0.75 |
| Distance Between Pads | G | 0.45 | | |

Notes:

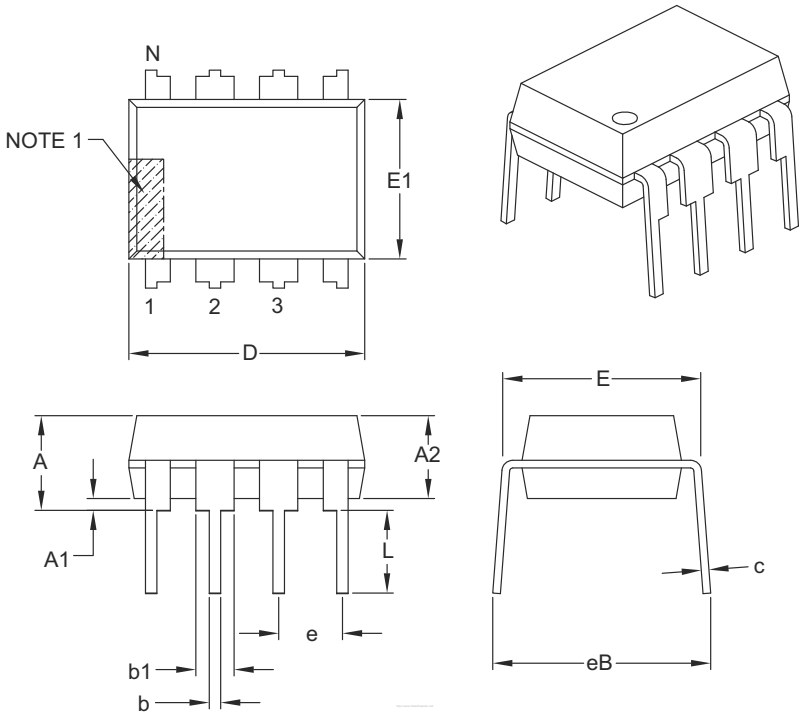
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2131C

## 8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | .100 BSC | |
| Top to Seating Plane | A | – | – | .210 |
| Molded Package Thickness | A2 | .115 | .130 | .195 |
| Base to Seating Plane | A1 | .015 | – | – |
| Shoulder to Shoulder Width | E | .290 | .310 | .325 |
| Molded Package Width | E1 | .240 | .250 | .280 |
| Overall Length | D | .348 | .365 | .400 |
| Tip to Seating Plane | L | .115 | .130 | .150 |
| Lead Thickness | c | .008 | .010 | .015 |
| Upper Lead Width | b1 | .040 | .060 | .070 |
| Lower Lead Width | b | .014 | .018 | .022 |
| Overall Row Spacing § | eB | – | – | .430 |

**Notes:**

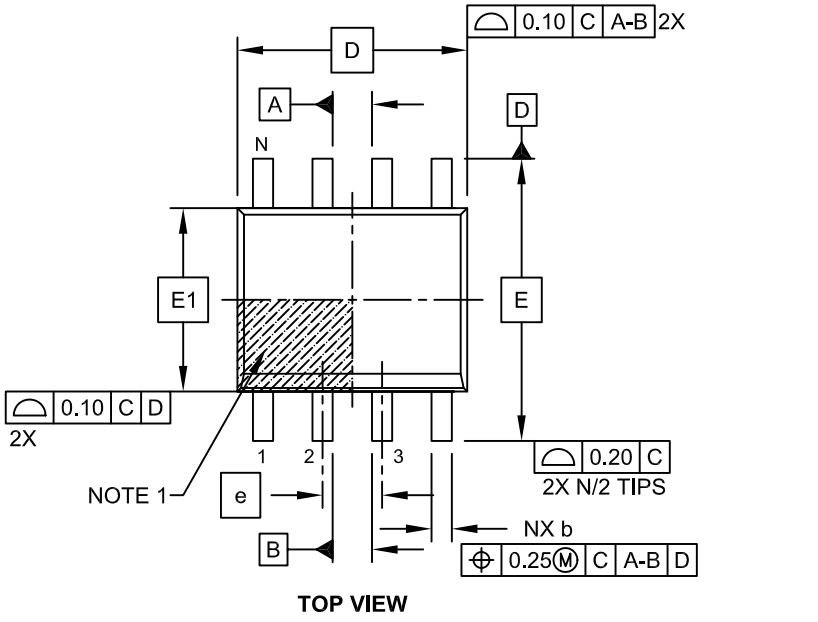
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

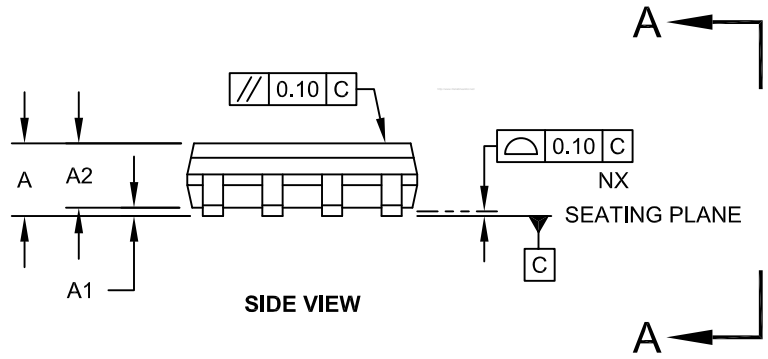
Microchip Technology Drawing C04-018B

### 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

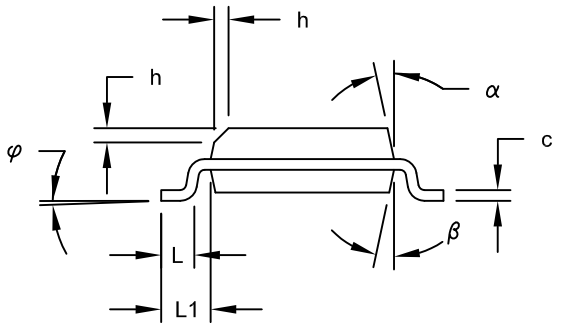
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




TOP VIEW




SIDE VIEW

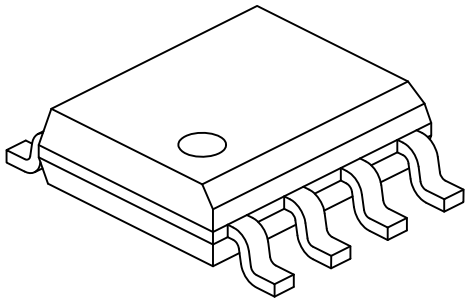



VIEW A-A

Microchip Technology Drawing No. C04-057C Sheet 1 of 2

## 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 1.27 BSC | |
| Overall Height | A | - | - | 1.75 |
| Molded Package Thickness | A2 | 1.25 | - | - |
| Standoff § | A1 | 0.10 | - | 0.25 |
| Overall Width | E | | 6.00 BSC | |
| Molded Package Width | E1 | | 3.90 BSC | |
| Overall Length | D | | 4.90 BSC | |
| Chamfer (Optional) | h | 0.25 | - | 0.50 |
| Foot Length | L | 0.40 | - | 1.27 |
| Footprint | L1 | | 1.04 REF | |
| Foot Angle | φ | 0° | - | 8° |
| Lead Thickness | c | 0.17 | - | 0.25 |
| Lead Width | b | 0.31 | - | 0.51 |
| Mold Draft Angle Top | α | 5° | - | 15° |
| Mold Draft Angle Bottom | β | 5° | - | 15° |

**Notes:**

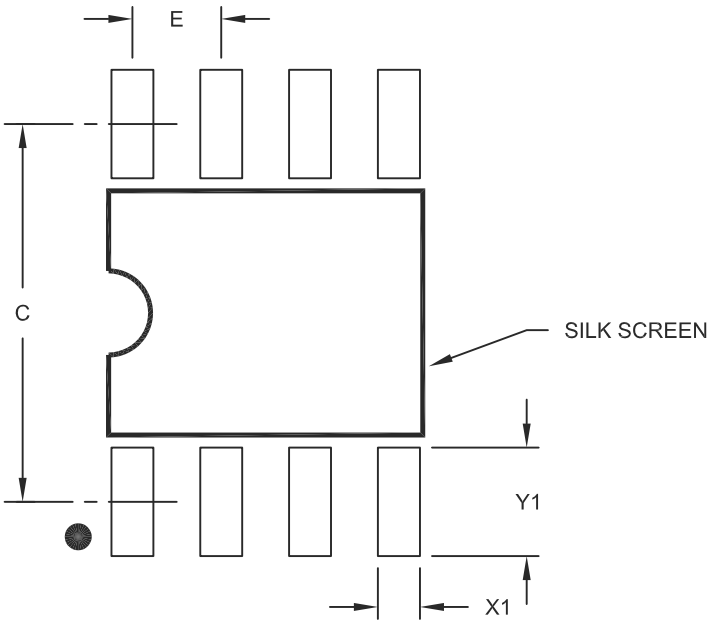
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

### 8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 1.27 BSC | |
| Contact Pad Spacing | C | | 5.40 | |
| Contact Pad Width (X8) | X1 | | | 0.60 |
| Contact Pad Length (X8) | Y1 | | | 1.55 |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

# APPENDIX A: REVISION HISTORY

## Revision A (June 2012)

- Original Release of this Document.

**NOTES:**

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | –X | /XX |
|---|---|---|
| Device | Temperature Range | Package |

| | | |
|---|---|---|
| Device: | MCP2025: | LIN Transceiver with Voltage Regulator |
| | MCP2025T: | LIN Transceiver with Voltage Regulator (Tape and Reel) (SOIC and DFN only) |
| Temperature Range: | E = | -40°C to +125°C |
| Package: | P = | Plastic DIP (300 mil Body), 8-lead |
| | SN = | Plastic Small Outline SOIC, 8-lead |
| | MD = | Plastic Dual Flat DFN, 8-lead |

**Examples:**

a) MCP2025-330E/SN: 3.3V, 8L-SOIC package
b) MCP2025-330E/P: 3.3V, 8L-PDIP package
c) MCP2025-330E/MD: 3.3V, 8L-DFN package
d) MCP2025-500E/SN: 5.0V, 8L-SOIC package
e) MCP2025-500E/P: 5.0V, 8L-PDIP package
f) MCP2025-500E/MD: 5.0V, 8L-DFN package
g) MCP2025T-330E/SN: Tape and Reel, 3.3V, 8L-SOIC package
h) MCP2025T-500E/SN: Tape and Reel, 5.0V, 8L-SOIC package
i) MCP2025T-330E/MD: Tape and Reel, 3.3V, 8L-DFN package
j) MCP2025T-500E/MD: Tape and Reel, 5.0V, 8L-DFN package

**NOTES:**

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- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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