EVB72011

433MHz FSK Transmitter
Evaluation Board Description

General Description

The TH72011 evaluation board is designed to demonstrate the optimal performance of the transmitter IC in a 50Ohm environment with the minimum of external components. The TH72011
board is populated for FSK transmission. The power amplifier is optimally matched to 50 Ohm by means of an antenna matching network for the resonant frequency of 433 MHz.

Board layout data in Gerber format is available on request.

Features

- ❑ Fully integrated PLL-stabilized VCO
- ❑ Frequency range from 380 MHz to 450 MHz
- ❑ Single-ended RF output
- ❑ FSK through crystal pulling allows modulation from DC to 40 kbit/s
- ❑ High FSK deviation possible for wideband data transmission
- ❑ Wide power supply range from 1.9 V to 5.5 V
- ❑ Low voltage detector
- ❑ High over-all frequency accuracy
- ❑ FSK deviation and center frequency independently adjustable
- ❑ Very low standby current
- ❑ Adjustable output power range from -15 dBm to +6 dBm
- ❑ Adjustable current consumption from 3.5 mA to 10.7 mA
- ❑ Conforms to EN 300 220 and similar standards

Ordering Information

Part No.

EVB72011-433

Applications

- ❑ General digital data transmission
- ❑ Tire Pressure Monitoring System(TPMS)
- ❑ Remote Keyless Entry (RKE)
- ❑ Low-power telemetry
- ❑ Alarm and security systems
- ❑ Garage door openers
- ❑ Home automation
- ❑ Remote controls
- ❑ Local oscillator signal generation

Document Content

1 Theory of Operation

1.1 General

As depicted in Fig.1, the TH72011 transmitter consists of a fully integrated voltage-controlled oscillator (VCO), a divide-by-32 divider (div32), a phase-frequency detector (PFD) and a charge pump (CP). An internal loop filter determines the dynamic behavior of the PLL and suppresses reference spurious signals. A Colpitts crystal oscillator (XOSC) is used as the reference oscillator of a phase-locked loop (PLL) synthesizer. The VCO's output signal feeds the power amplifier (PA). RF signal power P_{out} can be adjusted in four steps from P_{out} = –15 dBm to +6 dBm, either by changing the value of resistor RPS or by varying the voltage V_{PS} at pin PSEL. The open-collector output (OUT) can be used either to directly drive a loop antenna or to be matched to a 50Ohm load. Bandgap biasing ensures stable operation of the IC at a power supply range of 1.9 V to 5.5 V.

1.2 Block Diagram

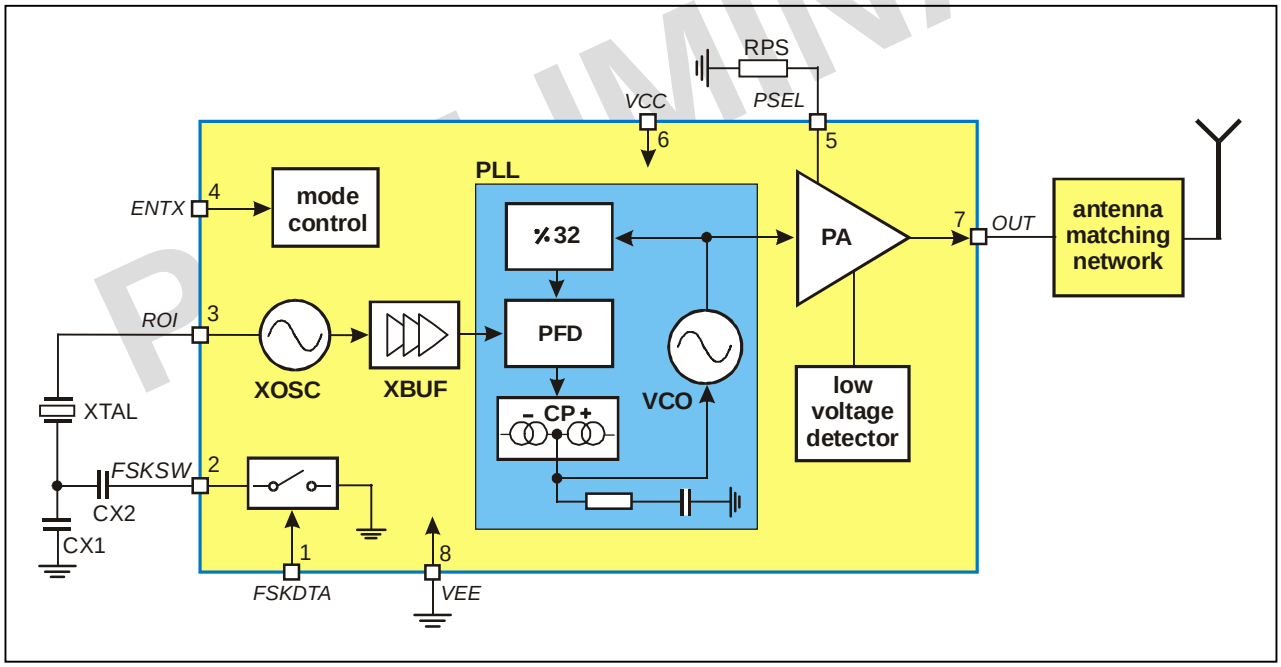


Fig. 1: Block diagram with external components

2 Functional Description

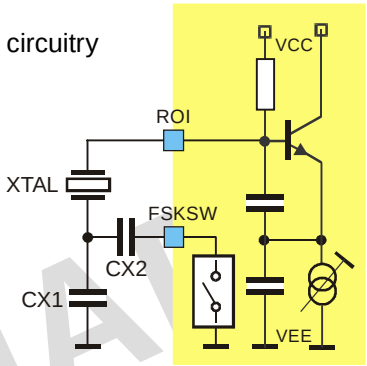
2.1 Crystal Oscillator

A Colpitts crystal oscillator with integrated functional capacitors is used as the reference oscillator for the PLL synthesizer. The equivalent input capacitance CRO offered by the crystal oscillator input pin ROI is about 18pF. The crystal oscillator is provided with an amplitude control loop in order to have a very stable frequency over the specified supply voltage and temperature range in combination with a short start-up time.

2.2 FSK Modulation

FSK modulation can be achieved by pulling the crystal oscillator frequency. A CMOS-compatible data stream applied at the pin FSKDTA digitally modulates the XOSC via an integrated NMOS switch. Two external pulling capacitors CX1 and CX2 allow the FSK deviation Δf and the center frequency f_c to be adjusted independently. At FSKDTA = 0, CX2 is connected in parallel to CX1 leading to the low-frequency component of the FSK spectrum (f_{min}); while at FSKDTA = 1, CX2 is deactivated and the XOSC is set to its high frequency f_{max}.
An external reference signal can be directly AC-coupled to the reference oscillator input pin ROI. Then the transmitter is used without a crystal. Now the reference signal sets the carrier frequency and may also contain the FSK (or FM) modulation.

Fig. 2: Crystal pulling circuitry



FSKDTA	Description
0	$f_{min}= f_c - \Delta f$ (FSK switch is closed)
1	$f_{max}= f_c + \Delta f$ (FSK switch is open)

2.3 Crystal Pulling

A crystal is tuned by the manufacturer to the required oscillation frequency f_0 at a given load capacitance CL and within the specified calibration tolerance. The only way to pull the oscillation frequency is to vary the effective load capacitance CL_{eff} seen by the crystal.
Figure 3 shows the oscillation frequency of a crystal as a function of the effective load capacitance. This capacitance changes in accordance with the logic level of FSKDTA around the specified load capacitance. The figure illustrates the relationship between the external pulling capacitors and the frequency deviation.
It can also be seen that the pulling sensitivity increases with the reduction of CL. Therefore, applications with a high frequency deviation require a low load capacitance. For narrow band FSK applications, a higher load capacitance could be chosen in order to reduce the frequency drift caused by the tolerances of the chip and the external pulling capacitors.

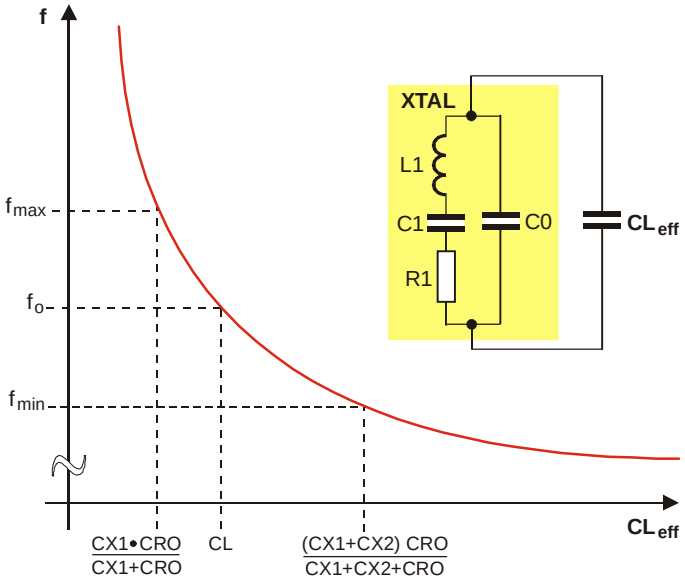


Fig. 3: Crystal pulling characteristic

2.4 Output Power Selection

The transmitter is provided with an output power selection feature. There are four predefined output power steps and one off-step accessible via the power selection pin PSEL. A digital power step adjustment was chosen because of its high accuracy and stability. The number of steps and the step sizes as well as the corresponding power levels are selected to cover a wide spectrum of different applications.

The implementation of the output power control logic is shown in figure 4. There are two matched current sources with an amount of about 8 µA. One current source is directly applied to the PSEL pin. The other current source is used for the generation of reference voltages with a resistor ladder. These reference voltages are defining the thresholds between the power steps. The four comparators deliver thermometer-coded control signals depending on the voltage level at the pin PSEL. In order to have a certain amount of ripple tolerance in a noisy environment the comparators are provided with a little hysteresis of about 20 mV. With these control signals, weighted current sources of the power amplifier are switched on or off to set the desired output power level (Digitally Controlled Current Source). The LOCK signal and the output of the low voltage detector are gating this current source.

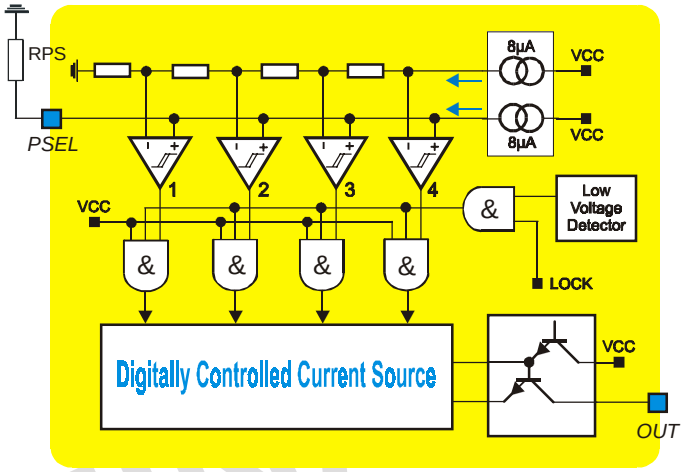


Fig. 4: Block diagram of output power control circuitry

There are two ways to select the desired output power step. First by applying a DC voltage at the pin PSEL, then this voltage directly selects the desired output power step. This kind of power selection can be used if the transmission power must be changed during operation. For a fixed-power application a resistor can be used which is connected from the PSEL pin to ground. The voltage drop across this resistor selects the desired output power level. For fixed-power applications at the highest power step this resistor can be omitted. The pin PSEL is in a high impedance state during the “TX standby” mode.

typical values at T_A = 23 °C and $V_{CC} \geq 4$ V

Power step	0	1	2	3	4
P_{out} / dBm	< -70	-15	-6	0	6
RPS / kΩ	< 10	22	47	100	> 220
V_{PS} / V	0.1	0.14 to 0.24	0.28 to 0.51	0.57 to 1.18	> 1.23

2.5 Lock Detection

The lock detection circuitry turns on the power amplifier only after PLL lock. This prevents from unwanted emission of the transmitter if the PLL is unlocked.

2.6 Low Voltage Detection

The supply voltage is sensed by a low voltage detect circuitry. The power amplifier is turned off if the supply voltage drops below a value of about 1.85 V. This is done in order to prevent unwanted emission of the transmitter if the supply voltage is too low.

2.7 Mode Control Logic

The mode control logic allows two different modes of operation as listed in the following table. The mode control pin ENTX is pulled-down internally. This guarantees that the whole circuit is shut down if this pin is left floating.

ENTX	Mode	Description
0	TX standby	TX disabled
1	TX active	TX enable

2.8 Timing Diagrams

After enabling the transmitter by the ENTX signal, the power amplifier remains inactive for the time t_{on}, the transmitter start-up time. The crystal oscillator starts oscillation and the PLL locks to the desired output frequency within the time duration t_{on}. After successful PLL lock, the LOCK signal turns on the power amplifier, and then the RF carrier can be FSK modulated.

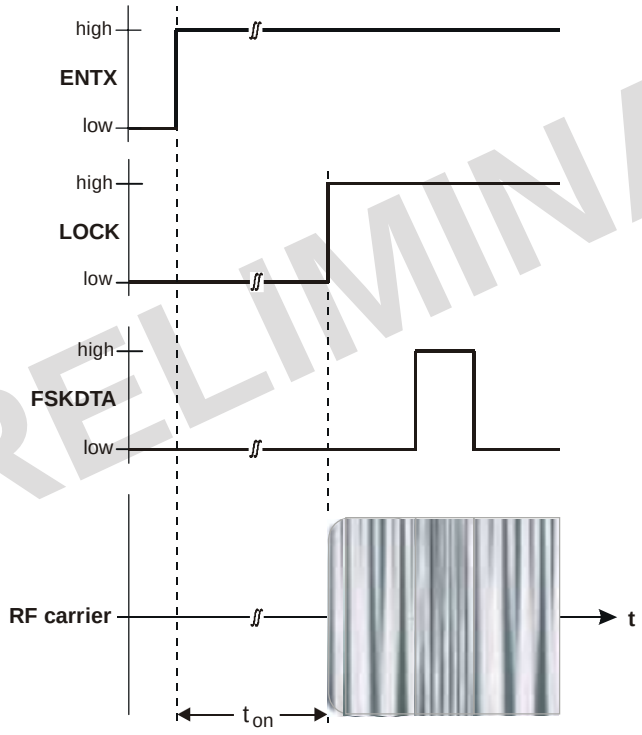


Fig. 5: Timing diagram for FSK modulation

For more detailed information, please refer to the latest TH72011 data sheet revision.

3 Circuit Diagram

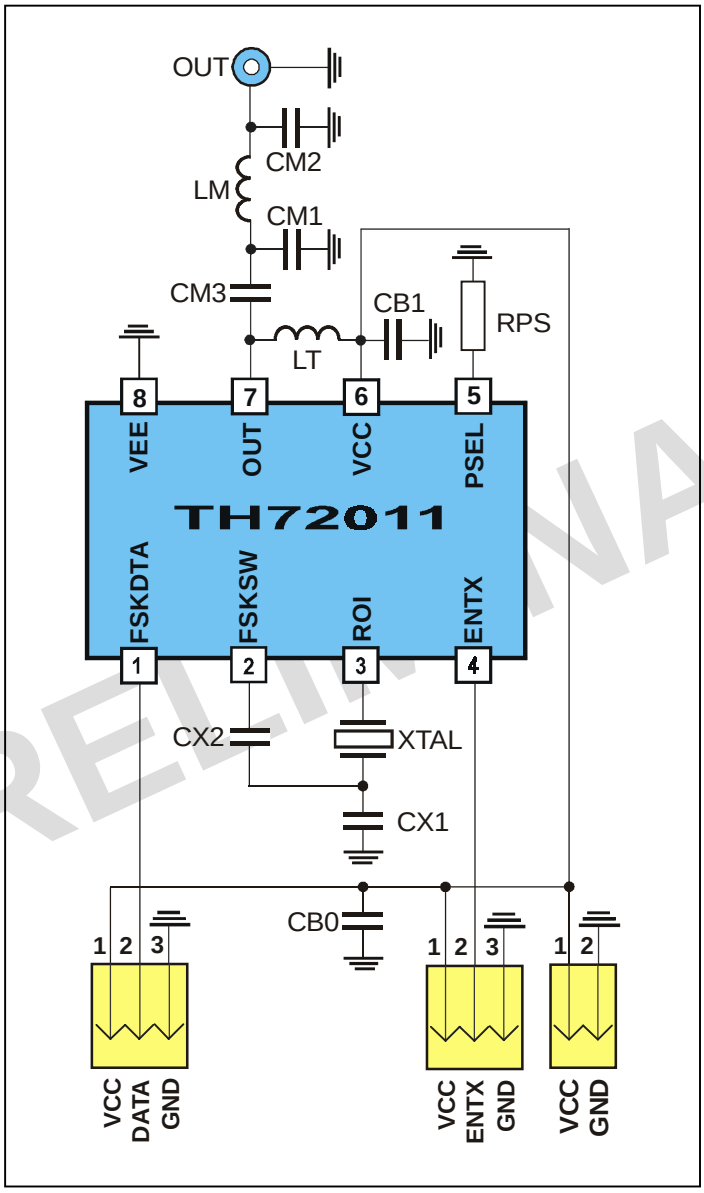
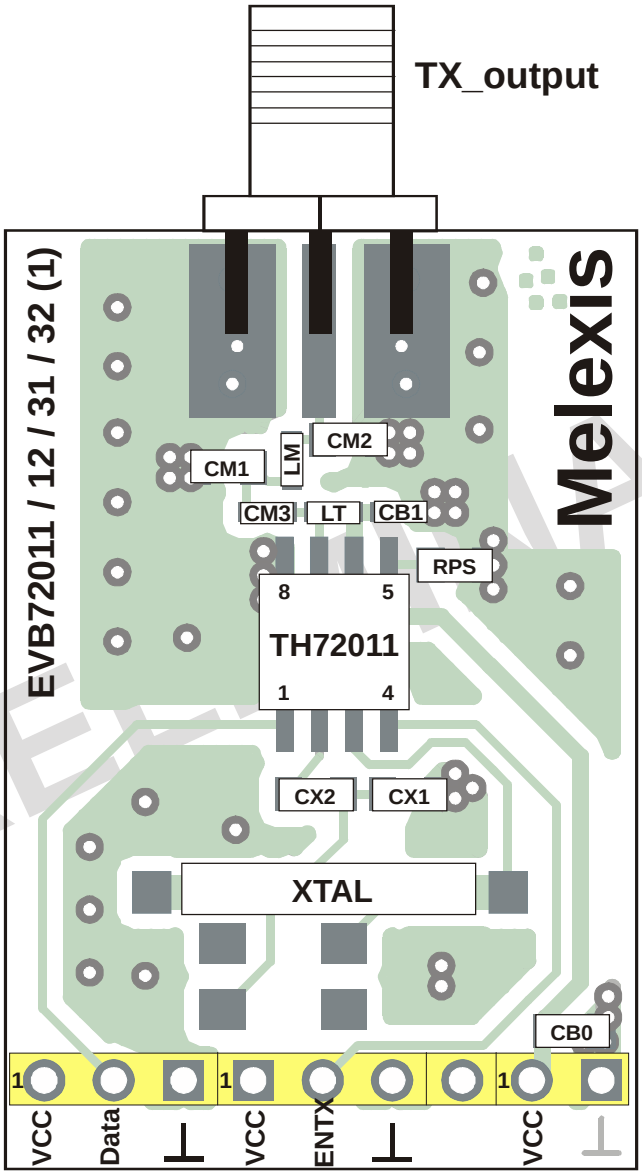


Fig. 6: Circuit diagram for FSK with 50 Ω matching network

4 PCB Top View



Board size is 23 mm x 34 mm

4.1 Board Connection

VCC	Power supply (1.9 V to 5.5 V)	**ENTX**	Mode control pin (see para. 2.4)
DATA	Input for FSK data (CMOS, see para. 2.2)	**GND**	Several ground pins

5 Board Component Values

Part	Size	Value @ 433.92 MHz	Tolerance	Description
*CX1	0805	27 pF	±5%	XOSC capacitor (Δf = ±20 kHz)
*CX2	0805	150 pF	±5%	XOSC capacitor (Δf = ±20 kHz)
CM1	0805	5.6 pF	±5%	impedance matching capacitor
CM2	0805	12 pF	±5%	impedance matching capacitor
CM3	0603	680 pF	±5%	impedance matching capacitor
CB0	0805	1 nF	±10%	blocking capacitor
CB1	0603	330 pF	±10%	blocking capacitor
LT	0603	39 nH	±5%	output tank inductor
LM	0603	33 nH	±5%	impedance matching inductor
RPS	0805	see para. 2.4	±10%	power-select resistor
XTAL	HC49/S	13.5600 MHz fundamental wave	±30ppm calibration ±30ppm temp.	crystal, C_L = 12 pF, $C_{0,\,max}$ = 7 pF, R_1 = 60 Ω

***Notes:** Value depends on crystal parameters

Your Notes

6 Package Information

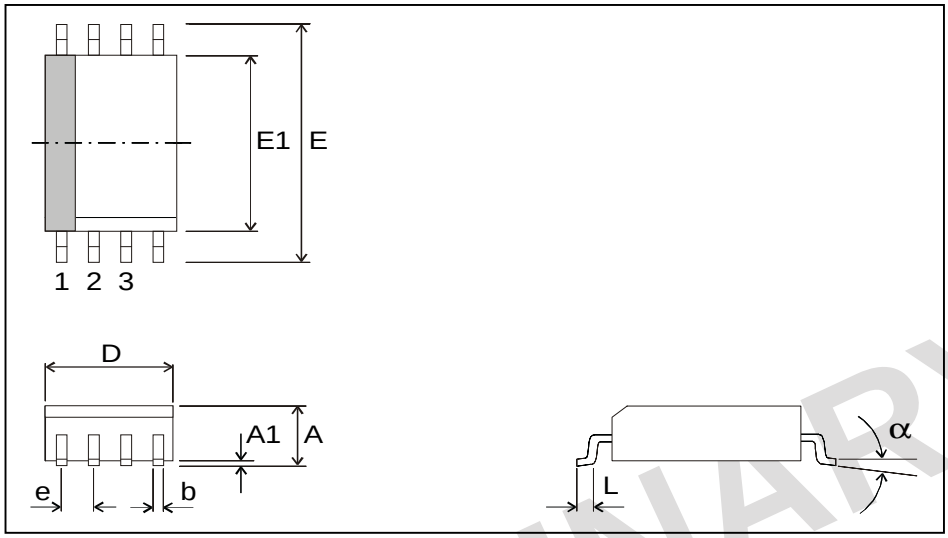


Fig. 7: SOIC8 (Shrink Small Outline Package)

all Dimension in mm, coplanarity < 0.1mm									
	D	**E1**	**E**	**A**	**A1**	**e**	**b**	**L**	**α**
min	4.80	3.81	5.80	1.32	0.10	1.27	0.36	0.41	0°
max	4.98	3.99	6.20	1.72	0.25		0.46	1.27	8°
all Dimension in inch, coplanarity < 0.004”									
min	0.189	0.150	0.2284	0.060	0.0040	0.05	0.014	0.016	0°
max	0.196	0.157	0.2440	0.068	0.0098		0.018	0.050	8°

Your Notes

7 Disclaimer

Devices sold by Melexis are covered by the warranty and patent indemnification provisions appearing in its Term of Sale. Melexis makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. Melexis reserves the right to change specifications and prices at any time and without notice. Therefore, prior to designing this product into a system, it is necessary to check with Melexis for current information. This product is intended for use in normal commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life-sustaining equipment are specifically not recommended without additional processing by Melexis for each application.

The information furnished by Melexis is believed to be correct and accurate. However, Melexis shall not be liable to recipient or any third party for any damages, including but not limited to personal injury, property damage, loss of profits, loss of use, interrupt of business or indirect, special incidental or consequential damages, of any kind, in connection with or arising out of the furnishing, performance or use of the technical data herein. No obligation or liability to recipient or any third party shall arise or flow out of Melexis' rendering of technical or other services.

For the latest version of this document. Go to our website at
www.melexis.com

Or for additional information contact Melexis Direct:

Europe and Japan:
Phone: +32 1367 0495
E-mail: sales_europe@melexis.com

All other locations:
Phone: +1 603 223 2362
E-mail: sales_usa@melexis.com