QUAD/DUAL P-CHANNEL MATCHED PAIR MOSFET ARRAY

GENERAL DESCRIPTION

The ALD1107/ALD1117 are monolithic quad/dual P-channel enhancement mode matched MOSFET transistor arrays intended for a broad range of precision analog applications. The ALD1107/ALD1117 offer high input impedance and negative current temperature coefficient. The transistor pairs are matched for minimum offset voltage and differential thermal response, and they are designed for precision analog switching and amplifying applications in +2V to +12V systems where low input bias current, low input capacitance and fast switching speed are desired. These MOSFET devices feature very large (almost infinite) current gain in a low frequency, or near DC, operating environment. The ALD1107/ALD1117 are building blocks for differential amplifier input stages, transmission gates, and multiplexer applications, current sources and many precision analog circuits.

FEATURES

- Low threshold voltage of -0.7V
- Low input capacitance
- Low Vos 2mV typical
- High input impedance -- $10^{14}\Omega$ typical
- Negative current (I_{DS}) temperature coefficient
- Enhancement-mode (normally off)
- DC current gain 10^9
- Low input and output leakage currents
- RoHS compliant

ORDERING INFORMATION ("L" suffix denotes lead-free (RoHS))

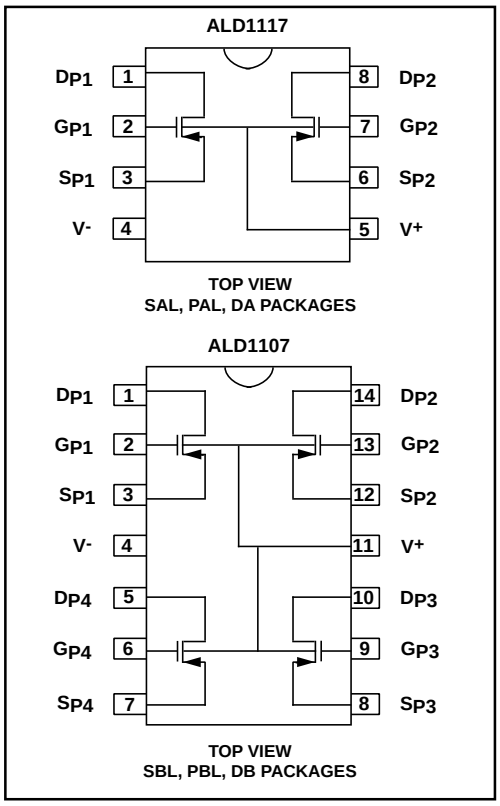
Operating Temperature Range*		
0°C to +70°C	0°C to +70°C	-55°C to +125°C
8-Pin SOIC Package	8-Pin Plastic Dip Package	8-Pin CERDIP Package
ALD1117SAL	ALD1117PAL	ALD1117DA
14-Pin SOIC Package	14-Pin Plastic Dip Package	14-Pin CERDIP Package
ALD1107SBL	ALD1107PBL	ALD1107DB

* Contact factory for leaded (non-RoHS) or high temperature versions.

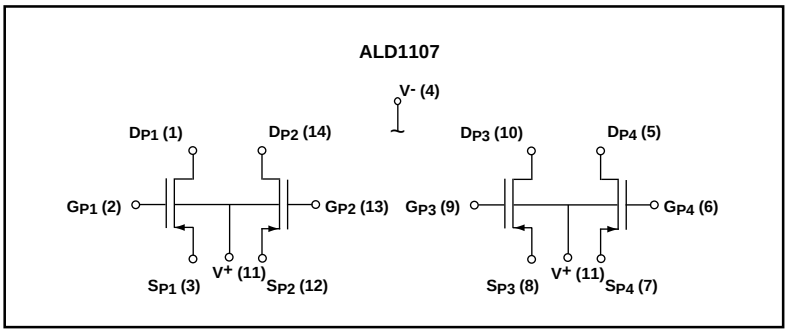
APPLICATIONS

- Precision current mirrors
- Precision current sources
- Voltage choppers
- Differential amplifier input stage
- Voltage comparator
- Data converters
- Sample and Hold
- Analog signal processing

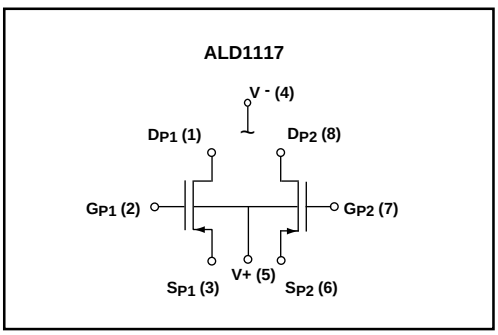
PIN CONFIGURATION



BLOCK DIAGRAM



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Drain-source voltage, V_{DS} ____ -10.6V
Gate-source voltage, V_{GS} ____ -10.6V
Power dissipation ____ 500mW
Operating temperature range SAL, PAL, SBL, PBL packages ____ 0°C to +70°C
DA, DB packages ____ -55°C to +125°C
Storage temperature range ____ -65°C to +150°C
Lead temperature, 10 seconds ____ +260°C
CAUTION: ESD Sensitive Device. Use static control procedures in ESD controlled environment.

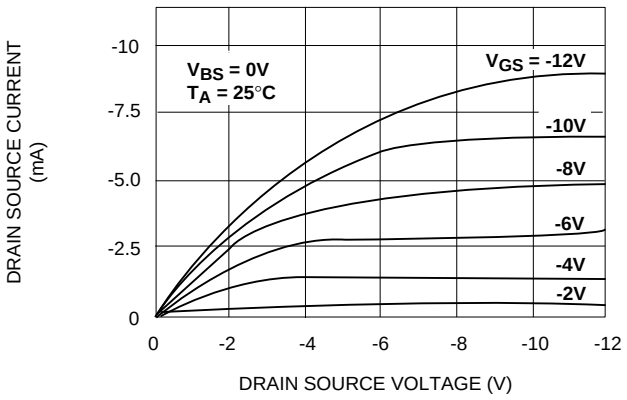
OPERATING ELECTRICAL CHARACTERISTICS
T_A = 25°C unless otherwise specified

		ALD1107			ALD1117				Test
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Conditions**
Gate Threshold Voltage	V_T	-0.4	-0.7	-1.0	-0.4	-0.7	-1.0	V	I_{DS} = -1.0μA V_{GS} = V_{DS}
Offset Voltage V_{GS1}-V_{GS2}	V_{OS}		2	10		2	10	mV	I_{DS} = -10μA V_{GS} = V_{DS}
Gate Threshold Temperature Drift [2]	TC_{VT}		-1.3			-1.3		mV/°C	
On Drain Current	$I_{DS\ (ON)}$	-1.3	-2		-1.3	-2		mA	V_{GS} = V_{DS} = -5V
Transconductance	G_{IS}	0.25	0.67		0.25	0.67		mmho	V_{DS} = -5V I_{DS} = -10mA
Mismatch	ΔG_{fs}		0.5			0.5		%	
Output Conductance	G_{OS}		40			40		μmho	V_{DS} = -5V I_{DS} = -10mA
Drain Source On Resistance	$R_{DS\ (ON)}$		1200	1800		1200	1800	Ω	V_{DS} = -0.1V V_{GS} = -5V
Drain Source On Resistance Mismatch	$\Delta R_{DS\ (ON)}$		0.5			0.5		%	V_{DS} = -0.1V V_{GS} = -5V
Drain Source Breakdown Voltage	BV_{DSS}	-12			-12			V	I_{DS} = -1.0μA V_{GS} = 0V
Off Drain Current [1]	$I_{DS\ (OFF)}$		10	400 4		10	400 4	pA nA	V_{DS} = -12V V_{GS} = 0V T_A = 125°C
Gate Leakage Current	I_{GSS}		0.1	10 1		0.1	10 1	pA nA	V_{DS} = 0V V_{GS} = -12V T_A = 125°C
Input Capacitance [2]	C_{ISS}		1	3		1	3	pF	

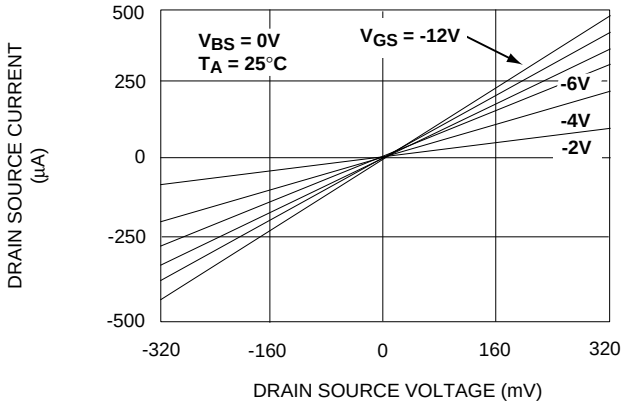
Notes: [1] Consists of junction leakage currents
[2] Sample tested parameters

TYPICAL PERFORMANCE CHARACTERISITCS

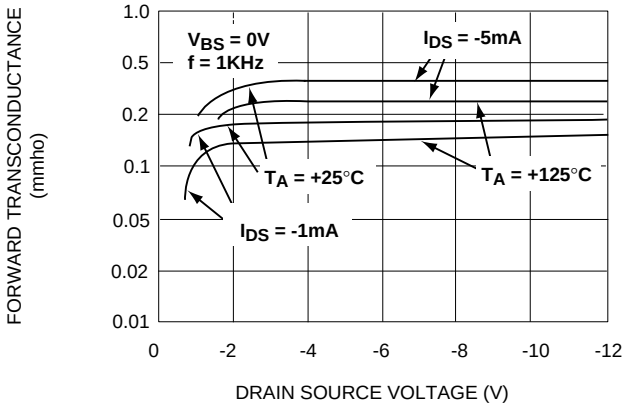
OUTPUT CHARACTERISTICS



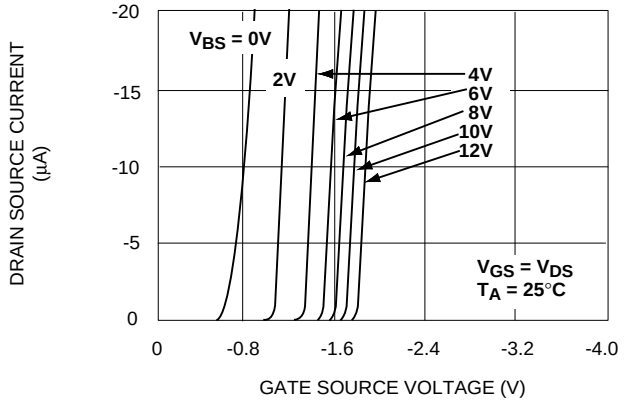
LOW VOLTAGE OUTPUT CHARACTERISTICS



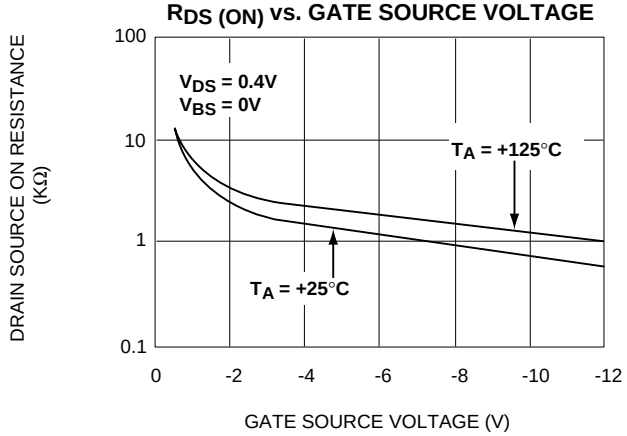
FORWARD TRANSCONDUCTANCE vs. DRAIN SOURCE VOLTAGE



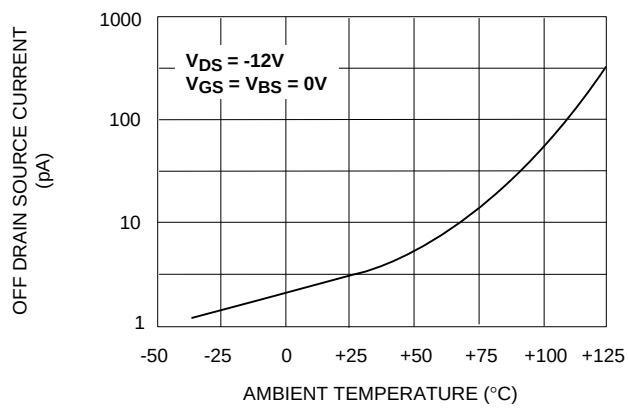
TRANSFER CHARACTERISTIC WITH SUBSTRATE BIAS



DRAIN SOURCE ON RESISTANCE $R_{DS\ (ON)}$ vs. GATE SOURCE VOLTAGE

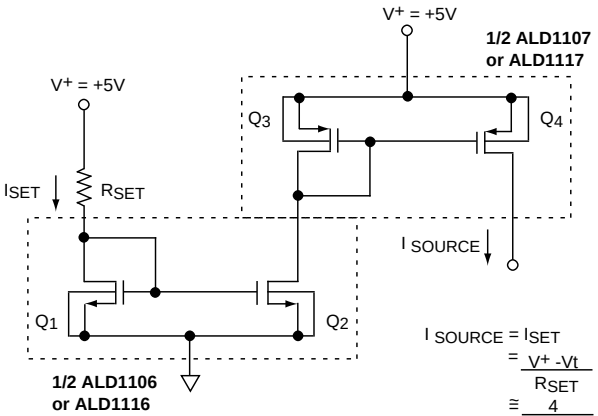


OFF DRAIN CURRENT vs. AMBIENT TEMPERATURE



TYPICAL APPLICATIONS

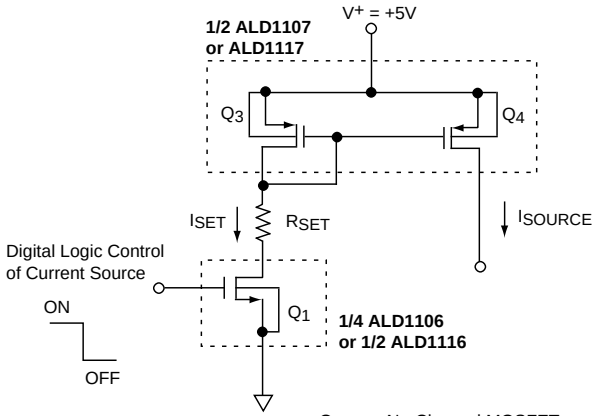
CURRENT SOURCE MIRROR



$I_{SOURCE} = I_{SET} = \frac{V^+ - Vt}{R_{SET}} \cong \frac{4}{R_{SET}}$

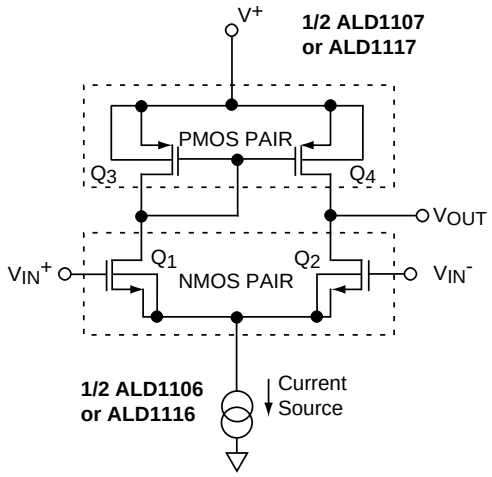
Q_1, Q_2: N - Channel MOSFET
Q_3, Q_4: P - Channel MOSFET

CURRENT SOURCE WITH GATE CONTROL



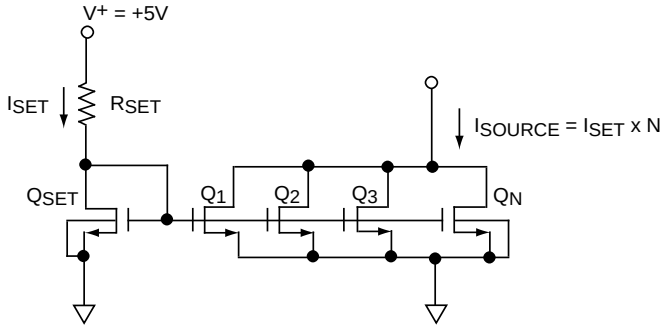
Q_1 : N - Channel MOSFET
Q_3,Q_4 : P - Channel MOSFET

DIFFERENTIAL AMPLIFIER



Q_1, Q_2: N - Channel MOSFET
Q_3, Q_4: P - Channel MOSFET

CURRENT SOURCE MULTIPLICATION

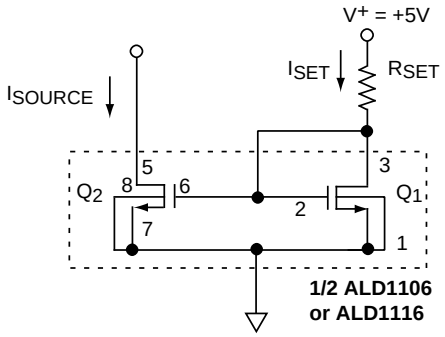


Q_{SET}, Q_1..Q_N: ALD1106 or ALD1116
N - Channel MOSFET

TYPICAL APPLICATIONS (cont.)

BASIC CURRENT SOURCES

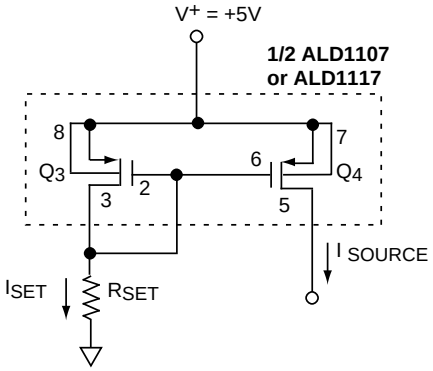
N- CHANNEL CURRENT SOURCE



$$I_{SOURCE} = I_{SET} = \frac{V^+ - Vt}{R_{SET}} \cong \frac{V^+ - 1.0}{R_{SET}} \cong \frac{4}{R_{SET}}$$

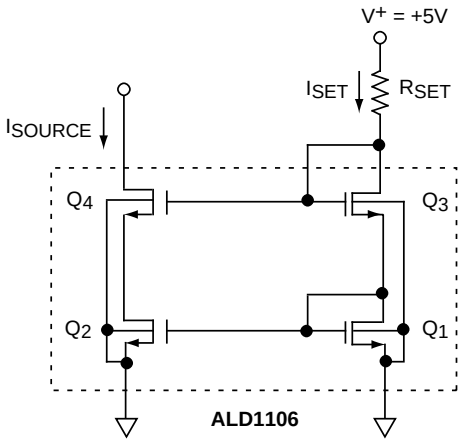
Q_1, Q_2 : N - Channel MOSFET

P- CHANNEL CURRENT SOURCE

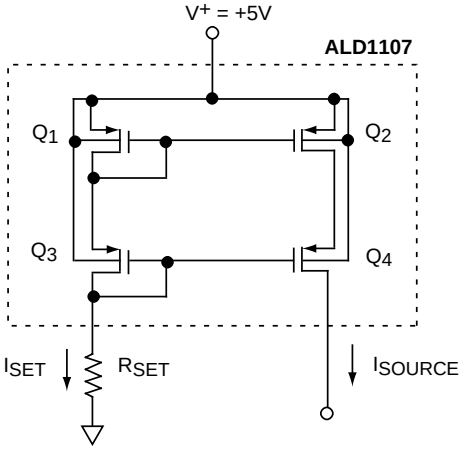


Q_3, Q_4: P - Channel MOSFET

CASCODE CURRENT SOURCES



Q_1, Q_2, Q_3, Q_4: N - Channel MOSFET
(ALD1101 or ALD1103)

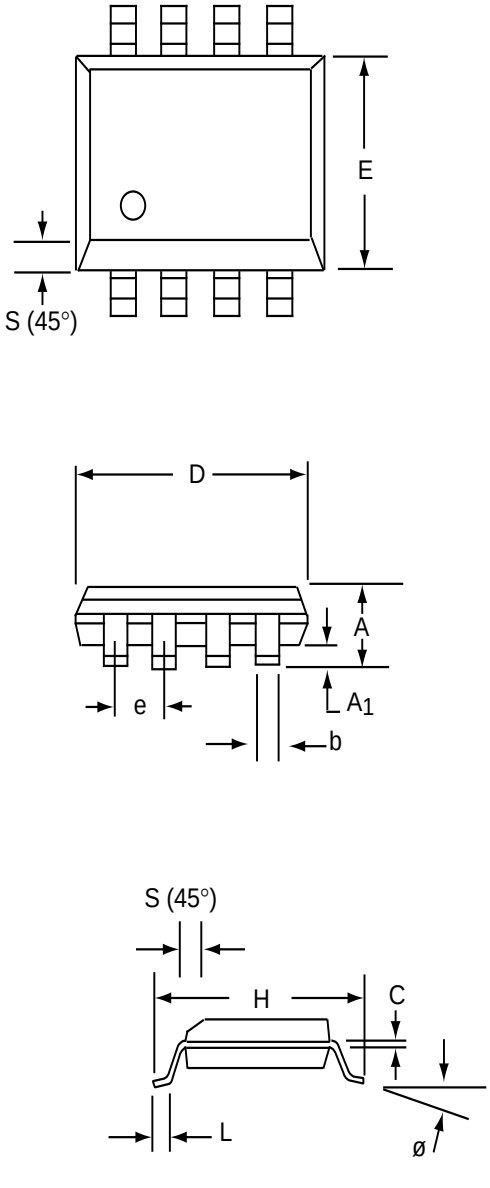


$$I_{SOURCE} = I_{SET} = \frac{V^+ - 2Vt}{R_{SET}} \cong \frac{3}{R_{SET}}$$

Q1, Q2, Q3, Q4: P - Channel MOSFET
(ALD1102 or ALD1103)

SOIC-8 PACKAGE DRAWING

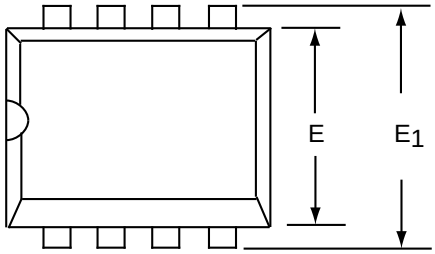
8 Pin Plastic SOIC Package

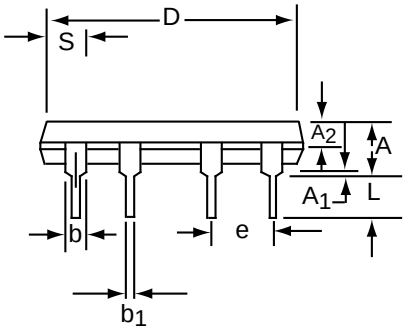


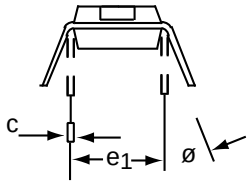
Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.25	0.004	0.010
b	0.35	0.45	0.014	0.018
C	0.18	0.25	0.007	0.010
D-8	4.69	5.00	0.185	0.196
E	3.50	4.05	0.140	0.160
e	1.27 BSC		0.050 BSC	
H	5.70	6.30	0.224	0.248
L	0.60	0.937	0.024	0.037
Ø	0°	8°	0°	8°
S	0.25	0.50	0.010	0.020

PDIP-8 PACKAGE DRAWING

8 Pin Plastic DIP Package



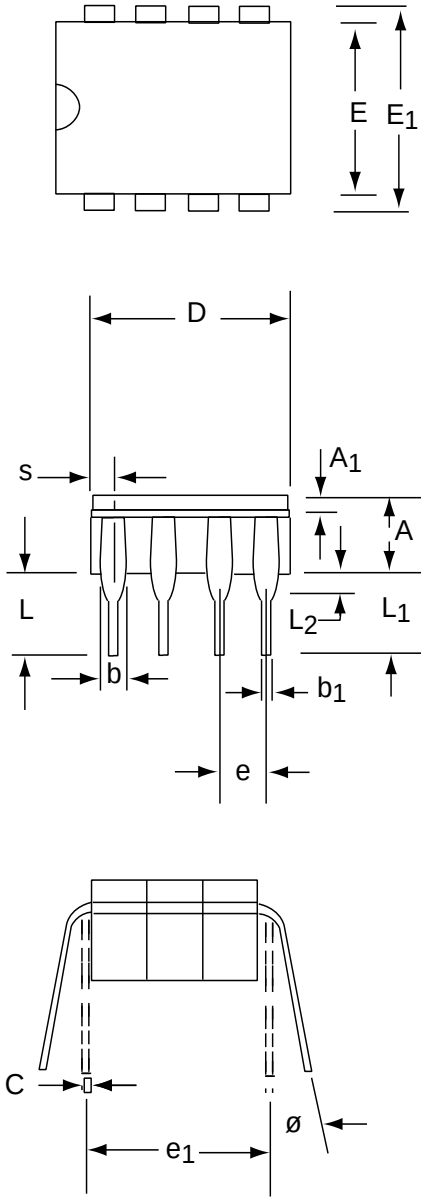




Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	3.81	5.08	0.105	0.200
A_1	0.38	1.27	0.015	0.050
A_2	1.27	2.03	0.050	0.080
b	0.89	1.65	0.035	0.065
b_1	0.38	0.51	0.015	0.020
c	0.20	0.30	0.008	0.012
D-8	9.40	11.68	0.370	0.460
E	5.59	7.11	0.220	0.280
E_1	7.62	8.26	0.300	0.325
e	2.29	2.79	0.090	0.110
e_1	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
S-8	1.02	2.03	0.040	0.080
ø	0°	15°	0°	15°

CERDIP-8 PACKAGE DRAWING

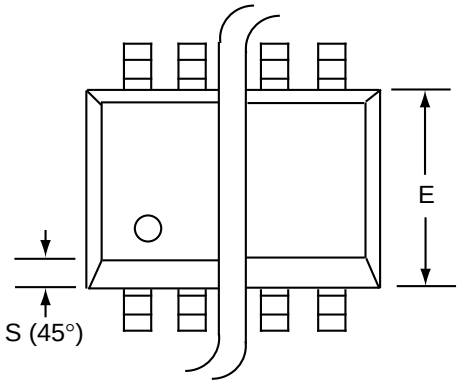
8 Pin CERDIP Package

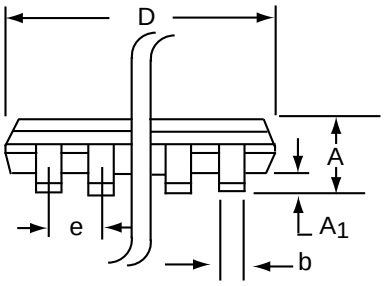


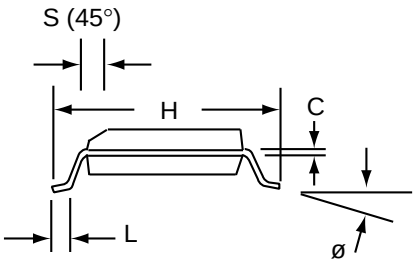
Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	3.55	5.08	0.140	0.200
A_1	1.27	2.16	0.050	0.085
b	0.97	1.65	0.038	0.065
b_1	0.36	0.58	0.014	0.023
C	0.20	0.38	0.008	0.015
D-8	--	10.29	--	0.405
E	5.59	7.87	0.220	0.310
E_1	7.73	8.26	0.290	0.325
e	2.54 BSC		0.100 BSC	
e_1	7.62 BSC		0.300 BSC	
L	3.81	5.08	0.150	0.200
L_1	3.18	--	0.125	--
L_2	0.38	1.78	0.015	0.070
S	--	2.49	--	0.098
Ø	0°	15°	0°	15°

SOIC-14 PACKAGE DRAWING

14 Pin Plastic SOIC Package



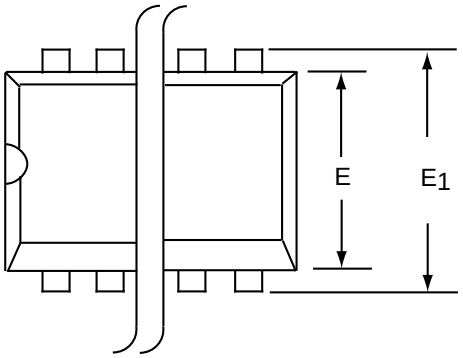


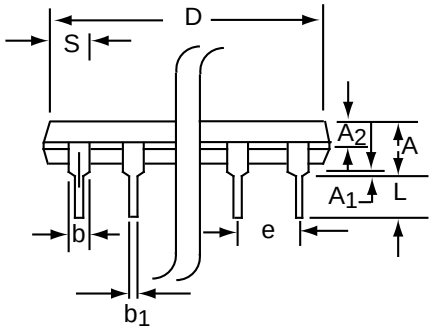


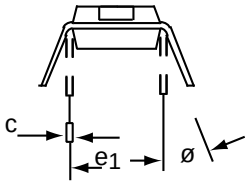
Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.25	0.004	0.010
b	0.35	0.45	0.014	0.018
C	0.18	0.25	0.007	0.010
D-14	8.55	8.75	0.336	0.345
E	3.50	4.05	0.140	0.160
e	1.27 BSC		0.050 BSC	
H	5.70	6.30	0.224	0.248
L	0.60	0.937	0.024	0.037
Ø	0°	8°	0°	8°
S	0.25	0.50	0.010	0.020

PDIP-14 PACKAGE DRAWING

14 Pin Plastic DIP Package



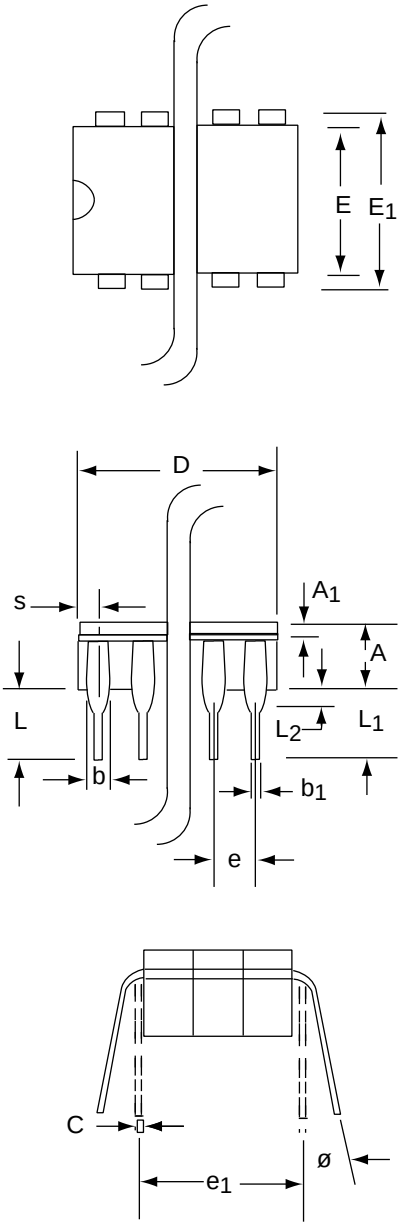




Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	3.81	5.08	0.105	0.200
A_1	0.38	1.27	0.015	0.050
A_2	1.27	2.03	0.050	0.080
b	0.89	1.65	0.035	0.065
b_1	0.38	0.51	0.015	0.020
c	0.20	0.30	0.008	0.012
D-14	17.27	19.30	0.680	0.760
E	5.59	7.11	0.220	0.280
E_1	7.62	8.26	0.300	0.325
e	2.29	2.79	0.090	0.110
e_1	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
S-14	1.02	2.03	0.040	0.080
ø	0°	15°	0°	15°

CERDIP-14 PACKAGE DRAWING

14 Pin CERDIP Package



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	3.55	5.08	0.140	0.200
A_1	1.27	2.16	0.050	0.085
b	0.97	1.65	0.038	0.065
b_1	0.36	0.58	0.014	0.023
C	0.20	0.38	0.008	0.015
D-14	--	19.94	--	0.785
E	5.59	7.87	0.220	0.310
E_1	7.73	8.26	0.290	0.325
e	2.54 BSC		0.100 BSC	
e_1	7.62 BSC		0.300 BSC	
L	3.81	5.08	0.150	0.200
L_1	3.18	--	0.125	--
L_2	0.38	1.78	0.015	0.070
S	--	2.49	--	0.098
Ø	0°	15°	0°	15°