

RJM0603JSC

Silicon N/P Channel Power MOS FET (6 in 1 Type)
High Speed Power Switching

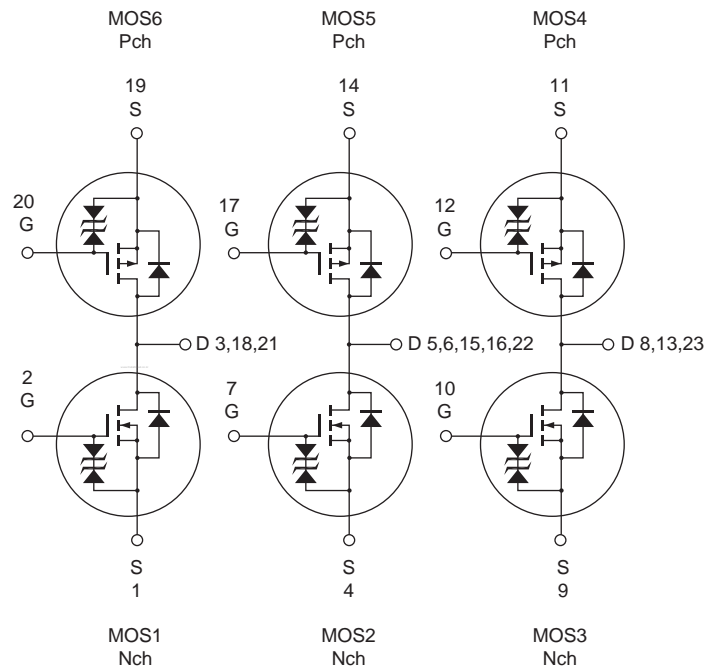
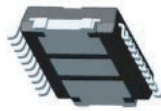
R07DS0339EJ0501
Rev.5.01
Jul 22, 2011

Features

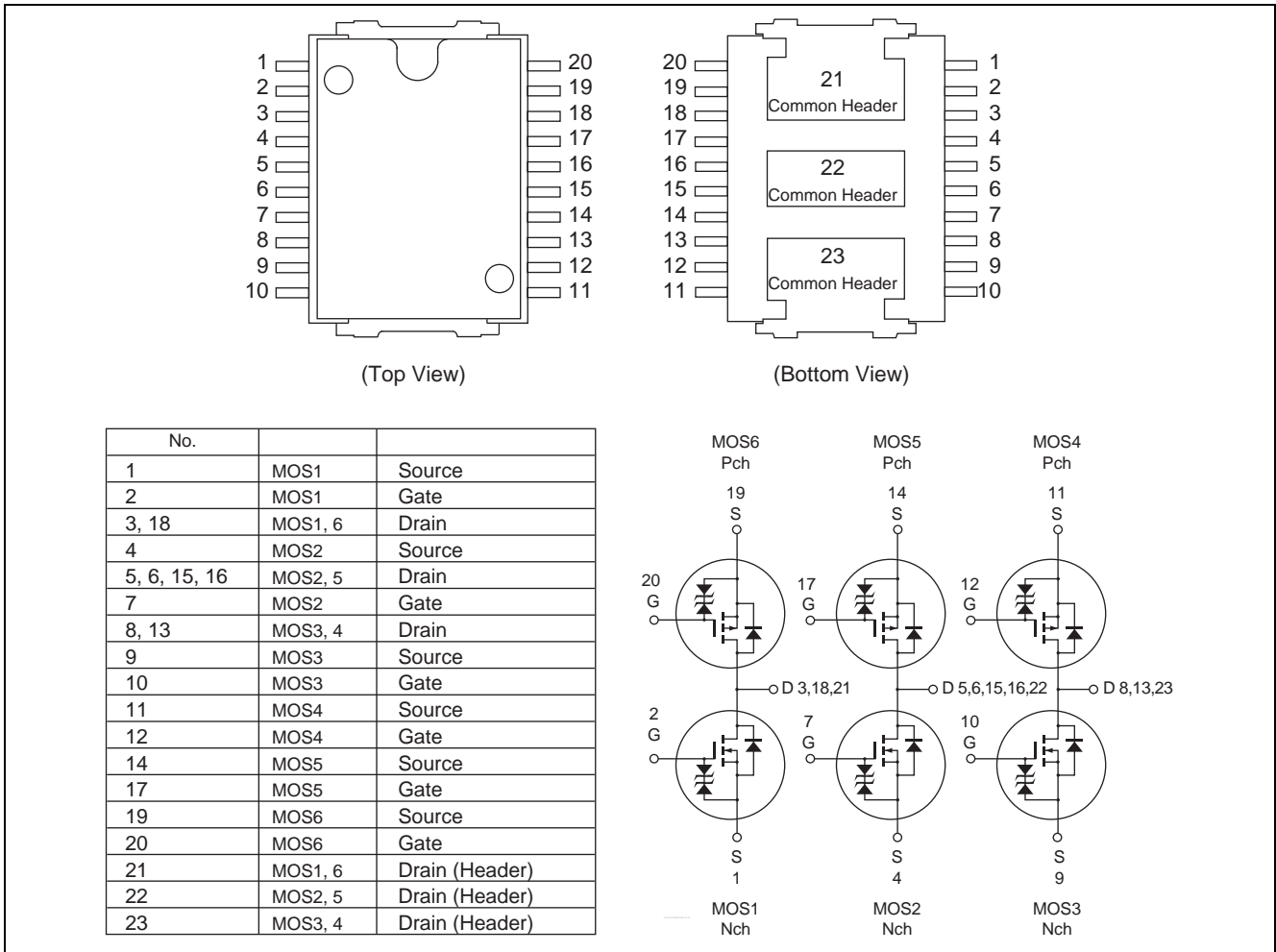
- For Automotive applications
- AEC-Q101 compliant
- N/P Channel MOS FET (6 in 1 Type). High density mounting
- Low on-resistance
- Capable of 4.5 V gate drive

Outline

RENESAS Package Code: PRSP0020DF-A
(Package Name: HSOP-20)



Pin Arrangement



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value		Unit
		MOS1, 2, 3 (Nch)	MOS4, 5, 6 (Pch)	
Drain to source voltage	V _{DSS}	60	-60	V
Gate to source voltage	V _{GSS}	+20 / -5	-20 / +5	V
Drain current	I _D	20	-20	A
Drain peak current	I _D (pulse) ^{Note1}	80	-80	A
Channel dissipation	P _{ch} ^{Note2}	54	54	W
Avalanche current	I _{AP} ^{Note3}	20	20	A
Avalanche energy	E _{AR} ^{Note3}	34	34	mJ
Channel temperature	T _{ch} ^{Note4}	175	175	°C
Storage temperature	T _{stg}	-55 to +150	-55 to +150	°C

- Notes: 1. PW ≤ 10μs duty cycle ≤ 1%
 2. 1 Drive Operation ; Value at Tc = 25°C
 3. Value at Tch = 25°C, Rg ≥ 50 Ω
 4. AEC-Q101 compliant

Thermal Impedance Characteristics

- Channel to case thermal impedance θ_{ch-c}: 2.78°C/W

Electrical Characteristics

• MOS1, MOS2, MOS3 (N Channel)

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero gate voltage drain current	I _{DSS}	—	—	10	μA	V _{DS} = 60 V, V _{GS} = 0
Gate to source leak current	I _{GSS}	—	—	±10	μA	V _{GS} = +20 V / -5 V, V _{DS} = 0
Gate to source cutoff voltage	V _{GS(off)}	1.0	—	2.5	V	V _{DS} = 10 V, I _D = 1 mA
Static drain to source on state resistance	R _{DS(on)}	—	16	20	mΩ	I _D = 10 A, V _{GS} = 10 V ^{Note5}
		—	21	32	mΩ	I _D = 10 A, V _{GS} = 4.5 V ^{Note5}
Input capacitance	C _{iss}	—	2600	—	pF	V _{DS} = 10V, V _{GS} = 0, f = 1 MHz
Output capacitance	C _{oss}	—	290	—	pF	
Reverse transfer capacitance	C _{rss}	—	140	—	pF	
Total gate charge	Q _g	—	43	—	nC	V _{DD} = 25 V, V _{GS} = 10 V, I _D = 20 A
Gate to source charge	Q _{gs}	—	6.2	—	nC	
Gate to drain charge	Q _{gd}	—	7.2	—	nC	
Turn-on delay time	t _{d(on)}	—	13	—	ns	V _{GS} = 10 V, I _D = 10 A, V _{DD} ≅ 30 V, R _L = 3 Ω, R _G = 4.7 Ω
Rise time	t _r	—	6	—	ns	
Turn-off delay time	t _{d(off)}	—	65	—	ns	
Fall time	t _f	—	4.5	—	ns	
Body-drain diode forward voltage	V _{DF}	—	0.91	1.18	V	I _F = 20 A, V _{GS} = 0 ^{Note5}
Body-drain diode reverse recovery time	t _{rr}	—	35	—	ns	I _F = 20 A, V _{GS} = 0 di _F /dt = 100 A/μs

Note: 5. Pulse test

• MOS4, MOS5, MOS6 (P Channel)

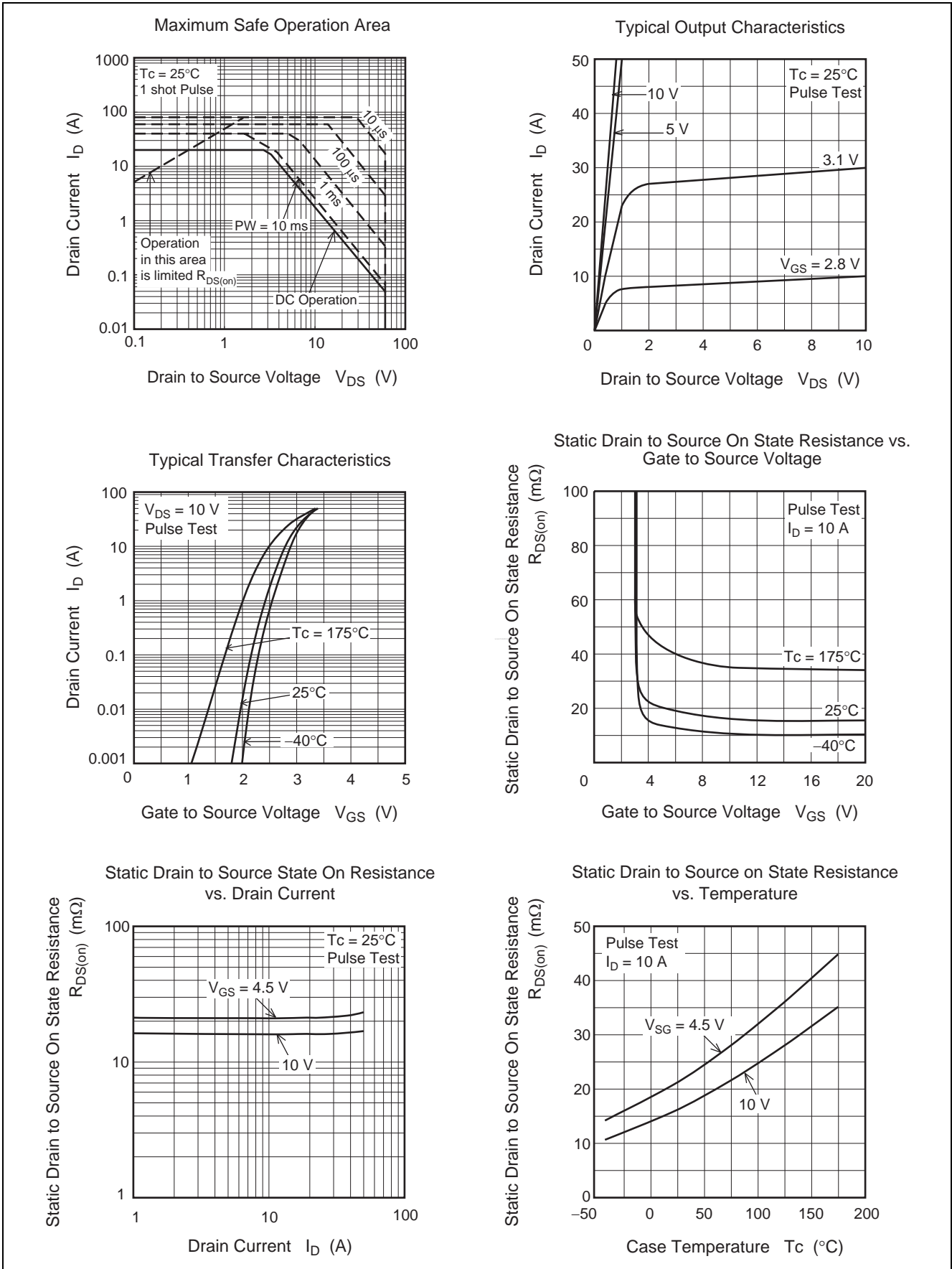
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero gate voltage drain current	I _{DSS}	—	—	-10	μA	V _{DS} = -60 V, V _{GS} = 0
Gate to source leak current	I _{GSS}	—	—	±10	μA	V _{GS} = -20 V / +5 V, V _{DS} = 0
Gate to source cutoff voltage	V _{GS(off)}	-1.0	—	-2.5	V	V _{DS} = -10 V, I _D = -1 mA
Static drain to source on state resistance	R _{DS(on)}	—	32	40	mΩ	I _D = -10 A, V _{GS} = -10 V ^{Note6}
		—	42	64	mΩ	I _D = -10 A, V _{GS} = -4.5 V ^{Note6}
Input capacitance	C _{iss}	—	2600	—	pF	V _{DS} = -10 V, V _{GS} = 0, f = 1 MHz
Output capacitance	C _{oss}	—	330	—	pF	
Reverse transfer capacitance	C _{rss}	—	240	—	pF	
Total gate charge	Q _g	—	53	—	nC	V _{DD} = -25 V, V _{GS} = -10 V, I _D = -20 A
Gate to source charge	Q _{gs}	—	8.8	—	nC	
Gate to drain charge	Q _{gd}	—	13	—	nC	
Turn-on delay time	t _{d(on)}	—	22	—	ns	V _{GS} = -10 V, I _D = -10 A, V _{DD} ≅ -30 V, R _L = 3 Ω, R _G = 4.7 Ω
Rise time	t _r	—	17	—	ns	
Turn-off delay time	t _{d(off)}	—	100	—	ns	
Fall time	t _f	—	20	—	ns	
Body-drain diode forward voltage	V _{DF}	—	-0.95	-1.24	V	I _F = -20 A, V _{GS} = 0 ^{Note6}
Body-drain diode reverse recovery time	t _{rr}	—	50	—	ns	I _F = -20 A, V _{GS} = 0 di _F /dt = 100 A/μs

Note: 6. Pulse test

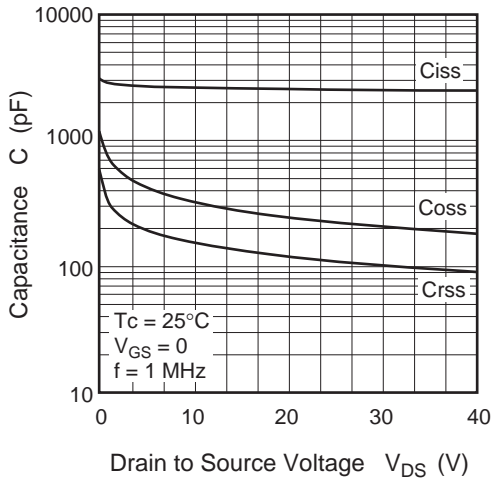
Main Characteristics

- MOS1, MOS2, MOS3 (N Channel)

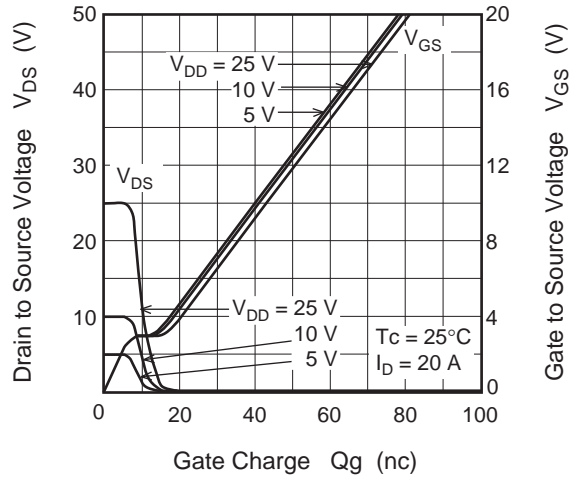


• MOS1, MOS2, MOS3 (N Channel)

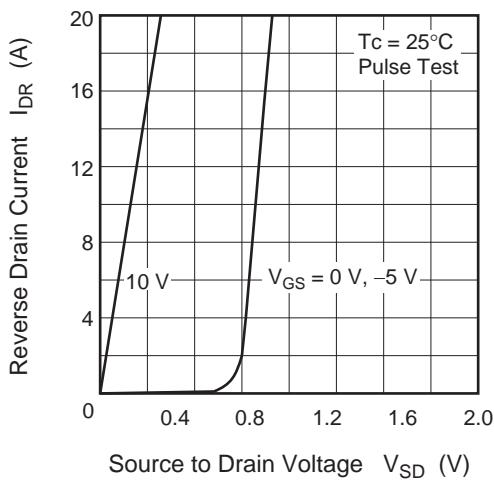
Typical Capacitance vs. Drain to Source Voltage



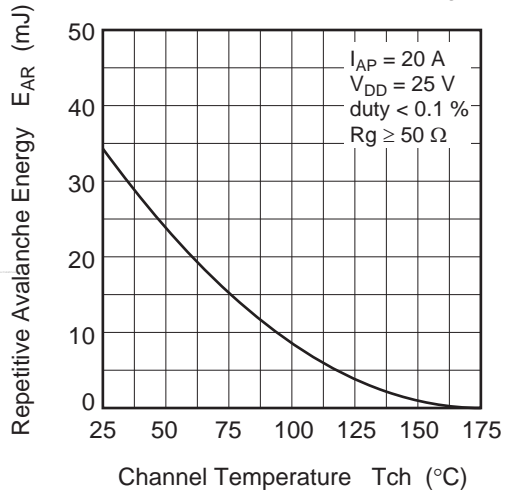
Dynamic Input Characteristics



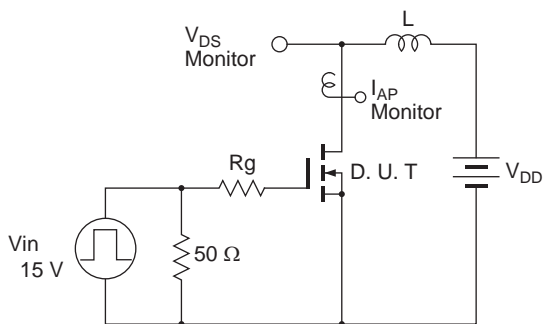
Reverse Drain Current vs. Source to Drain Voltage



Avalanche Energy vs. Channel Temperature Derating

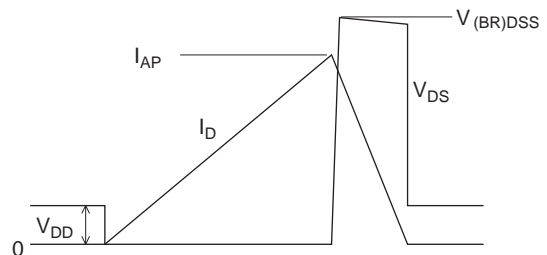


Avalanche Test Circuit

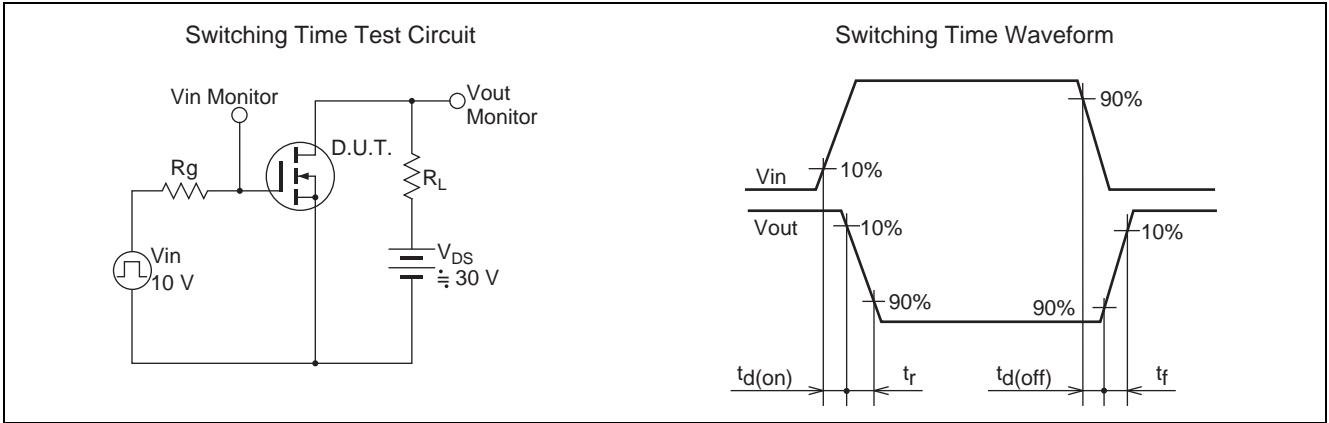


Avalanche Waveform

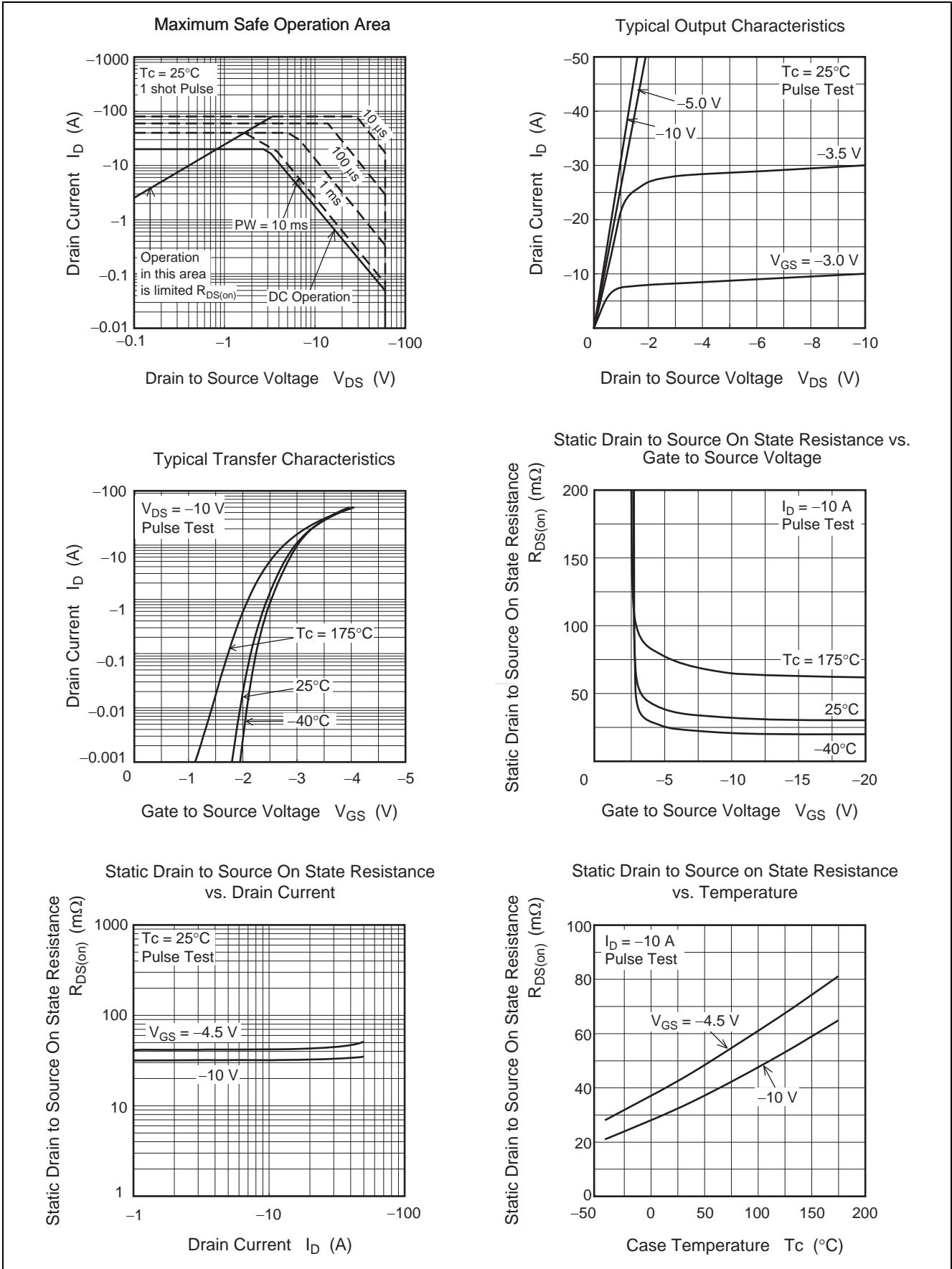
$$E_{AR} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



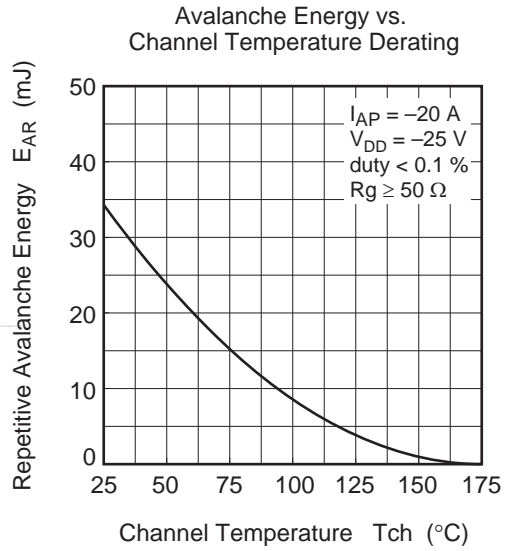
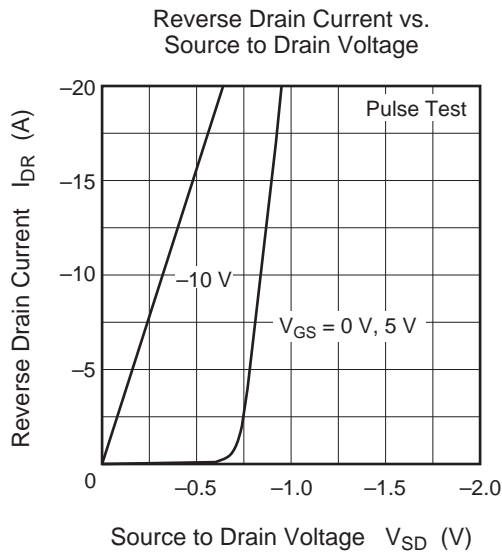
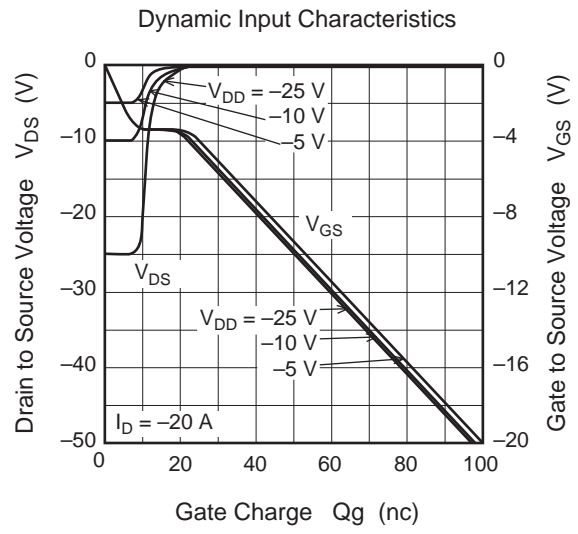
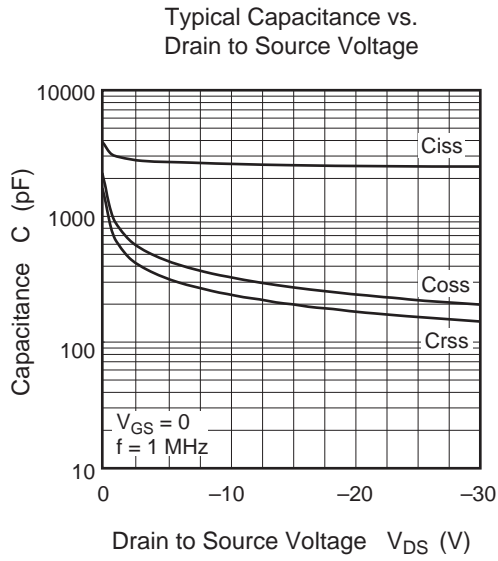
• MOS1, MOS2, MOS3 (N Channel)



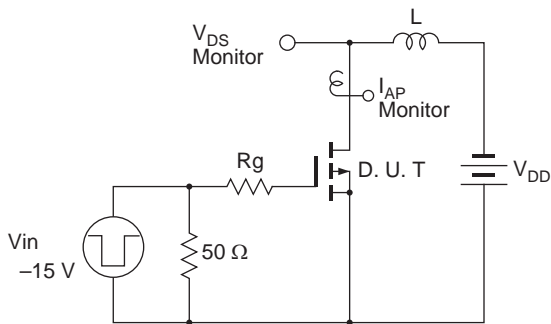
• MOS4, MOS5, MOS6 (P Channel)



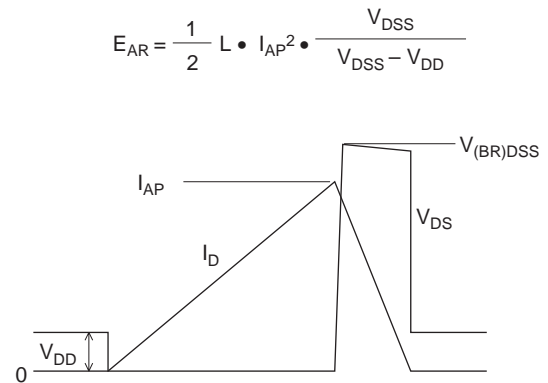
• MOS4, MOS5, MOS6 (P Channel)



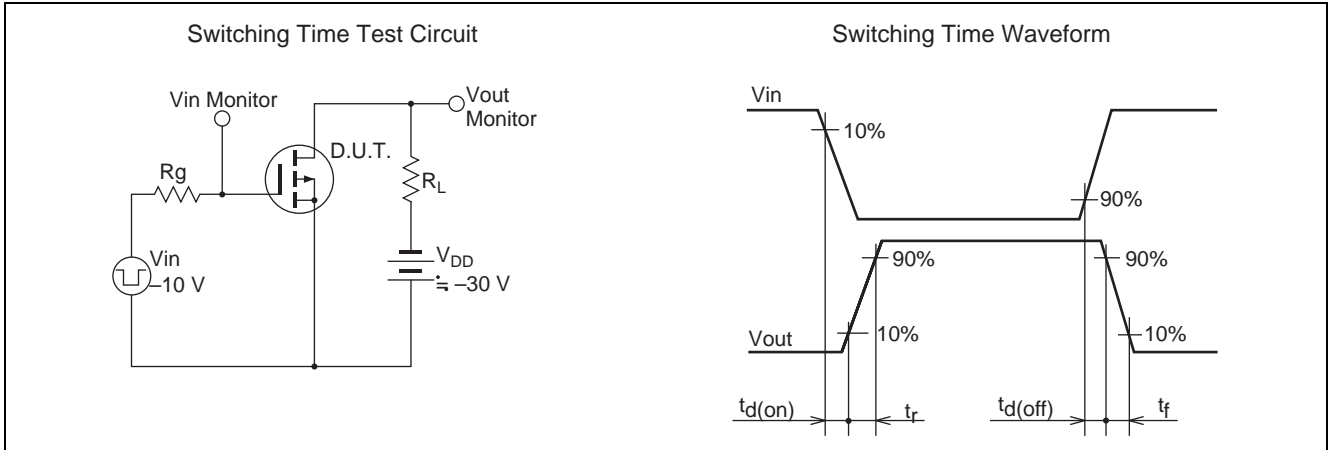
Avalanche Test Circuit



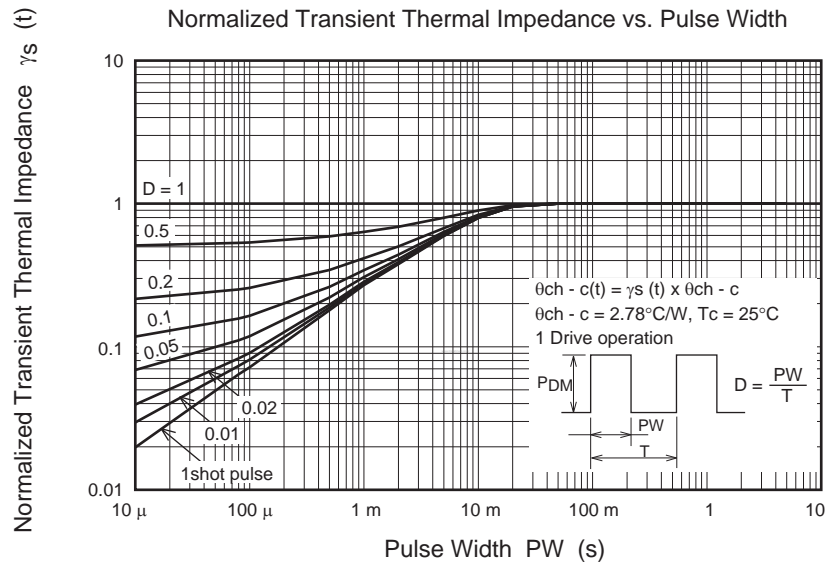
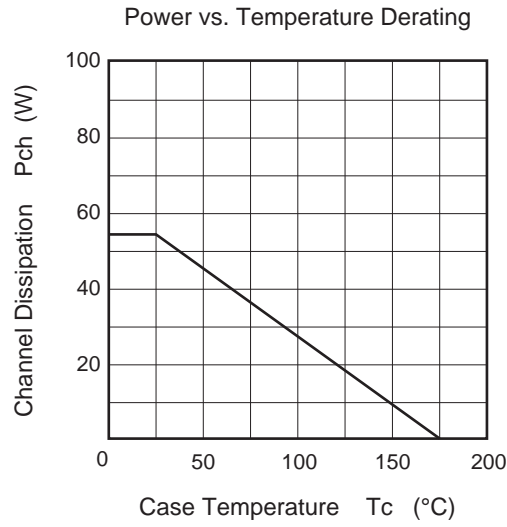
Avalanche Waveform



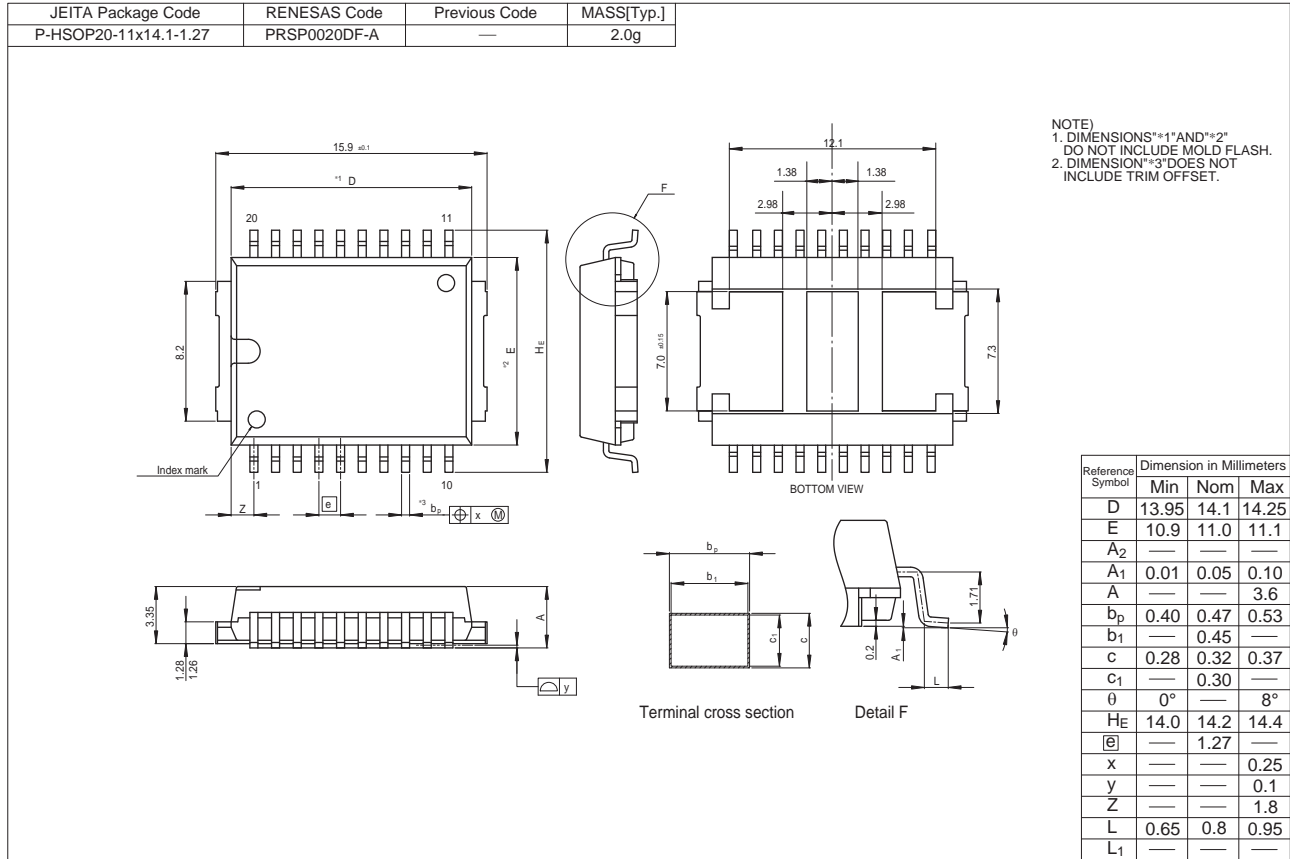
• MOS4, MOS5, MOS6 (P Channel)



• Common



Package Dimensions



Ordering Information

Orderable Part Number	Quantity	Shipping Container
RJM0603JSC-00-12	700 pcs	Tray

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