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512K x 32Bit CMOS Quad CAS DRAM with EDO

DESCRIPTION

This is a 524,288 x 32 bit Extended Data Out CMOS DRAM. Extended Data Out Mode offers high speed random access of memory cells within the same row, so called Hyper Page Mode. Power supply voltage (+5.0V or +3.3V), refresh cycle 1K, access time (-50 or -60), power consumption(Normal or Low power) and SOJ package type are optional features of this family. All of this family have CAS-before-RAS refresh, RAS-only refresh and Hidden refresh capabilities. Furthermore, Self-refresh operation is available in L-version. This 512Kx32 EDO Mode Quad CAS DRAM is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

FEATURES

• Part Identification

- K4Q153211M-JC (5.0V, 1K Ref.)
- K4Q153211M-JL (5.0V, 1K Ref. LP)
- K4Q153212M-JC (3.3V, 1K Ref.)
- K4Q153212M-JL (3.3V, 1K Ref. LP)

- Extended Data Out Mode operation (Fast Page Mode with Extended Data Out)
- Four separate CAS pins provide for separate I/O operation
- CAS-before-RAS refresh capability
- RAS-only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Plastic SOJ 400mil x 1125mil package
- Single +5.0V±0.5V power supply(5V product)
- Single +3.3V±0.3V power supply(3.3V product)

• Active Power Dissipation

Unit : mW

Speed	3.3V	5.0V
-50	-	880
-60	540	825

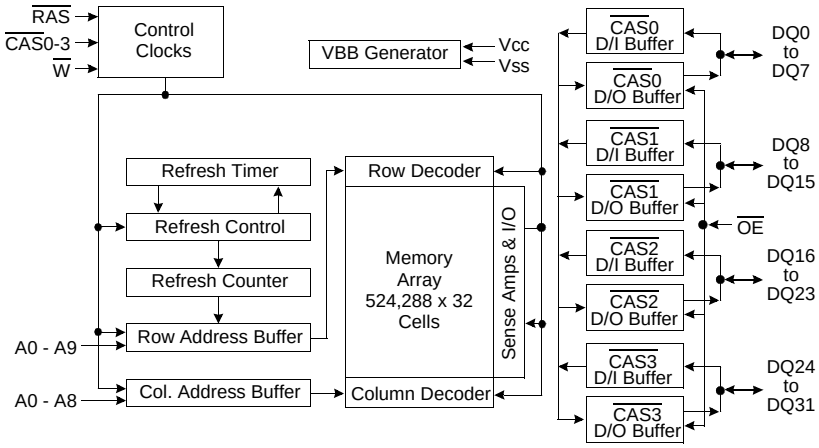
• Refresh Cycles

Part NO.	VCC	Refresh cycle	Refresh period	
			Normal	L-ver
153211M-J	5.0V	1K	16ms	128ms
153212M-J	3.3V	1K	16ms	128ms

• Performance Range

Speed	tRAC	tCAC	tRC	tHPC	Remark
-50	50ns	15ns	84ns	20ns	5.0V only
-60	60ns	17ns	104ns	27ns	5V/3.3V

FUNCTIONAL BLOCK DIAGRAM



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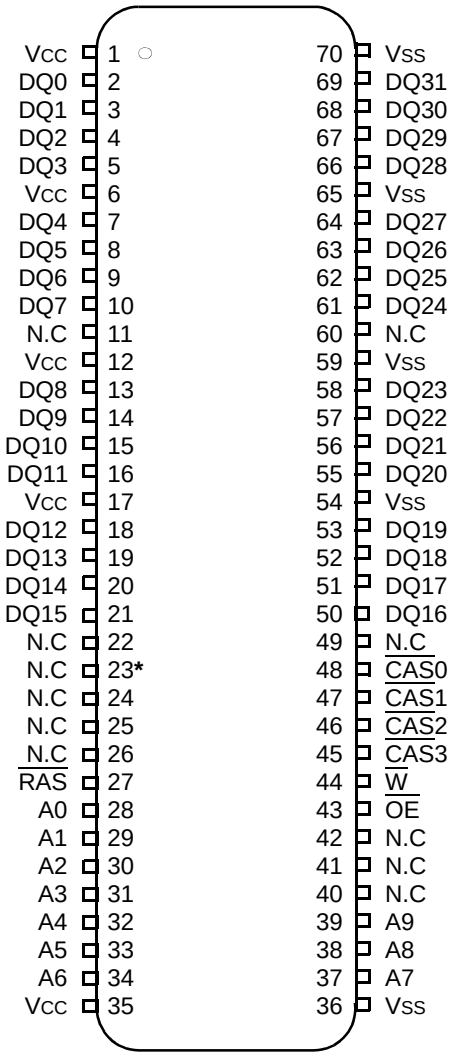
PIN CONFIGURATION (Top Views)



K4Q153211(2)M-J

J : 400mil 70pin SOJ

Pin Name	Pin Function
A0 - A9	Address Inputs
DQ0 - 31	Data In/Out
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$0 - 3	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
Vss	Ground
Vcc	Power(+5V)
	Power(+3.3V)
N.C	No Connection

* Pin23 : must be NC or Vss

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-0.5 to +4.6	-1.0 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	-1.0 to +7.0	V
Storage Temperature	Tstg	-55 to +150	-55 to +150	°C
Power Dissipation	P_D	1	1	W
Short Circuit Output Current	I_{OS} Address	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A= 0 to 70°C)

Parameter	Symbol	3.3V			5V			Units
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	V_{CC}+0.3[*1]	2.4	-	V_{CC}+1.0[*1]	V
Input Low Voltage	V_{IL}	-0.3[*2]	-	0.8	-1.0[*2]	-	0.8	V

*1 : V_{CC}+1.3V/15ns(3.3V), V_{CC}+2.0V/15ns(5V), Pulse width is measured at V_{CC}
*2 : -1.3V/15ns(3.3V), -2.0V/20ns(5V), Pulse width is measured at V_{SS}

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Max	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input 0≤V_{IN}≤V_{IN}+0.3V, all other input pins not under test=0 Volt)	$I_{I(L)}$	-5	5	uA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{CC})	$I_{O(L)}$	-5	5	uA
	Output High Voltage Level(I_{OH}=-2mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level(I_{OL}=2mA)	V_{OL}	-	0.4	V
5V	Input Leakage Current (Any input 0≤V_{IN}≤V_{IN}+0.5V, all other input pins not under test=0 Volt)	$I_{I(L)}$	-5	5	uA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{CC})	$I_{O(L)}$	-5	5	uA
	Output High Voltage Level(I_{OH}=-5mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level(I_{OL}=4.2mA)	V_{OL}	-	0.4	V

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DC AND OPERATING CHARACTERISTICS (Continued)

Symbol	Power	Speed	Max		Units
			K4Q153212M-J	K4Q153211M-J	
I_{CC1}	Don't care	-50 -60	- 150	160 150	mA mA
I_{CC2}	Normal L-ver	Don't care	- 1	2 1	mA mA
I_{CC3}	Don't care	-50 -60	- 150	160 150	mA mA
I_{CC4}	Don't care	-50 -60	- 100	110 100	mA mA
I_{CC5}	Normal L-ver	Don't care	500 300	1000 500	uA uA
I_{CC6}	Don't care	-50 -60	- 150	160 150	mA mA
I_{CC7}	L-ver	Don't care	300	500	uA
I_{CCS}	L-ver	Don't care	200	300	uA

I_{CC1}* : Operating Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min.)

I_{CC2} : Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = $\overline{W}$ = V_{IH})

I_{CC3}* : $\overline{RAS}$-only Refresh Current ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$, Address cycling @t_{RC}=min.)

I_{CC4}* : Hyper Page Mode Current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address cycling @t_{HPC}=min.)

I_{CC5} : Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = $\overline{W}$ = V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$, $\overline{CAS}$ cycling @t_{RC}=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH}) = V_{CC}-0.2V, Input low voltage(V_{IL}) = 0.2V, $\overline{CAS}$ = 0.2V,

Din = Don't care, t_{RC} = 125us(1K/L-ver)

t_{RAS} = t_{RAS}min~300ns

I_{CCS} : Self Refresh Current

$\overline{RAS}$=$\overline{CAS}$0~3 =V_{IL}, $\overline{W}$ = $\overline{OE}$ = A0 ~ A9 = V_{CC}-0.2V or 0.2V,

DQ0 ~ DQ31 = V_{CC}-0.2V, 0.2V or Open

***Note :** I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3} and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Hyper page mode cycle time, t_{HPC}.

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CAPACITANCE (T_A=25°C, V_{CC}=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Units
Input capacitance [A0 ~ A9]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$x, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output capacitance [DQ0 - DQ31]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)

Test condition (5V device) : V_{CC}=5.0V±0.5V, Vih/Vil=2.4/0.8V, Voh/Vol=2.0/0.8V

Test condition (3.3V device) : V_{CC}=3.3V±0.3V, Vih/Vil=2.2/0.8V, Voh/Vol=2.0/0.8V

Parameter	Symbol	-50*1		-60		Units	Notes
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	115		140		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		15		17	ns	3,4,5,18
Access time from column address	t_{AA}		25		30	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		ns	3,18
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	15	ns	6,11,18
$\overline{OE}$ to output in Low-Z	t_{OLZ}	3		3		ns	3
Transition time (rise and fall)	t_T	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		17		ns	14
$\overline{CAS}$ hold time	t_{CSH}	40		48		ns	17
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	12	10K	ns	23
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	35	20	43	ns	4,16
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	15
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	16
Column address hold time	t_{CAH}	8		10		ns	16
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8,15
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write command hold time	t_{WCH}	10		10		ns	14
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	8		10		ns	17

Note) *1 : 5V only

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AC CHARACTERISTICS (Continued)

Parameter	Symbol	-50*1		-60		Units	Notes
		Min	Max	Min	Max		
Data set-up time	t_{DS}	0		0		ns	9
Data hold time	t_{DH}	8		10		ns	9
Refresh period (1K, Normal)	t_{REF}		16		16	ms	
Refresh period (L-ver)	t_{REF}		128		128	ms	
Write command set-up time	t_{WCS}	0		0		ns	7,16
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	32		36		ns	7,14
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	67		79		ns	7
Column address $\overline{W}$ delay time	t_{AWD}	42		49		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	47		54		ns	7
$\overline{CAS}$ set-up time ($\overline{CAS}$ -before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	16
$\overline{CAS}$ hold time ($\overline{CAS}$ -before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	15
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	16
Access time from $\overline{CAS}$ precharge	t_{CPA}		28		35	ns	3,15
Hyper Page mode cycle time	t_{HPC}	20		27		ns	12,19
Hyper Page read-modify-write cycle time	t_{HPRWC}	47		56		ns	12,19
$\overline{CAS}$ precharge time (Hyper Page cycle)	t_{CP}	7		7		ns	20
$\overline{RAS}$ pulse width (Hyper Page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		ns	
$\overline{OE}$ access time	t_{OEA}		13		15	ns	21
$\overline{OE}$ to data delay	t_{OED}	13		15		ns	22
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	3	13	3	15	ns	6
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
Output data hold time	t_{DOH}	5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	13	3	15	ns	6,11
Output buffer turn off delay from $\overline{W}$	t_{WEZ}	3	13	3	15	ns	6
$\overline{W}$ to data delay	t_{WED}	15		15		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width (Hyper Page Cycle)	t_{WPE}	5		5		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{RASS}	100		100		us	25,26,27
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{RPS}	90		110		ns	25,26,27
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{CHS}	-50		-50		ns	25,26,27
Hold time $\overline{CAS}$ low to $\overline{CAS}$ high	t_{CLCH}	5		5		ns	13,24

Note) *1 : 5V only

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NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only refresh or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals.
   Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 1 TTL load and 50pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only.
   If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{oh} or V_{ol}.
7. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the first $\overline{CAS}$ falling edge in early write cycles and to $\overline{W}$ falling edge in $\overline{OE}$ controlled write cycle and read-modify-write cycles.
10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only.
    If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
11. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going.
    If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
12. $t_{ASC} \geq 6$ns, Assume t_T = 2.0ns.
13. In order to hold the address latched by the first $\overline{CAS}$ going low, the parameter t_{CLCH} must be met.
14. The last $\overline{CAS}$x edge to go low.
15. The last $\overline{CAS}$x edge to go high.
16. The first $\overline{CAS}$x edge to go low.
17. The first $\overline{CAS}$x edge to go high.
18. Output parameter is refrenced to corresponding $\overline{CAS}$x input.
19. The last rising $\overline{CAS}$x edge to next cycle's last rising $\overline{CAS}$x edge.
20. The last rising $\overline{CAS}$x edge to first falling $\overline{CAS}$x edge.
21. The first DQx controlled by the first $\overline{CAS}$x to go low.
22. The last DQx controlled by the last $\overline{CAS}$x to go high.
23. Each $\overline{CAS}$x must meet minimum pulse width.
24. The last falling $\overline{CAS}$x edge to the first rising $\overline{CAS}$x edge.
25. If $t_{RASS} \geq 100$us, then $\overline{RAS}$ precharge time must use t_{RPS} instead of t_{RP}.
26. For $\overline{RAS}$-only refresh and burst $\overline{CAS}$-before-$\overline{RAS}$ refresh mode, 1024(1K) cycles of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.
27. For distributed $\overline{CAS}$-before-$\overline{RAS}$ with 15.6us interval, $\overline{CAS}$-before-$\overline{RAS}$ refresh should be executed with in 15.6us immediately before and after self refresh in order to meet refresh specification.

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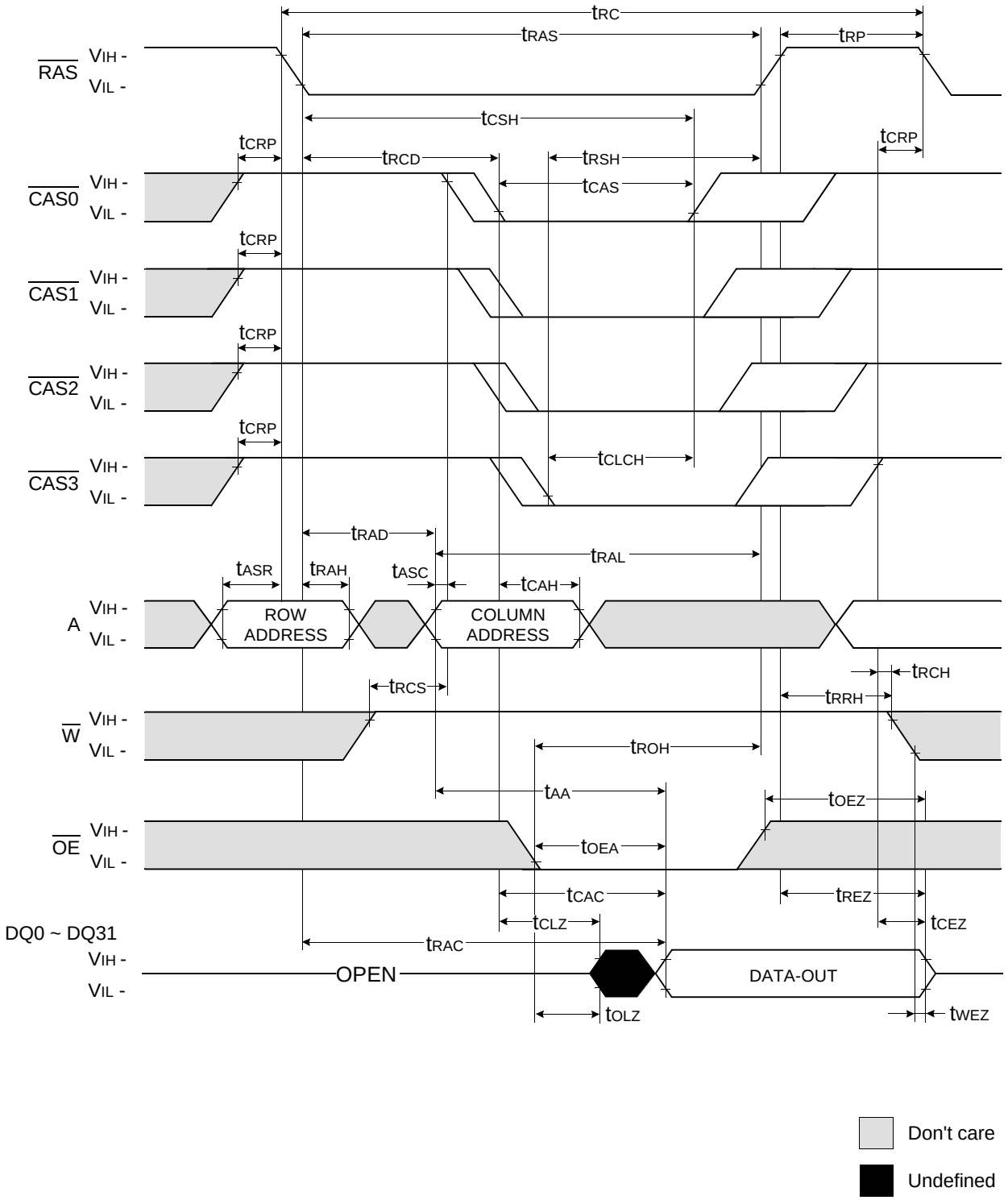
2 WORDS READ CYCLE



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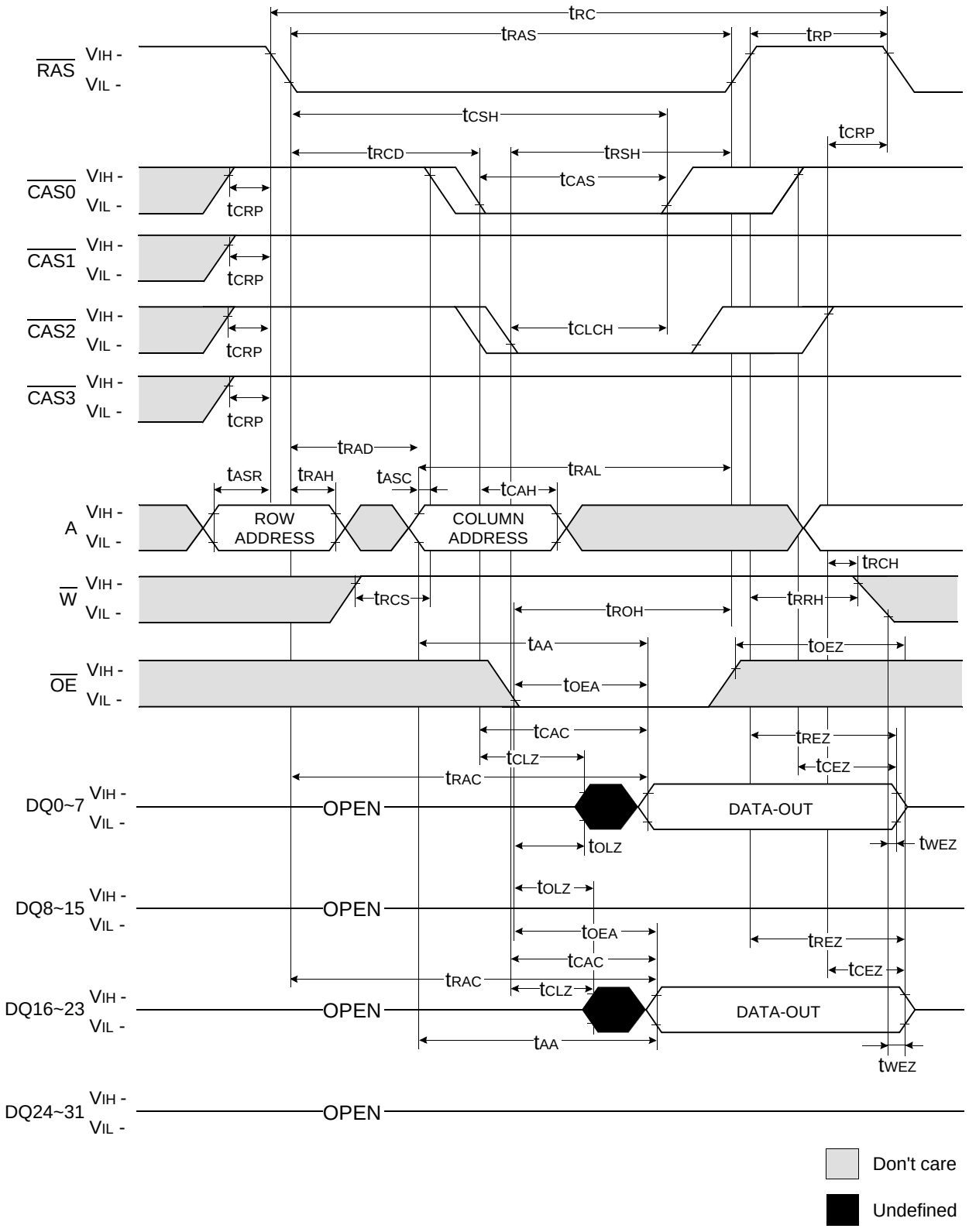
BYTE WIDE READ CYCLE

NOTE : DOUT = OPEN



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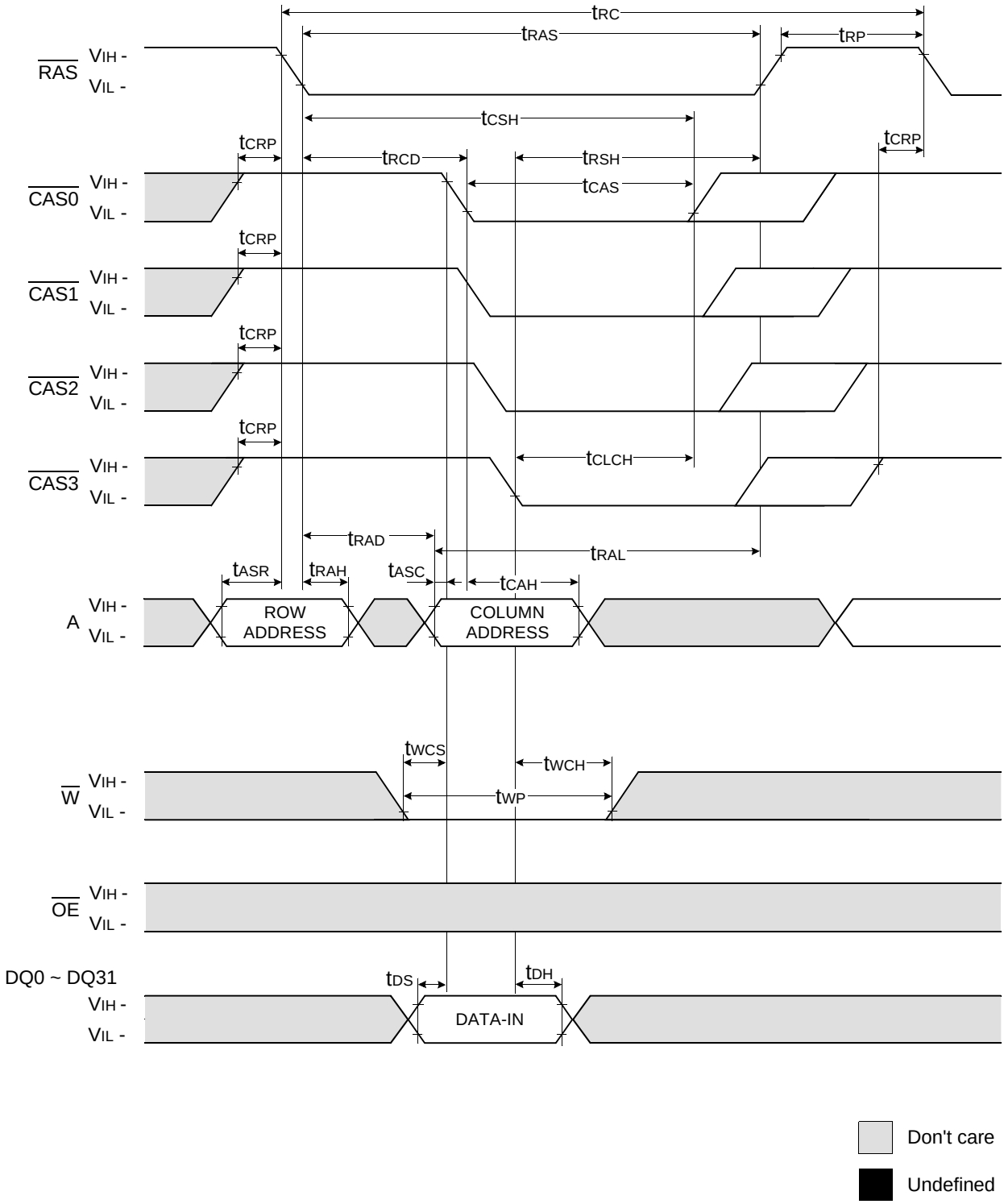
2 WORDS WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



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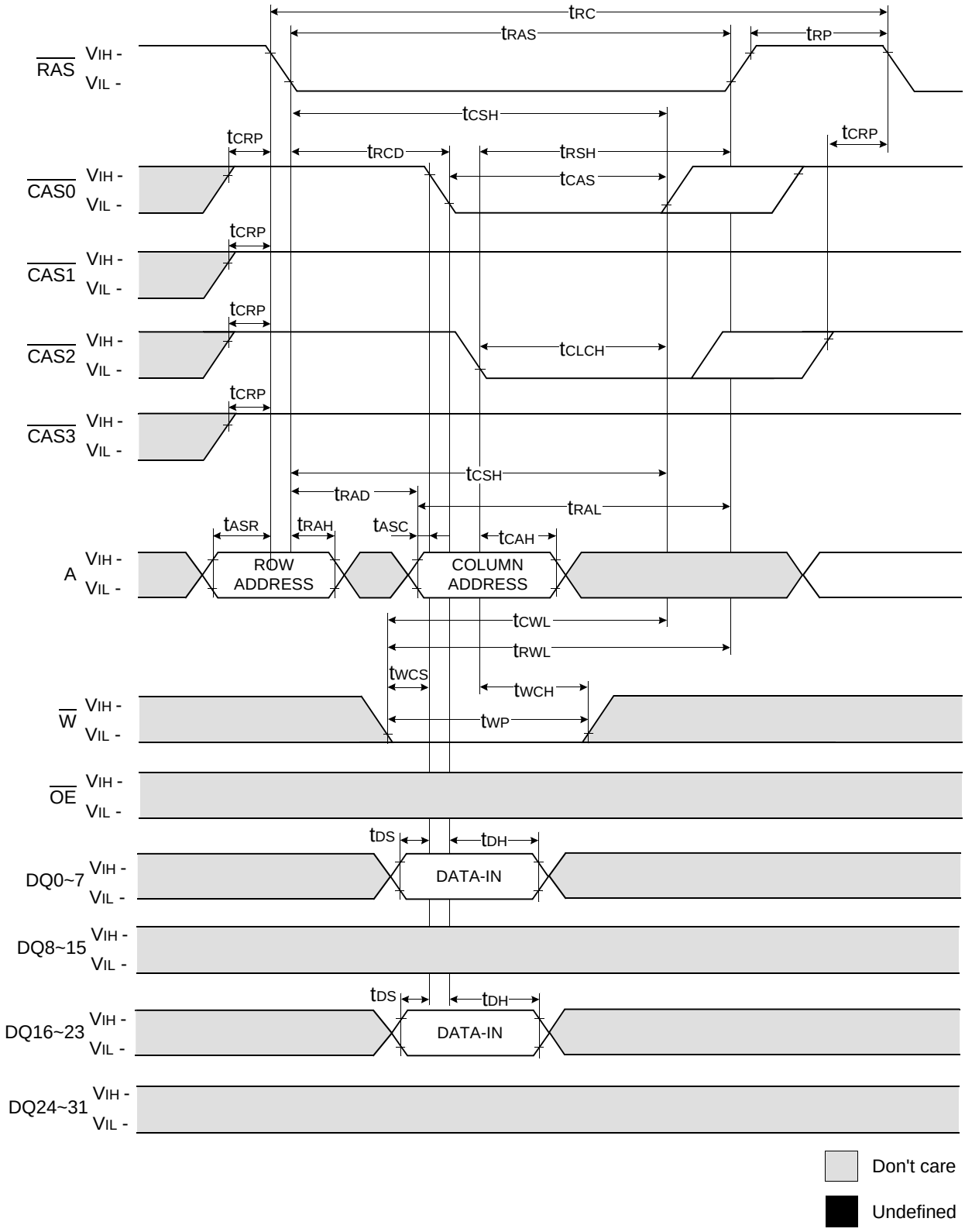
BYTE WIDE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



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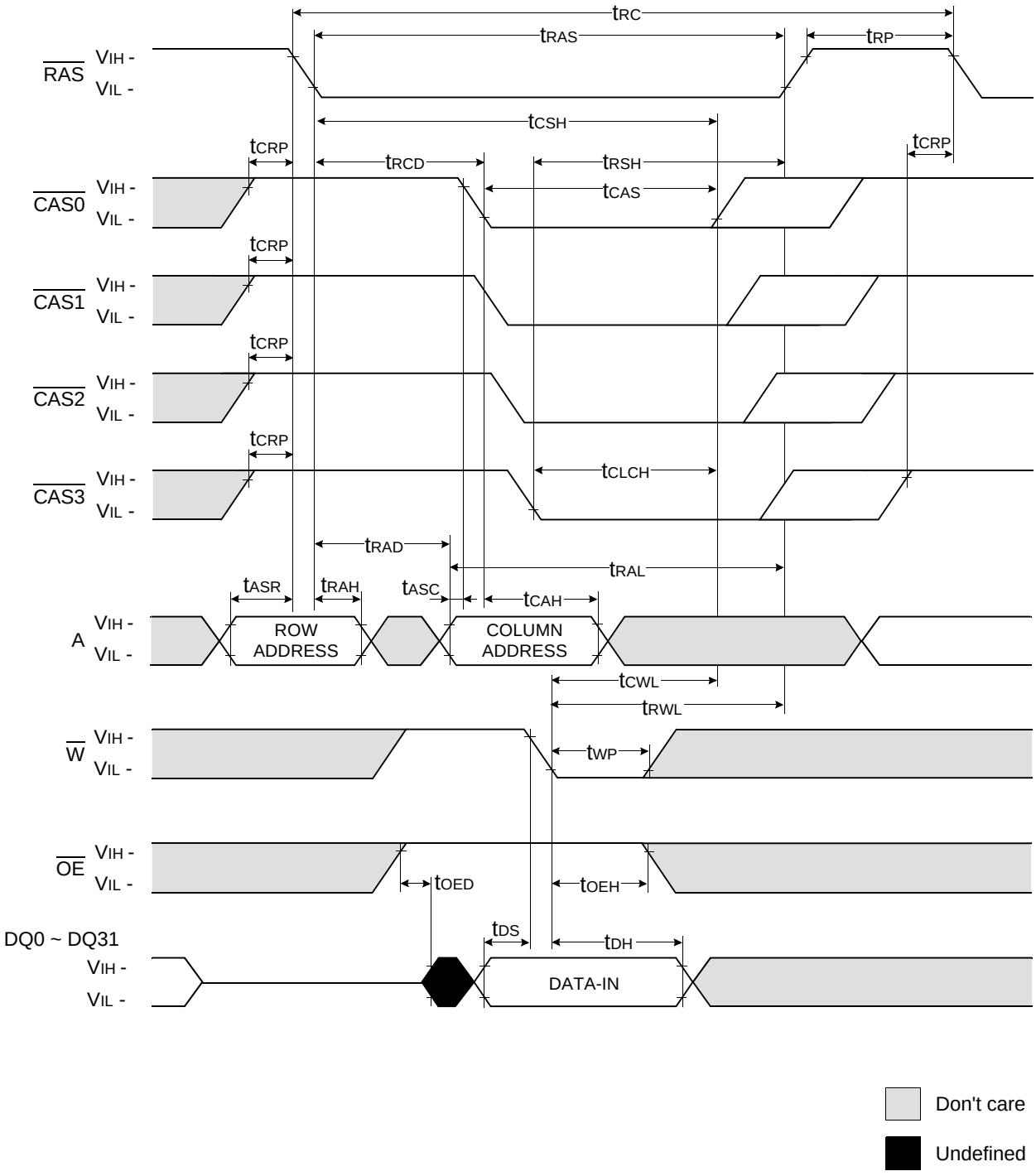
2 WORDS WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : DOUT = OPEN



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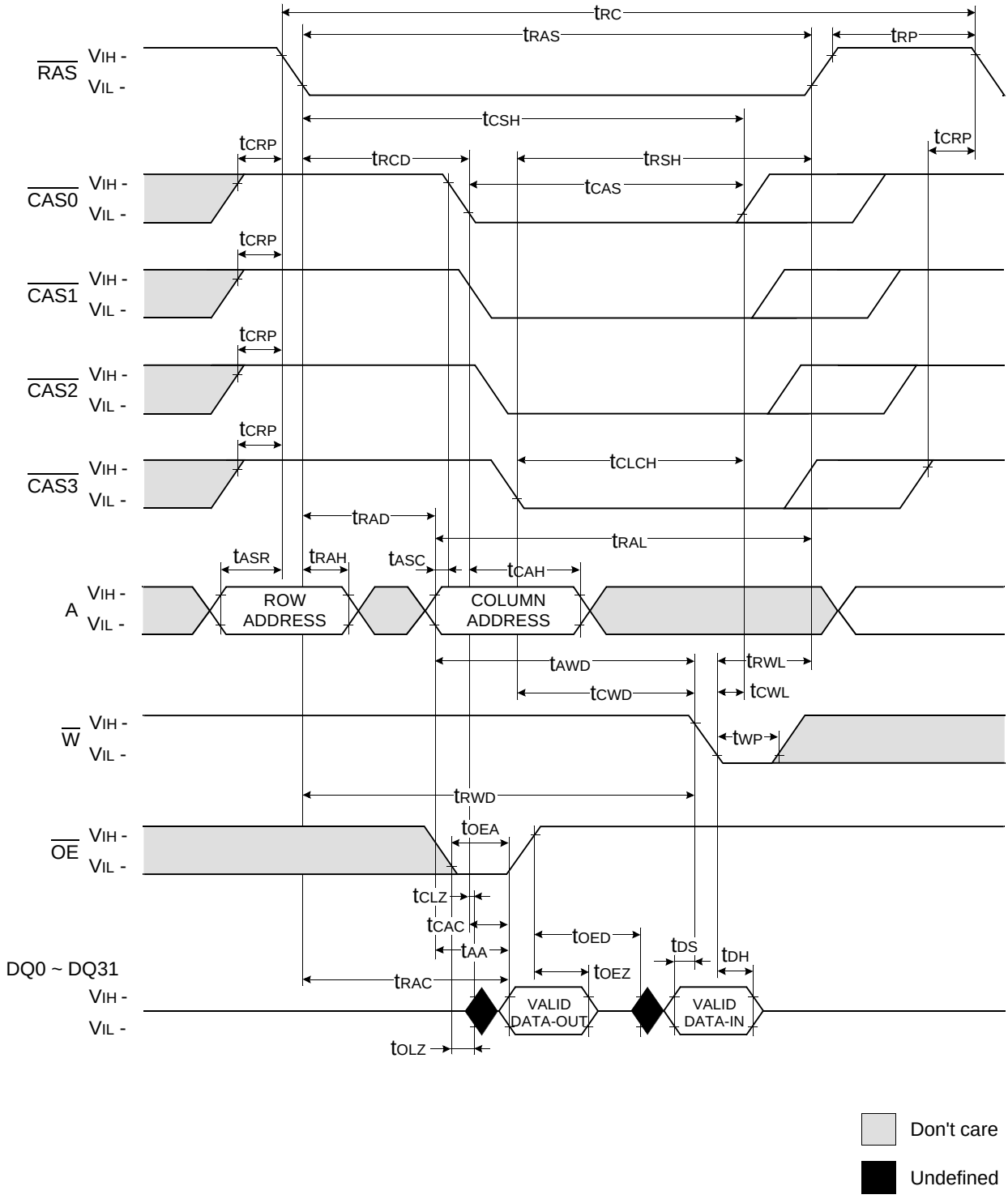
2 WORDS READ - MODIFY - WRITE CYCLE



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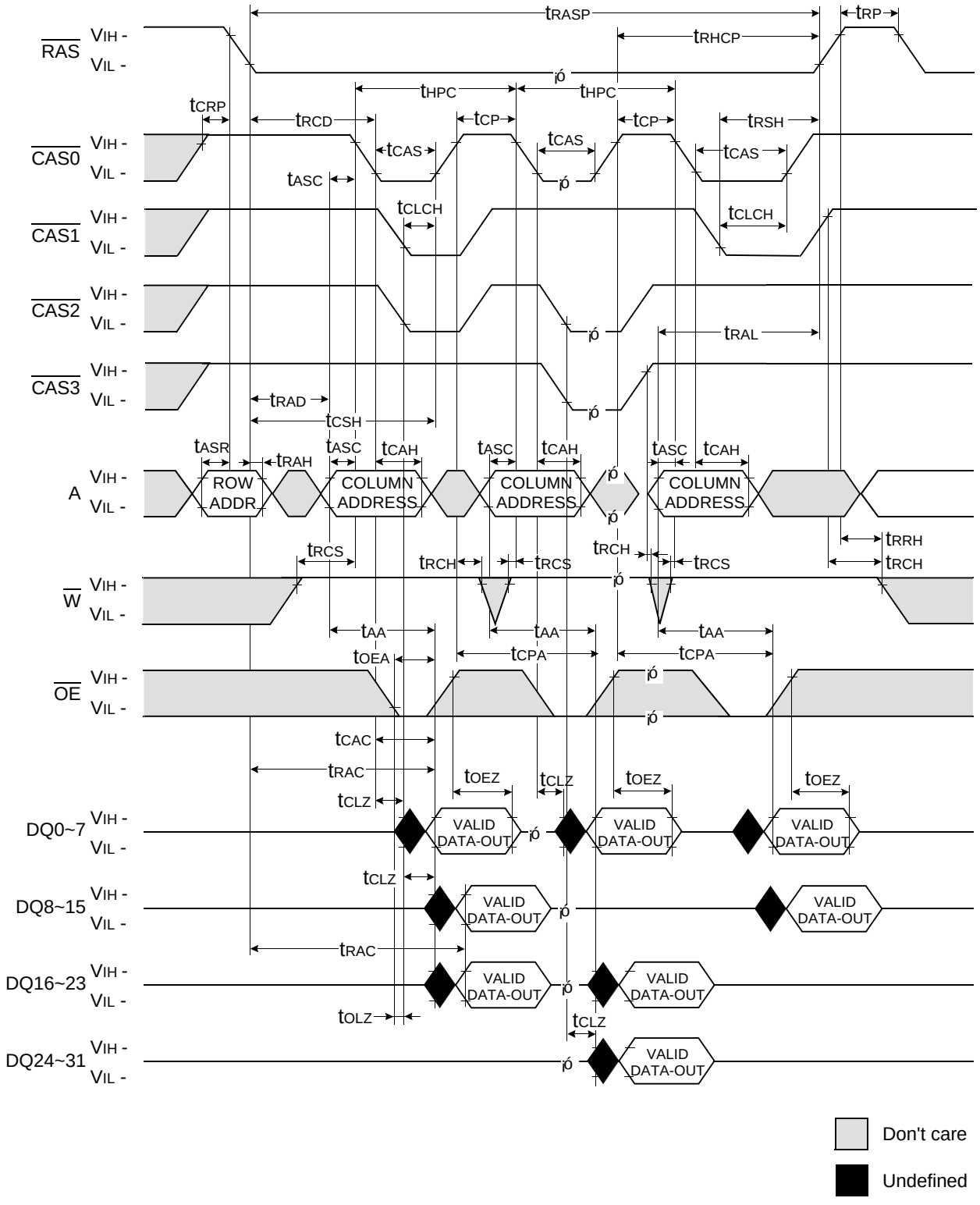
HYPER PAGE MODE READ CYCLE



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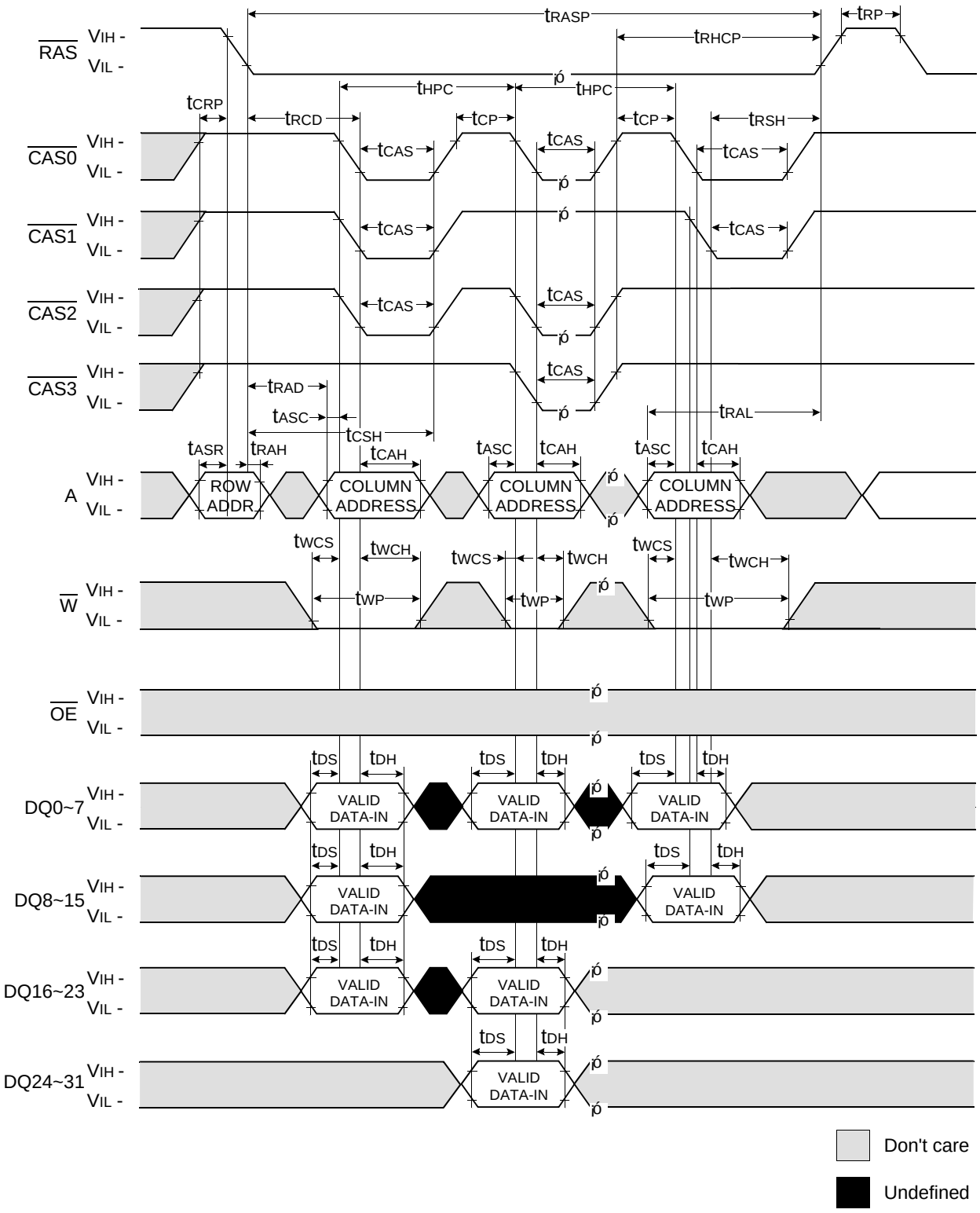
HYPER PAGE MODE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



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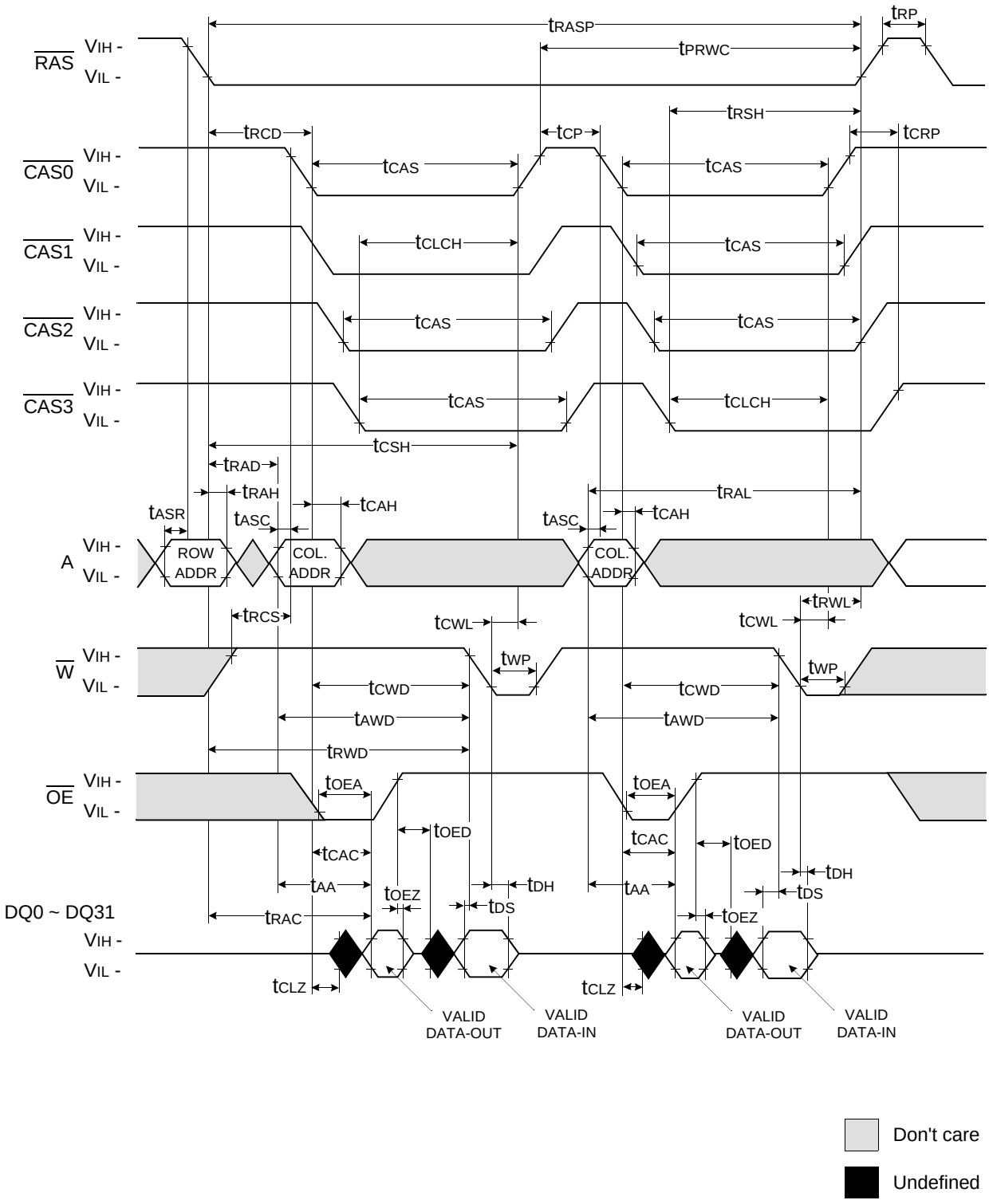
2 WORDS HYPER PAGE READ - MODIFY - WRITE CYCLE



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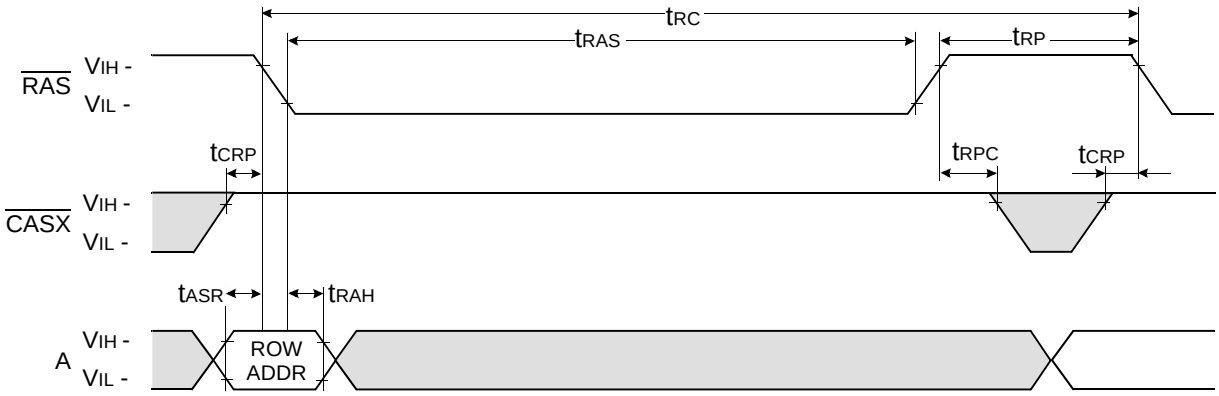
$\overline{RAS}$ - ONLY REFRESH CYCLE

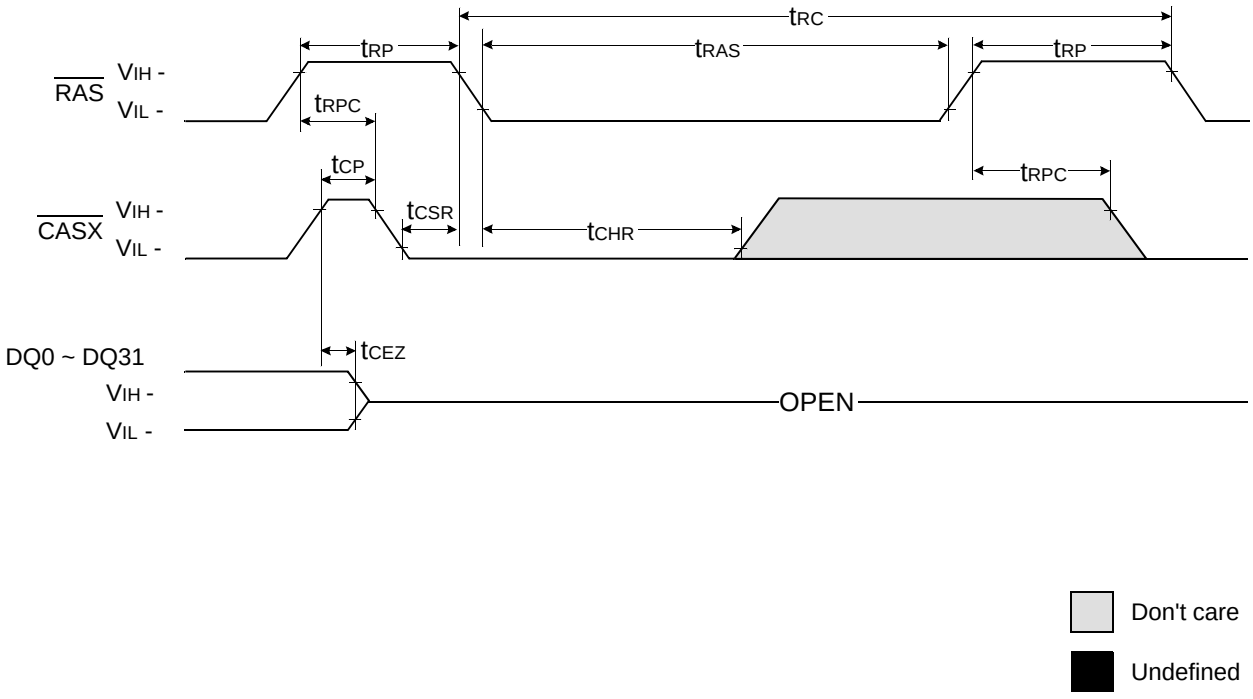
NOTE : $\overline{W}$, $\overline{OE}$, D_{IN} = Don't care

D_{OUT} = OPEN



$\overline{CAS}$ - BEFORE - $\overline{RAS}$ REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, A = Don't care



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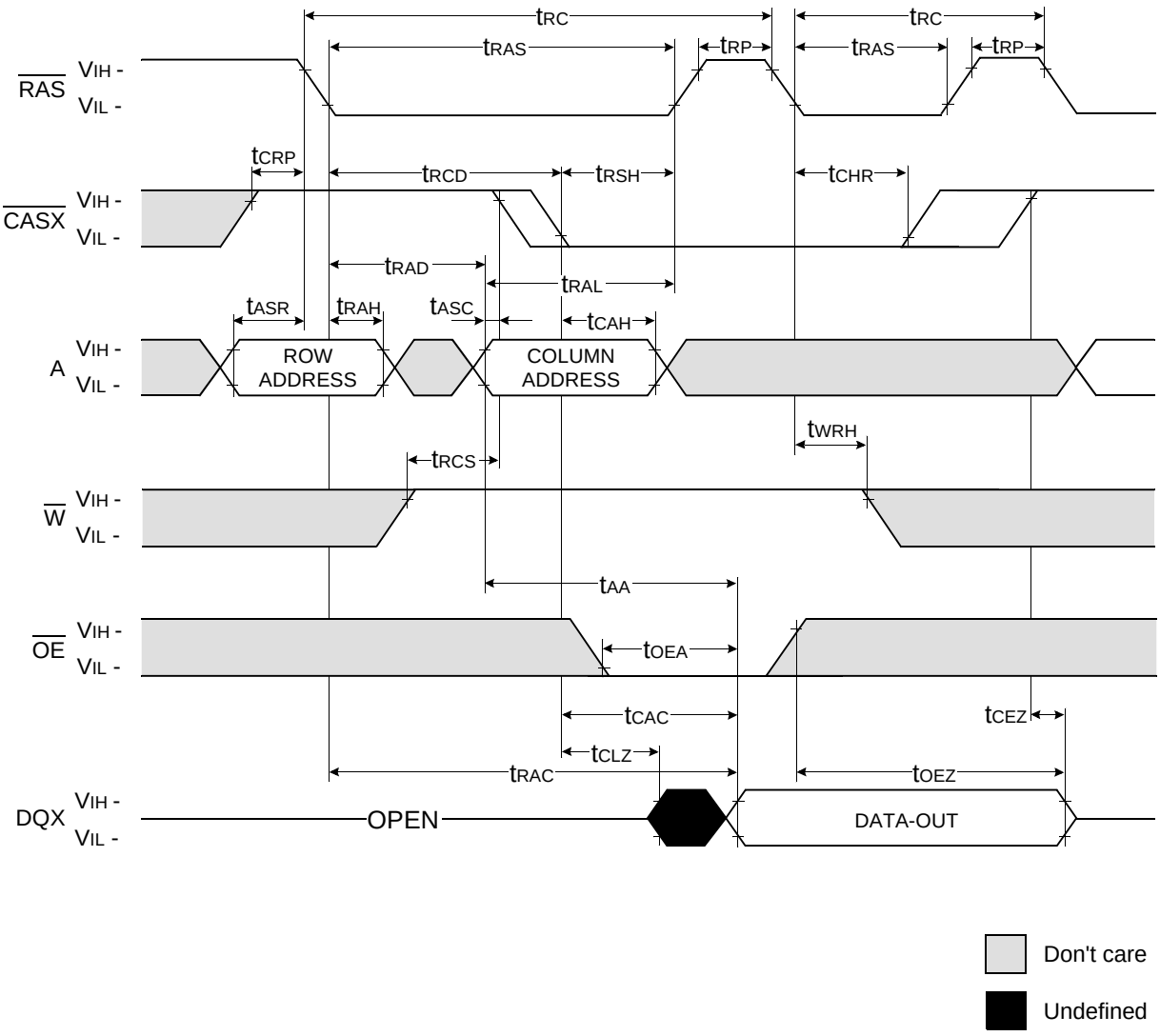
HIDDEN REFRESH CYCLE (READ)



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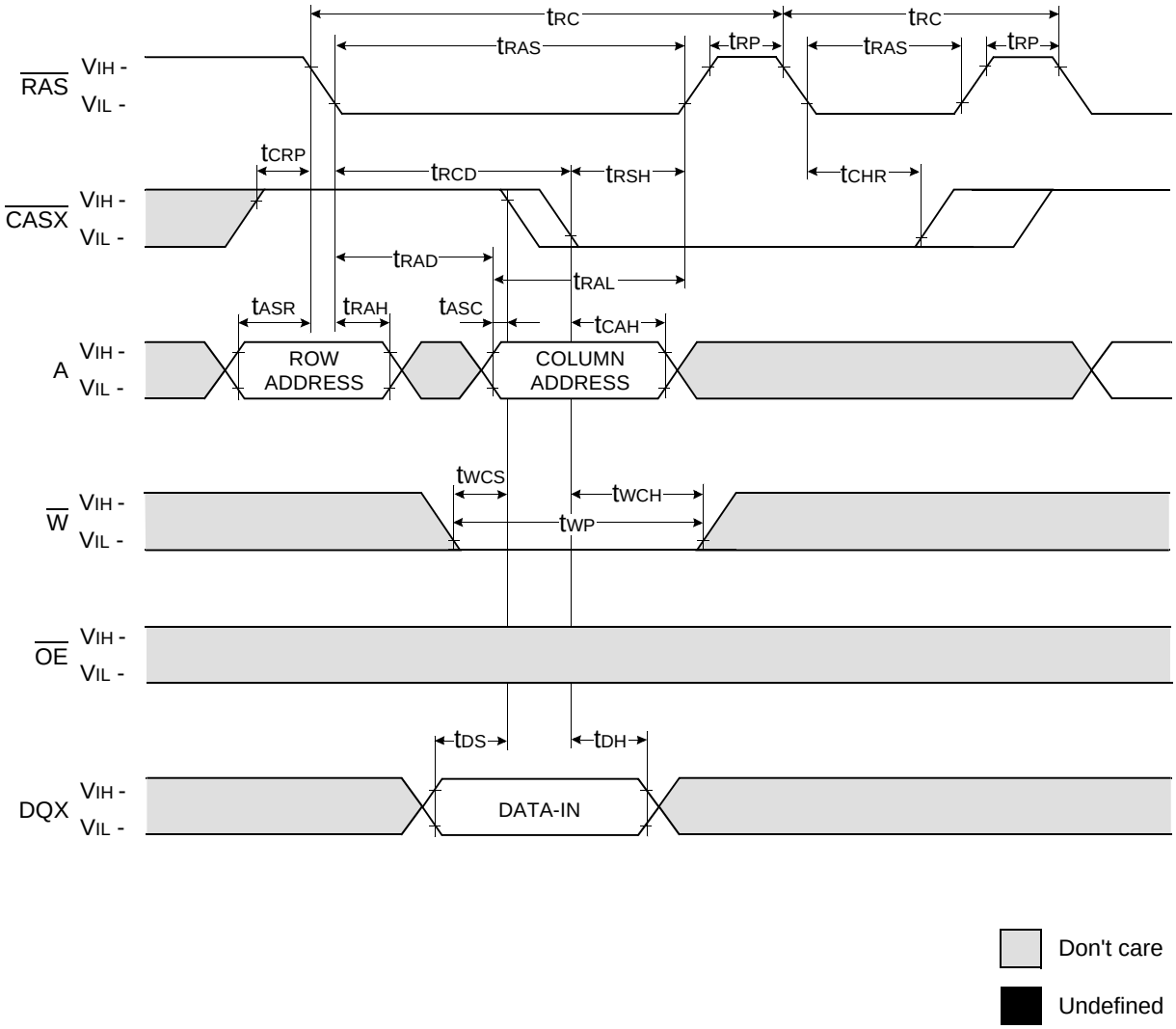
HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT = OPEN



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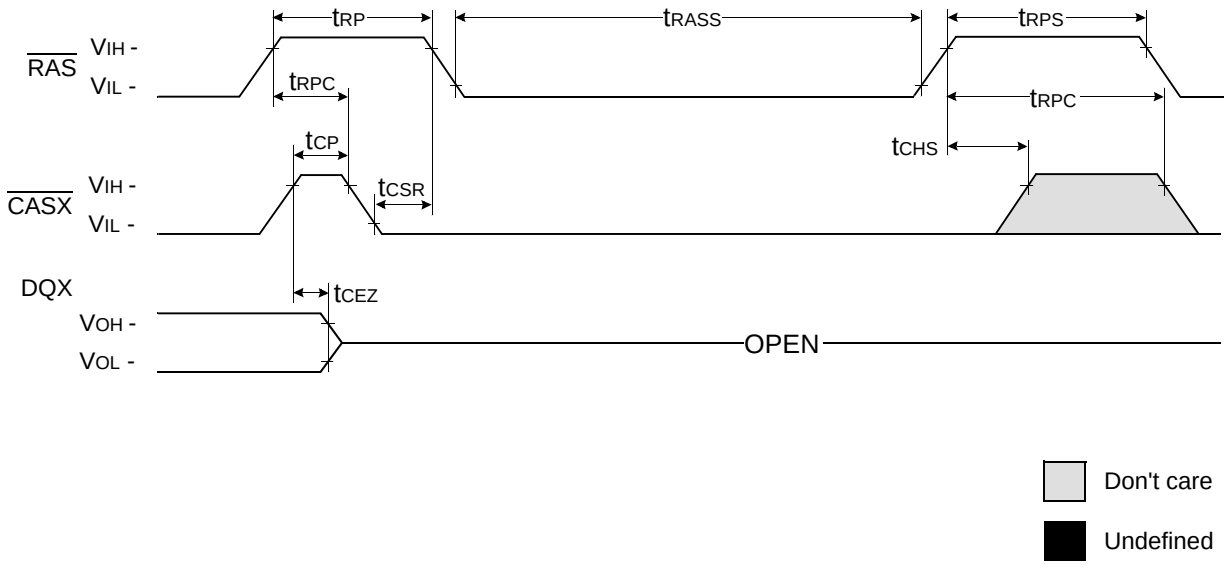
$\overline{\text{CAS}}$ - BEFORE - $\overline{\text{RAS}}$ SELF REFRESH CYCLE

NOTE : $\overline{\text{OE}}$, A = Don't care



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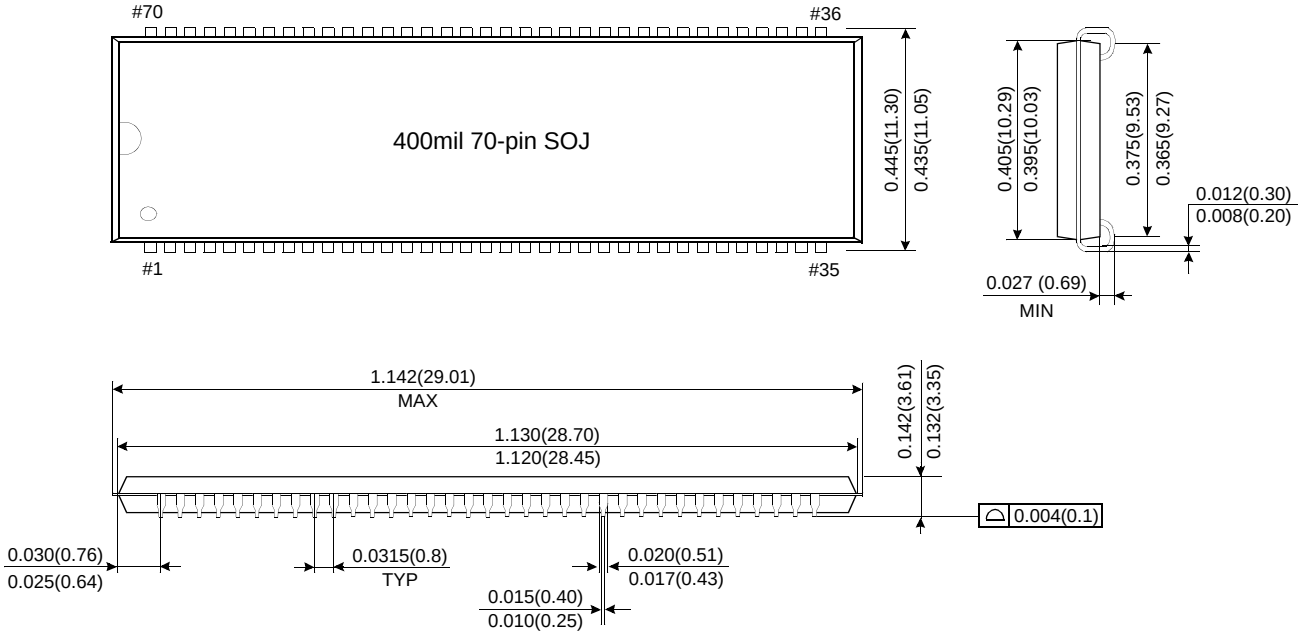
PACKAGE DIMENSIONS

Units : Inches (millimeters)



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