# μPD46710A
# 16,384 x 10-Bit x 2
# Static BiCMOS RAM

## Description

The μPD46710A is a high-performance static BiCMOS RAM organized as 16,384 x 10 bits x 2 and designed for use as a high-speed cache memory. The μPD46710A integrates two 16,384 x 10-bit SRAM cores with associated address latches and control signals that can be used to implement an instruction/data cache for 25- and 33-MHz VR3000™ RISC systems.

## Features

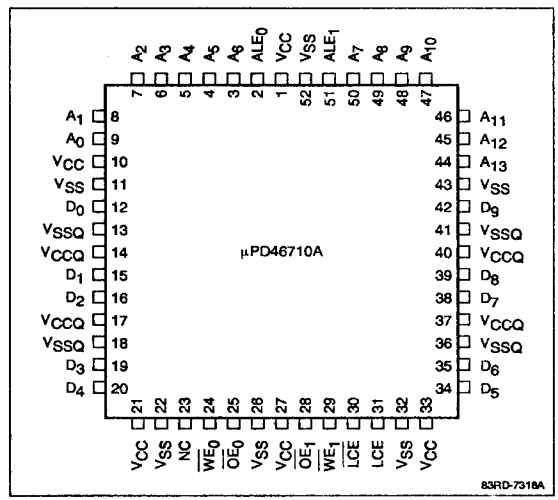
- Fast access time: 12 or 15 ns
- 16,384 x 10-bit x 2 organization
- On-chip address latches
- On-chip instruction/data caches
- Fully static read/write operation
- TTL-compatible inputs and outputs
- 52-pin PLCC package

## Ordering Information

| Part Number | Access Time | Output Enable Time | Package |
|---|---|---|---|
| μPD46710ALN-12 | 12 ns | 4.5 ns | 52-pin PLCC |
| LN-15 | 15 ns | 7 ns | |

## Pin Configuration

### *52-Pin PLCC*




## Pin Identification

| Symbol | Function |
|---|---|
| $A_0$ - $A_{13}$ | Addresses |
| $ALE_0$ and $ALE_1$ | Address latch enable inputs |
| $D_0$ - $D_9$ | Data inputs/outputs |
| LCE and $\overline{LCE}$ | Latch chip enable inputs |
| $\overline{OE}_0$ and $\overline{OE}_1$ | Output enable inputs |
| $\overline{WE}_0$ and $\overline{WE}_1$ | Write enable inputs |
| $V_{CC}$ and $V_{CCQ}$ | +5-volt power supply |
| $V_{SS}$ and $V_{SSQ}$ | Ground |
| NC | No connection |

23a

VR3000 is a trademark of NEC Corporation.

## Block Diagram

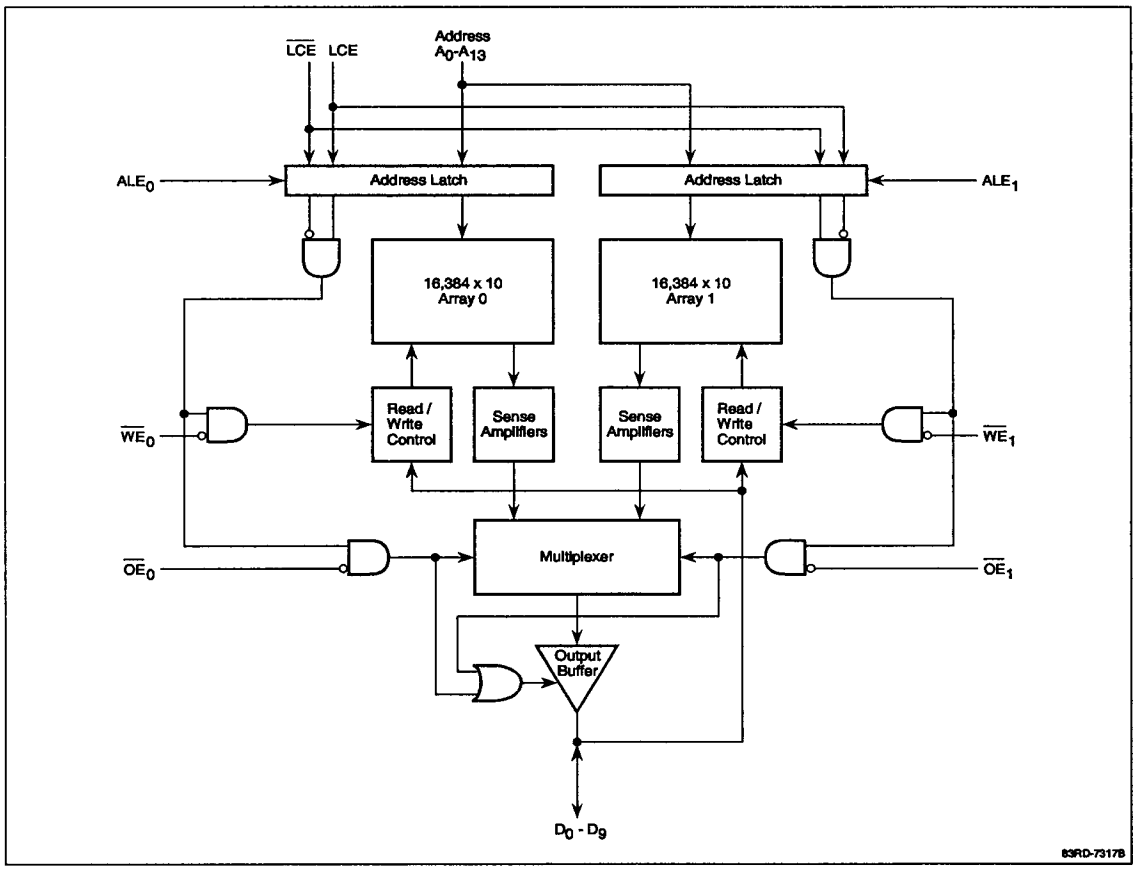
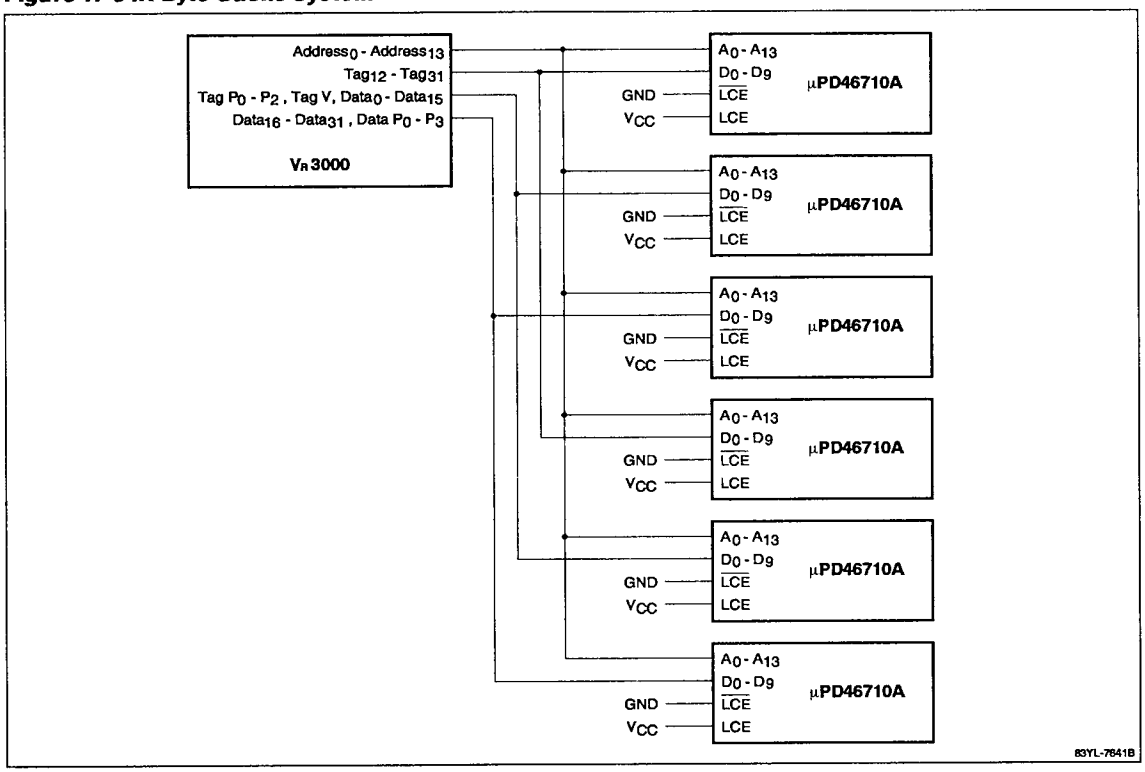


***Figure 1. 64K-Byte Cache System***




## Functional Operation

The μPD46710A integrates two 16K x 10 SRAM cores with associated address latches and control logic to be used as an instruction/data cache in a high-speed VR3000 RISC processor. In this system, the CPU initiates a μPD46710A memory cycle by outputting an address to one of the two memory arrays. The signals on address lines $A_0$ - $A_{13}$ are latched onto the address latch of array 0 at the rising edge of $ALE_0$ while $ALE_1$ is inactive low. The CPU executes a read cycle on array 0 and initiates the next memory operation. Memory array 1 is then accessed by latching the CPU address at the rising edge of $ALE_1$ with $ALE_0$ inactive low.

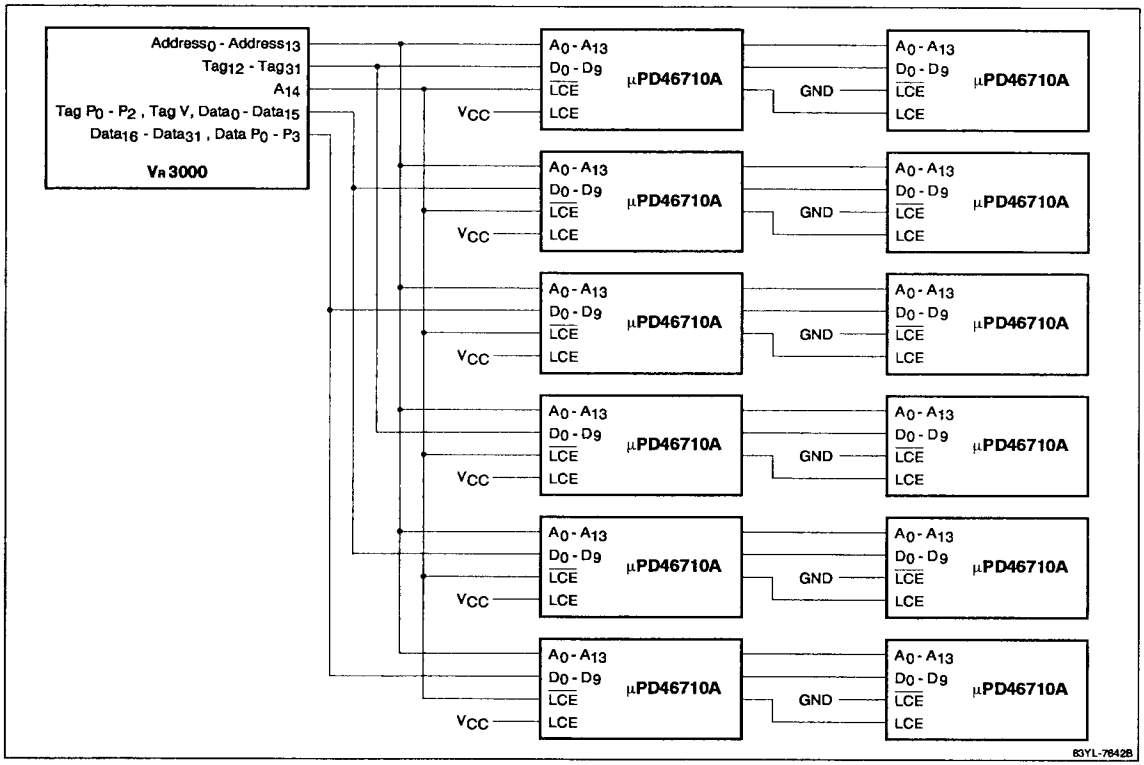
To read data from memory array 0, $\overline{OE}_0$ is driven active low while $\overline{WE}_0$, $\overline{WE}_1$, and $\overline{OE}_2$ remain inactive high. Data in memory array 1 is read by driving $\overline{OE}_1$ low with $\overline{OE}_0$, $\overline{WE}_0$, and $\overline{WE}_1$ inactive high.

The $\overline{WE}_0$ and $\overline{WE}_1$ signals control write cycles into each of the two memory arrays. Data is written into memory array 0 by driving write data on data lines $D_0$ - $D_9$ with $\overline{WE}_0$ active low. In a similar manner, the $\overline{WE}_1$ signal controls write cycles into memory array 1.

The LCE and $\overline{LCE}$ latch chip enable signals provide a decoding function that can be used to increase the size of the VR3000 cache memory. A 64K-byte cache (figure 1) can be implemented using six μPD46710As with LCE and $\overline{LCE}$ connected to $V_{CC}$ and GND, respectively.

Cache size can be increased to 128K bytes (figure 2) using two banks of six μPD46710As. In this case, address signal $A_{14}$ is used to decode the two 64K-byte memory banks. $\overline{LCE}$ of the first bank is connected to address $A_{14}$ and LCE is connected to $V_{CC}$. LCE of the second bank is connected to $A_{14}$ with $\overline{LCE}$ grounded.

*Figure 2. 128K-Byte Cache System*




## Truth Table

| Function | LCE | $\overline{LCE}$ | $\overline{WE_0}$ | $\overline{WE_1}$ | $\overline{OE_0}$ | $\overline{OE_1}$ | Output |
|---|---|---|---|---|---|---|---|
| Not selected | L | L | X | X | X | X | High-Z |
| Not selected | L | H | X | X | X | X | High-Z |
| Not selected | H | H | X | X | X | X | High-Z |
| Read RAM array 0 data | H | L | H | H | L | H | Read data |
| Read RAM array 1 data | H | L | H | H | H | L | Read data |
| Output high-Z | H | L | H | H | H | H | High-Z |
| (Note 1) | H | L | H | H | L | L | High-Z |
| Write data into RAM array 0 | H | L | L | H | X | X | Write data |
| Write data into RAM array 1 | H | L | H | L | X | X | Write data |
| Write same data into both RAM arrays. (Note 2) | H | L | L | L | X | X | Write data |

**Notes:**

(1) Not recommended for use because of multiselection in the multiplexer circuit.

(2) Not recommended for use because of increasing ac power during write operation.

(3) X = don't care.

## Absolute Maximum Ratings

| | |
|---|---|
| Supply voltage, $V_{CC}$ | −0.5 to +7.0 V |
| Input voltage, $V_{IN}$ | −0.5 to + 7.0 V |
| Output voltage, $V_{OUT}$ | −0.5 to + 7.0 V |
| Operating temperature, $T_{OPR}$ | 0 to +70°C |
| Storage temperature, $T_{STG}$ | −55 to +125°C |

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

## Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| Input voltage, high | $V_{IH}$ | 2.2 | | $V_{CC}$ + 0.3 | V |
| Input voltage, low | $V_{IL}$ | −0.5 * | | 0.8 | V |
| Ambient temperature | $T_A$ | 0 | | +70 | °C |

* $V_{IL}$ = −2.0 V min for 20-ns maximum pulse.

## Capacitance

$T_A$ = 25°C; f = 1 MHz; $V_{IN}$ and $V_{OUT}$ = 0 V

| Parameter* | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input capacitance | $C_{IN}$ | | | 6 | pF |
| Input/output capacitance | $C_{I/O}$ | | | 8 | pF |

* These parameters are sampled and not 100% tested.

## DC Characteristics

$T_A$ = 0 to +70°C; $V_{CC}$ = +5.0 V ±10%

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Input leakage current | $I_{LI}$ | −2 | | 2 | μA | $V_{IN}$ = 0 V to $V_{CC}$ |
| Output leakage current | $I_{LO}$ | −2 | | 2 | μA | $V_O$ = 0 V to $V_{CC}$ |
| Operating supply current* | $I_{CCA}$ | | | 300 | mA | $V_O$ = open; $V_{CC}$ = max; f = $2/t_{RC}$ |
| Output voltage, low | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 8 mA; $V_{CC}$ = min |
| Output voltage, high | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = −4.0 mA; $V_{CC}$ = min |

* Applicable to two SRAM cores operating at maximum frequency.

## AC Characteristics

$T_A$ = 0 to +70°C; $V_{CC}$ = +5.0 V ±10%

| | | μPD46710A-12 | | μPD46710A-15 | | | |
|---|---|---|---|---|---|---|---|
| Parameter | Symbol | Min | Max | Min | Max | Unit | Test Conditions |
| ***Read Operation*** | | | | | | | |
| Address access time | $t_{AA}$ | | 12 | | 15 | ns | |
| Address hold time for $ALE_0$ and $ALE_1$ | $t_{AHLL}$ | 2 | | 2 | | ns | (Note 3) |
| Latched chip enable access time | $t_{ALCE}$ | | 12 | | 15 | ns | |
| ALE access time | $t_{ALEA}$ | 1 | 14 | 1 | 17 | ns | |
| Address latch enable pulse width | $t_{AP}$ | 6 | | 8 | | ns | |
| Address setup time for $ALE_0$ and $ALE_1$ | $t_{ASLL}$ | 4 | | 4 | | ns | (Note 4) |
| Latched chip enable to output in high-Z | $t_{CHZ}$ | 1 | 6 | 2 | 7 | ns | (Note 1) |
| Latched chip enable to output in low-Z | $t_{CLZ}$ | 1 | | 2 | | ns | (Note 1) |
| Output enable to output valid | $t_{OE}$ | | 4.5 | | 6 | ns | (Note 5) |
| Output hold from address change | $t_{OH}$ | 3 | | 3 | | ns | |
| $\overline{OE}$ to output in high-Z | $t_{OHZ}$ | 0 | 4 | 0 | 6 | ns | (Note 1) |
| $\overline{OE}$ to output in low-Z | $t_{OLZ}$ | 0 | | 0 | | ns | |
| Output enable overlap time | $t_{OO}$ | 1 | | 1 | | ns | |
| Read cycle time | $t_{RC}$ | 15 | | 20 | | ns | |

## AC Characteristics (cont)

| Parameter | Symbol | μPD46710A-12 Min | μPD46710A-12 Max | μPD46710A-15 Min | μPD46710A-15 Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| ***Write Operation*** | | | | | | | |
| Address hold time for $ALE_0$ and $ALE_1$ | $t_{AHLL}$ | 2 | | 2 | | ns | (Note 3) |
| ALE setup time prior to end of write | $t_{ALES}$ | 2 | | 2 | | ns | |
| ALE setup time to end of write | $t_{ALEW}$ | 17 | | 17 | | ns | |
| Address latch enable pulse width | $t_{AP}$ | 6 | | 8 | | ns | |
| Address setup time | $t_{AS}$ | 2 | | 2 | | ns | |
| Address setup time for $ALE_0$ and $ALE_1$ | $t_{ASLL}$ | 4 | | 4 | | ns | (Note 4) |
| Address valid to end of write | $t_{AW}$ | 12 | | 15 | | ns | |
| Address latch enable hold time after write | $t_{AWH}$ | 0 | | 0 | | ns | |
| Latched chip enable to end of write | $t_{CW}$ | 12 | | 15 | | ns | |
| Data hold time | $t_{DH}$ | 0 | | 0 | | ns | (Note 8) |
| Data valid to end of write | $t_{DW}$ | 5 | | 7 | | ns | (Note 7) |
| Output enable to end of write | $t_{OEW}$ | 0 | | 0 | | ns | (Note 6) |
| Output disable to write enable | $t_{ODW}$ | 2 | | 2 | | ns | |
| Write cycle time | $t_{WC}$ | 12 | | 15 | | ns | |
| Write pulse width | $t_{WP}$ | 7 | | 10 | | ns | |
| Write recovery time | $t_{WR}$ | 2 | | 3 | | ns | |

**Notes:**

(1) This transition is measured ±200 mV from steady-state with the output load in figure 3.

(2) Input pulse levels = 0.8 to 2.4 V; input pulse rise and fall times ≤ 3 ns; see figure 3.

(3) $t_{AHLL}$ = 1.5 ns for $V_{CC}$ = +5 V ±5%, $T_A$ = 0 to 50°C.

(4) $t_{ASLL}$ = 3 ns for $V_{CC}$ = +5 V ±5%, $T_A$ = 0 to 50°C.

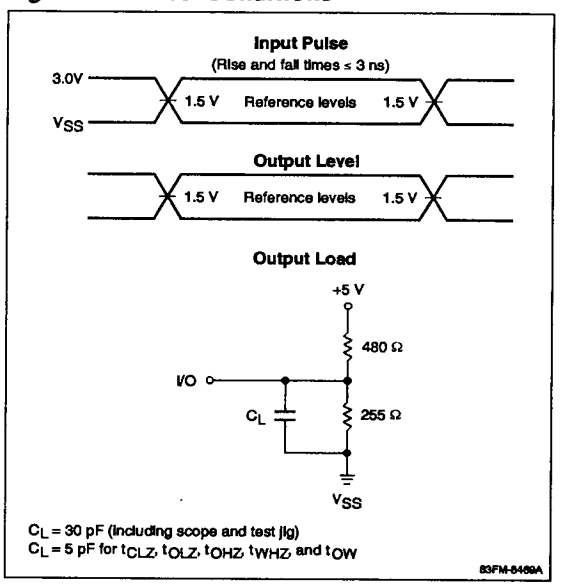
(5) $t_{OE}$ = 4 ns for $V_{CC}$ = +5 V ±5%, $T_A$ = 0 to 50°C.

(6) $\overline{OE}_n$, $\overline{WE}_m$ (n = 0 or 1, m = 0 or 1)
$t_{OEW}$ = 0 ns min at n ≠ m
= 2 ns min at n = m

(7) $t_{DW}$ = 4 ns for $V_{CC}$ = +5 V ±5%, $T_A$ = 0 to 50°C.

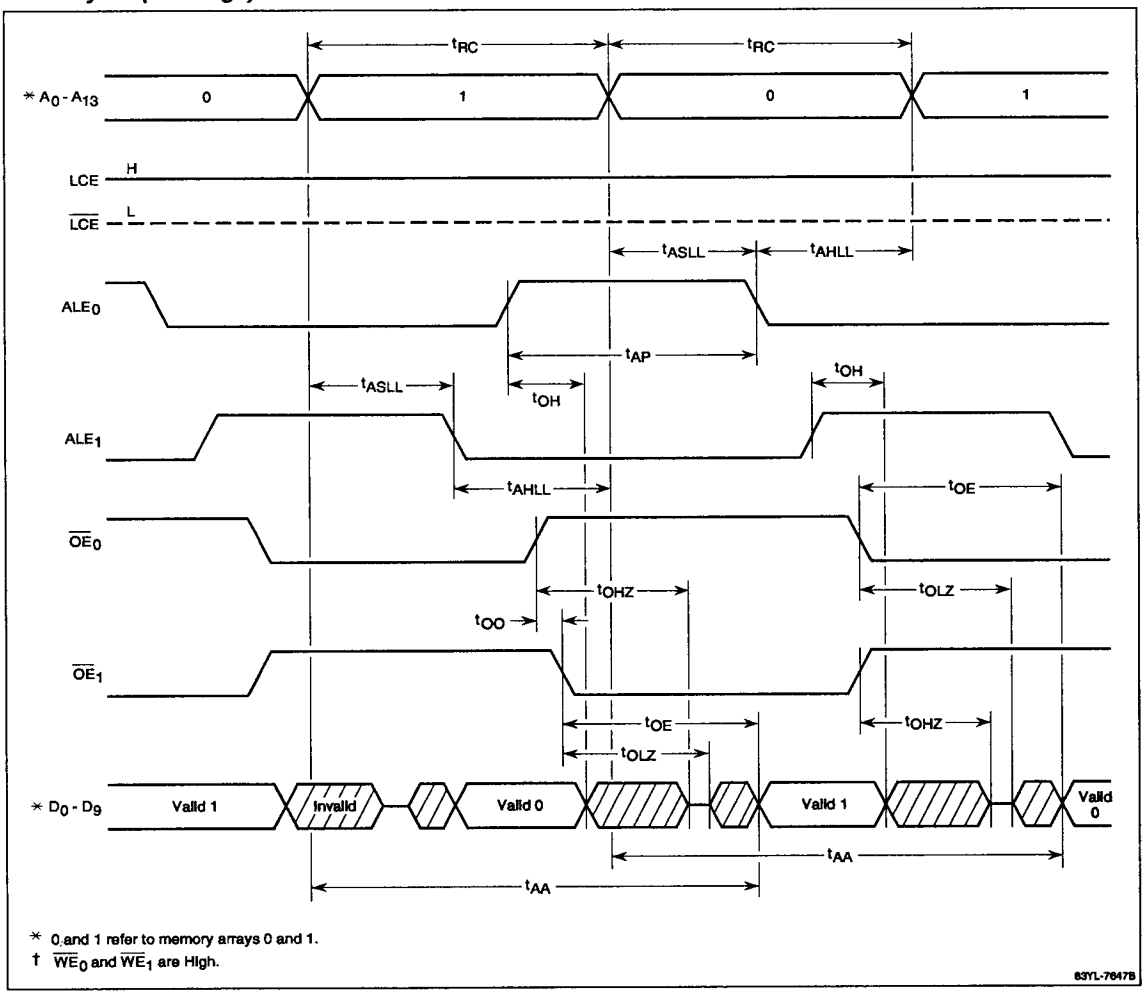
(8) $t_{DH}$ = 0.5 ns for $V_{CC}$ = +5 V ±5%, $T_A$ = 0 to 50°C.

***Figure 3. AC Test Conditions***



## Timing Waveforms

### *Read Cycle (LCE High)*




* 0 and 1 refer to memory arrays 0 and 1.
† $\overline{WE}_0$ and $\overline{WE}_1$ are High.

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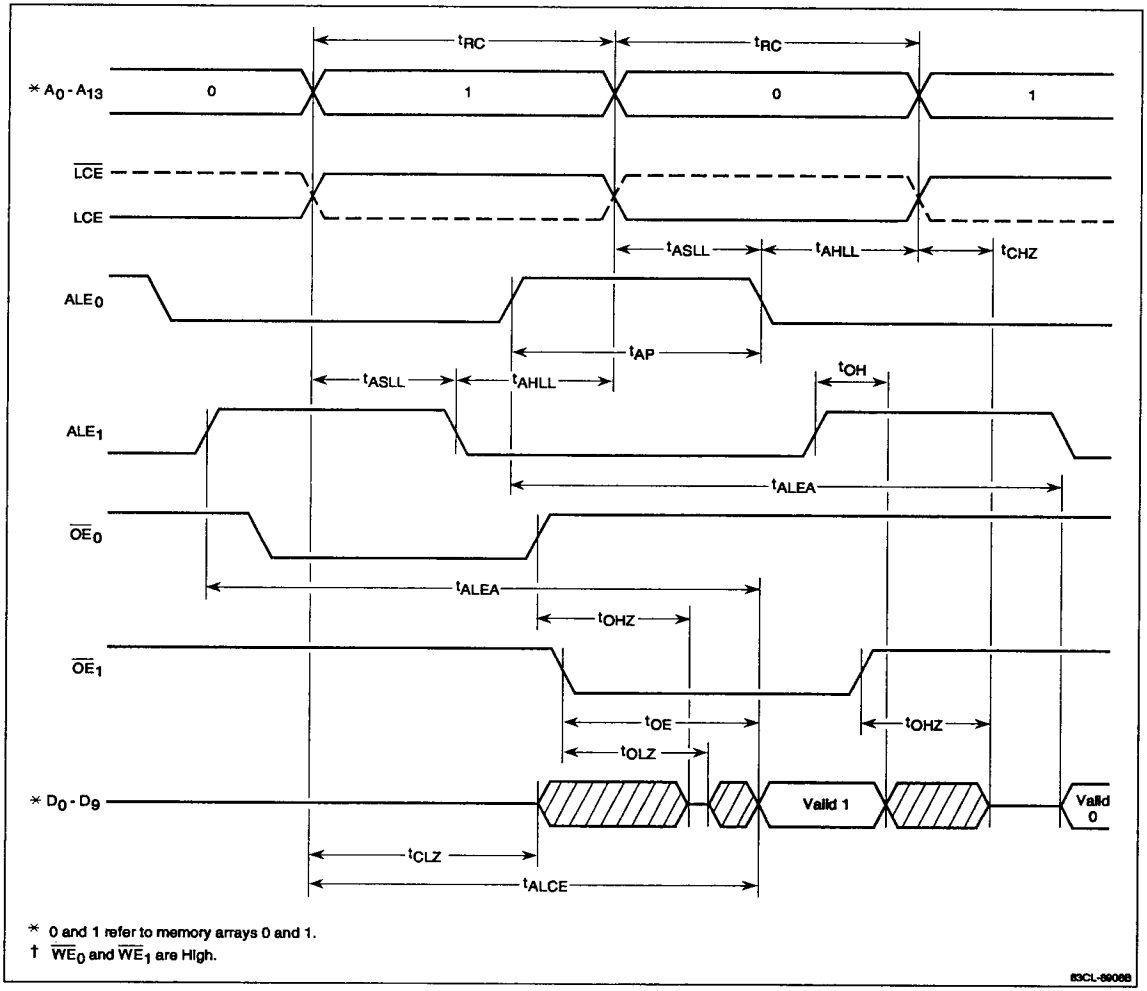
## Timing Waveforms (cont)

***Read Cycle (LCE = Address)***




* 0 and 1 refer to memory arrays 0 and 1.
† $\overline{WE_0}$ and $\overline{WE_1}$ are High.

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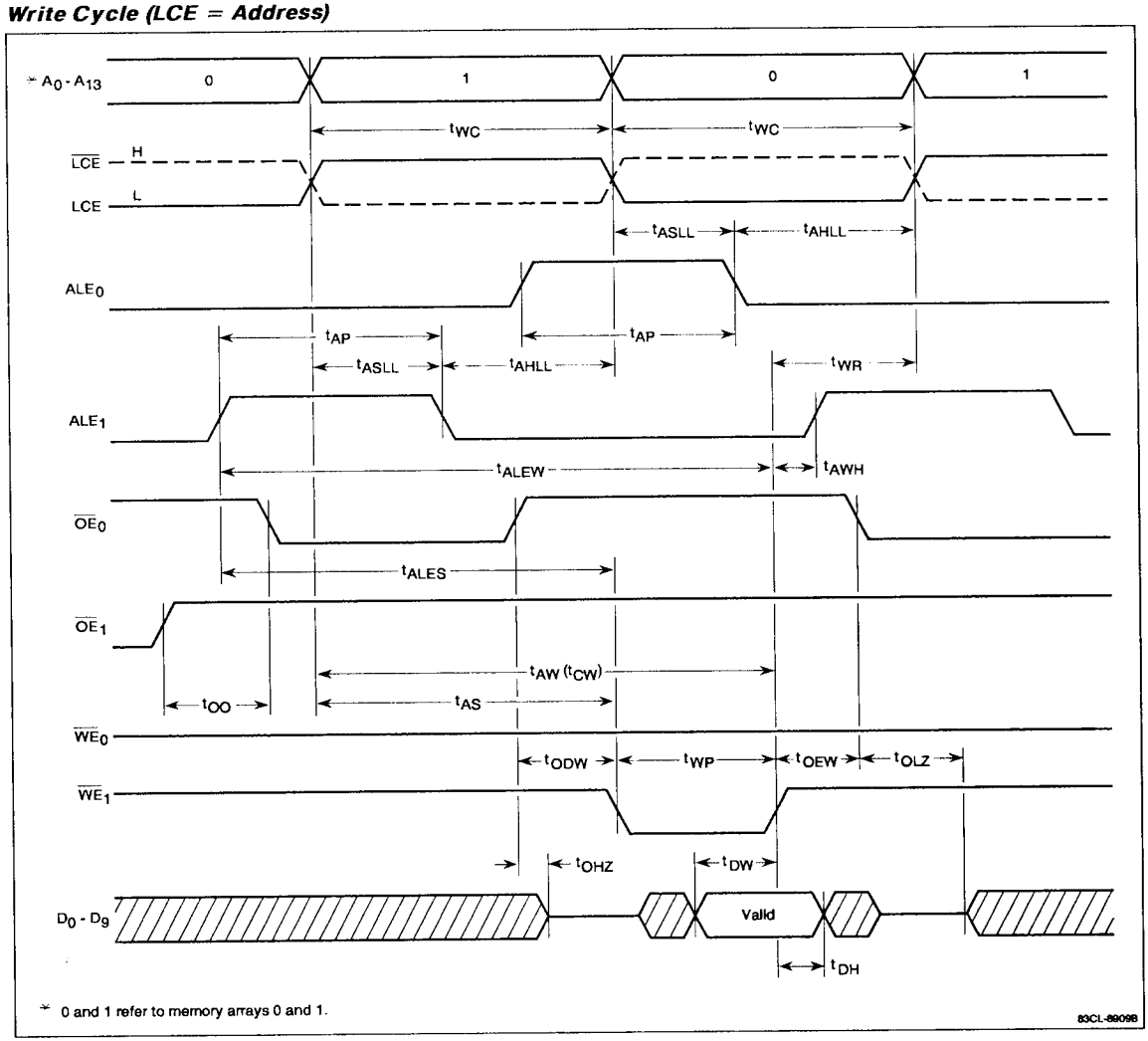
## Timing Waveforms (cont)

***Write Cycle (LCE = Address)***

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