GEC PLESSEY
SEMICONDUCTORS

APRIL 1996

ADVANCE INFORMATION

DS4367 1.3

PCA873F

HIGH SPEED COPPER MEDIA 100 BASE Tx TRANSCEIVER DEVICE

The PCA873F is a transceiver device for use with category 5 unshielded twisted pair (UTP) and type 1 shielded twisted pair (STP) operating with data rates of 100/155 Mbit/s.

The device is aimed at dual 10/100Mb/s Ethernet applications with Auto Negotiation. The PCA873F may also be used for ATM, FDDI and Fast Ethernet applications.

To enable Auto Negotiation to function in some 10/100 Mb/s applications the PCA873F has its receive side continuously enabled so as the system can have full visibility of any 100Mb/s link pulses received whilst in 10mb/s mode.

An important feature of the device is a Quantized Feedback circuit which overcomes the "baseline wander" associated with the MLT-3 and NRZ codes and consequently, maintains the signal noise immunity.

The PCA873F is fabricated using the GEC Plessey Semiconductors' complementary high performance bipolar array technology.

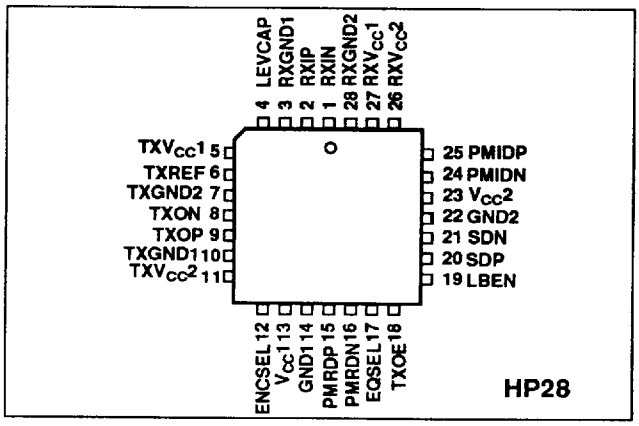


Fig.1 Pin connections - top view

FEATURES

- Complies with ANSI X 3T9.5 TP-PMD Draft standards
- Operates over 100 meters STP and category 5 UTP
- Quantized feedback circuit to overcome "baseline wander"
- Adaptive equalization
- Programmable TX output current
- Low voltage shutdown of TX output
- Tristatable TX outputs for dual 10Mb/s and 100Mb/s ETHERNET applications
- Permanent receive during tristate to allow Auto Negotiation with fixed 100Mb/s cards
- Single +5 V supply
- 28 pin Plastic Leaded Chip Carrier (PLCC)

ORDERING INFORMATION

PCA873F/CG/HPAS

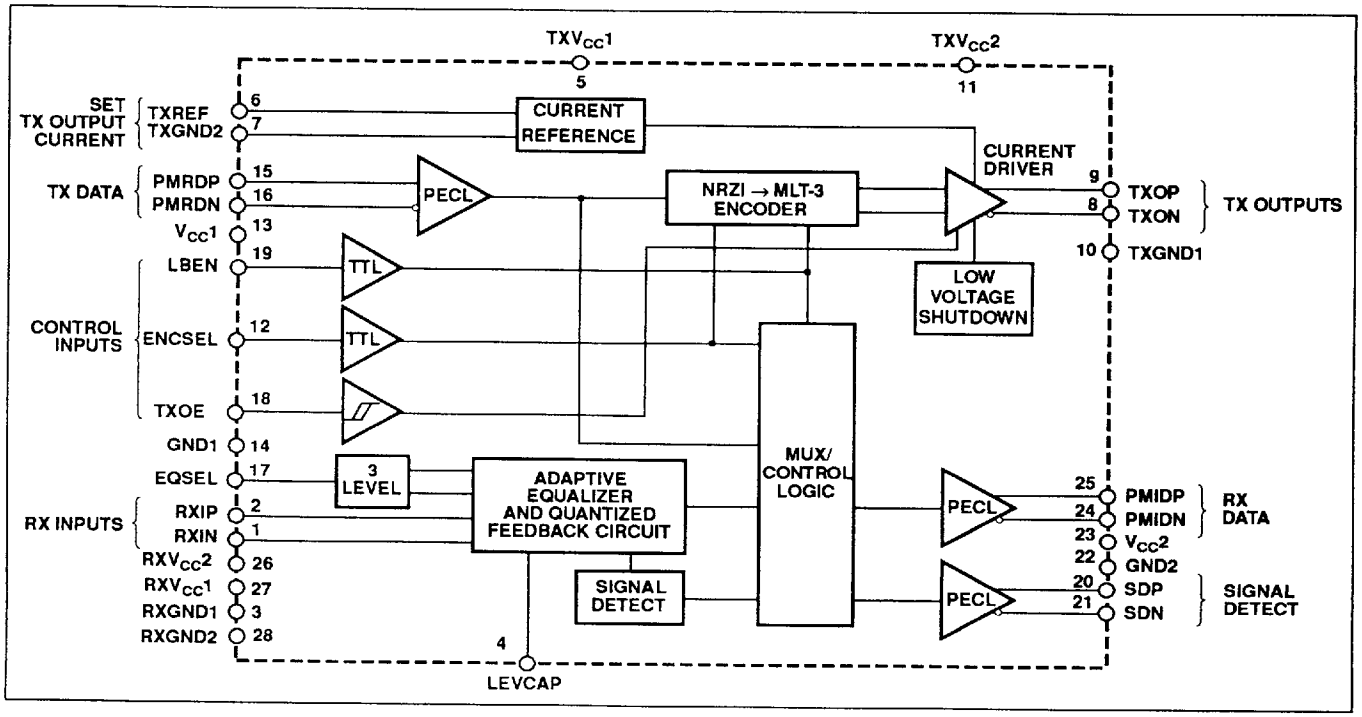


Fig.2 System block diagram

ABSOLUTE MAXIMUM RATINGS

Operation at absolute max. ratings is not implied. Exposure to stresses outside those listed could cause permanent damage to the device.

DC Supply voltage (V_{CC})	-0.5 to +7V
Storage temperature (tst)	-65 to +150°C
ESD	T.B.D.

RECOMMENDED OPERATING CONDITIONS

DC supply voltages (V_{CC})	+5V ±5%
Operating temperature (T_A)	0°C to +70°C (+25°C typ.)
Power dissipation (P_D)	575mW (typ.)

ELECTRICAL CHARACTERISTICS

Recommended operating conditions apply except where stated.

Characteristic	Symbol	Value Min.	Value Typ.	Value Max.	Units	Conditions
DC characteristics						
V_{CC} supply current	I_{CC}	-	115	-	mA	no load
TTL high level I/P	V_{IH}	2	-	-	V	
TTL low level I/P	V_{IL}	-	-	0.8	V	
Schmitt high level	V_{IH}	3.7	-	-	V	
Schmitt low level	V_{IL}	-	-	1.5	V	
EQSEL high level I/P	V_{IH}	4.2	-	-	V	
EQSEL low level I/P	V_{IL}	-	-	0.8	V	
EQSEL floating level I/P	V_{IZ}	-	$V_{CC}/2$	-	V	
PECL high level I/P		3.8	-	V_{CC}-0.5	V	
PECL low level I/P		-	-	3.6	V	
PECL high level O/P		-	V_{CC}-0.9	-	V	
PECL low level O/P		-	V_{CC}-1.75	3.5	V	
TTL high level I/P current	I_{IH}	-	-	10	µA	$V_{IH} = V_{CC}$
TTL low level I/P current	I_{IL}	-	-	-400	µA	$V_{IL} = 0V$
Schmitt high level I/P current	I_{IH}	-	-	10	µA	$V_{IH} = V_{CC}$
Schmitt low level I/P current	I_{IL}	-	-	±10	µA	$V_{IL} = 0V$
EQSEL high level I/P current	I_{IH}	-	-	1400	µA	$V_{IH} = V_{CC}$
EQSEL low level I/P current	I_{IL}	-	-	-1400	µA	$V_{IL} = 0V$
Transmit O/P current		-	40	-	mA	R_{REF} = 1.2kΩ (MLT-3)
pins TXOP, TXON		-	20	-	mA	R_{REF} = 1.2kΩ (NRZ)
Differential RX I/P signal voltage MLT-3		-	1.4	-	Vp-p	measured on device pins 1,2
Differential RX I/P signal voltage NRZ		-	0.7	-	Vp-p	measured on device pins 1,2
RX I/P common mode voltage		-	$V_{CC}/2$	-	V	RX I/Ps floating
RX I/P impedance			24		kΩ	
Signal detect threshold	V_{TH}	-	50	-	%	wrt normalized output of equalizer (Fig. 3)
AC characteristics						
TX driver outputs rise/fall times pins TXOP, TXON	t_{TXr} t_{TXf}	-	2.5	-	ns	50Ω load
Transmit propagation delay PMRD to TXO	t_{TXpd}	-	10	-	ns	
Receive propagation delay RXI to PMID	t_{RXpd}	-	12	-	ns	MLT-3 or NRZ input
Total Peak to Peak Jitter including Transmitter Cable and Receiver	-	-	2.5	-	ns	

FUNCTIONAL DESCRIPTION

The functional blocks within the device are shown in Fig. 2 These are described below:-

Transmit Section

NRZ or NRZI input data is applied to the 'PMRD' PECL inputs and passed via the NRZI→MLT-3 encoder and current driver to the 'TXO' outputs.

Encoder

The encoder operation is controlled by the state of the 'ENCSEL' pin.

When 'ENCSEL' is high, the NRZ data is passed unencoded to the 'TXO' outputs.

When 'ENCSEL' is low, the NRZI data is converted to a three level MLT-3 format at the 'TXO' outputs.

Note: In FDDI applications NRZI would be the binary format at the PHY interface with the PCA873F whereas for ATM applications NRZ would be used. The use of NRZ or NRZI is transparent to internal circuits employed within the device.

TXO Outputs

These are differential current source outputs with programmable sink capability, each designed to drive a nominal output impedance of 50Ω.

Output current is set by the value of an external resistor (R_{REF}) between pin 'TXREF' and 'TXGND2'.

This resistor defines an internal reference current derived from an on-chip bandgap reference.

Final output current at the 'TXO' outputs is a multiple of this current and is defined as:-

$$I_{TXO}(mA) = 26/R_{REF}(k\Omega) \text{ -NRZ mode}$$
$$I_{TXO}(mA) = 52/R_{REF}(k\Omega) \text{ -MLT-3 mode}$$

The TXO outputs can be tristated by taking the TXOE pin high. This feature is useful when the output is to be overdriven such as in dual 10Mb/s and 100Mb/s applications. Transition times of the 'TXO' outputs are matched and internally limited to approx. 2.5ns to reduce EMI emissions.

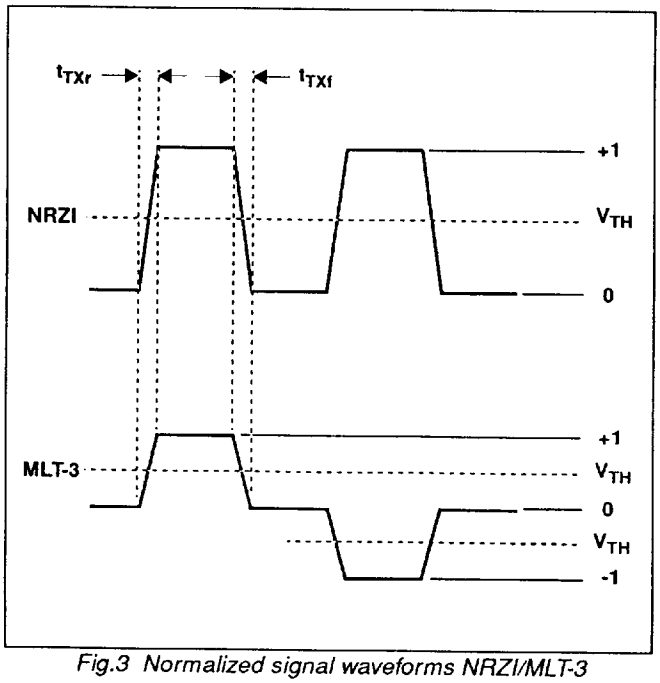


Fig.3 Normalized signal waveforms NRZI/MLT-3

Fig.3 shows the normalised waveforms to be seen at the TX outputs. A low voltage shutdown circuit turns off the TX outputs when system V_{CC} voltage falls to a level below the specified minimum.

Receiver Section

This comprises a multi-mode adaptive equalizer, a signal detect circuit and a quantized feedback block.

The recovered data is passed via the 'MUX/CONTROL LOGIC' block, to the PMID outputs.

Input data may be in either two level NRZ format, or three level MLT-3 format, as selected by the state of the 'ENCSEL' pin. (High = NRZ: LOW = MLT-3)

Equalizer

The equalizer circuit is necessary to compensate for signal degradation due to cable losses, however over-equalization must be avoided to prevent excessive overshoots resulting in errors during the reception of MLT-3 data. Three operating modes are therefore provided.

These three operating modes are controlled by the state of tristate input 'EQSEL' and are described below:-

1) Auto Equalization ('EQSEL' floating)

Fully automatic equalization is achieved through the use of a feedback loop driven by a control signal derived from the signal amplitude. This provides adaptive control and prevents over-modulation of the signal when short cable lengths are used.

2) Full Equalization ('EQSEL' low)

In this mode, full equalization is applied to the input signal irrespective of amplitude.

3) No Equalization ('EQSEL' high)

The equalization is disabled completely when EQSEL is high causing the received data signal to pass through the equalizer with no correction being performed on it.

Signal Detector

A high level is produced on the 'SD' output when the input signal on the 'RX' inputs exceeds the required minimum for reliable operation. The 'SD' output is forced high irrespective of input signal amplitude during loopback mode (see later section on Loopback).

Quantized Feedback Circuit

The MLT-3 and NRZ codes have significant low frequency components in their spectrum, which are not transmitted through the transformers that couple the line to the board. This results in 'Base Line Wander', which can reduce the noise immunity of the receiver significantly.

The purpose of the quantized feedback circuit is to restore these low frequency components through the use of a feedback arrangement. The circuit will also correct any DC offset that may exist on the received signal.

The quantized feedback circuit generates both NRZ and MLT-3 outputs. The appropriate output and feedback signal are selected by the state of the 'ENCSEL' pin.

Control Functions

In addition to the encoding and equalization selection functions, the device also provides a loopback facility and supports external cable detection circuits (wire fault). These functions are described below:-

Loopback

Pin 'LBEN' controls loopback operation.

A low level on this pin defines normal operation, a high level defines loopback mode.

In loopback mode, the 'PMRD' inputs are internally routed to the 'PMID' outputs, 'SD' is forced high and the TXOP and TXON outputs are disabled.

Output Enable

This function is controlled by pin 'TXOE'

A low level on this pin defines normal operation, a high level defines tristate mode.

In tristate mode, data transmission is inhibited and the TXOP and TXON forced into tristate.

INTERFACING TO THE TWISTED PAIR (TP) MEDIA

The PCA873F requires transmit and receive magnetics to couple to the copper media.

Listed below are four Magnetic Manufacturers and their recommended parts for use on the 155Mbps ATM and 100Base-TX standards:

VENDOR	PART No
Bel Magnetics	S558-5999-02
Nano Pulse	NPI 6121-30
Pulse	PE-68511
Valor	ST 6022

Application Note ref. AN4078 is available giving a more detailed technical note on the design issues relating to transceivers for transmission over UTP cables.

Please contact each magnetics vendor for the latest detailed component part numbers.

JITTER CHARACTERISTICS

TX Side

The jitter performance of the transmit side is illustrated in Fig.5 for NRZI and Fig.6 for MLT-3. The PCA873F was driven with a differential PECL signal on pins PMRDP and PMRDN with the TX output waveform monitored on the cable side of the magnetics. It can be seen from the plots that there is no significant jitter introduced by the TX stage.

RX Side

For the receive side the jitter performance is demonstrated in Fig.7 for NRZI and Fig.8 for MLT-3. The measurements were made using a PCA873F interfacing to 100m of Cat 5 UTP cable fitted with RJ45 connectors and via a Pulse Engineering PE-68511 magnetics module. The FDDI defined Killer Packet was used for data and was run at 125Mb/s in MLT-3 mode and 155Mb/s in NRZ mode. The eye diagrams were extracted at the PMIDP and PMIDN differential PECL outputs. The PCA873F was set for auto Equalisation (EQSEL floating) and used the external components shown in Fig.4. The jitter figures are the total for the internal circuits including the Adaptive Equalizer, Quantized Feedback and, in the case of MLT-3, the MLT-3 to NRZI decoder. As the test was made with a PCA873F driving the cable the figure is in effect inclusive of the transmitter side jitter.

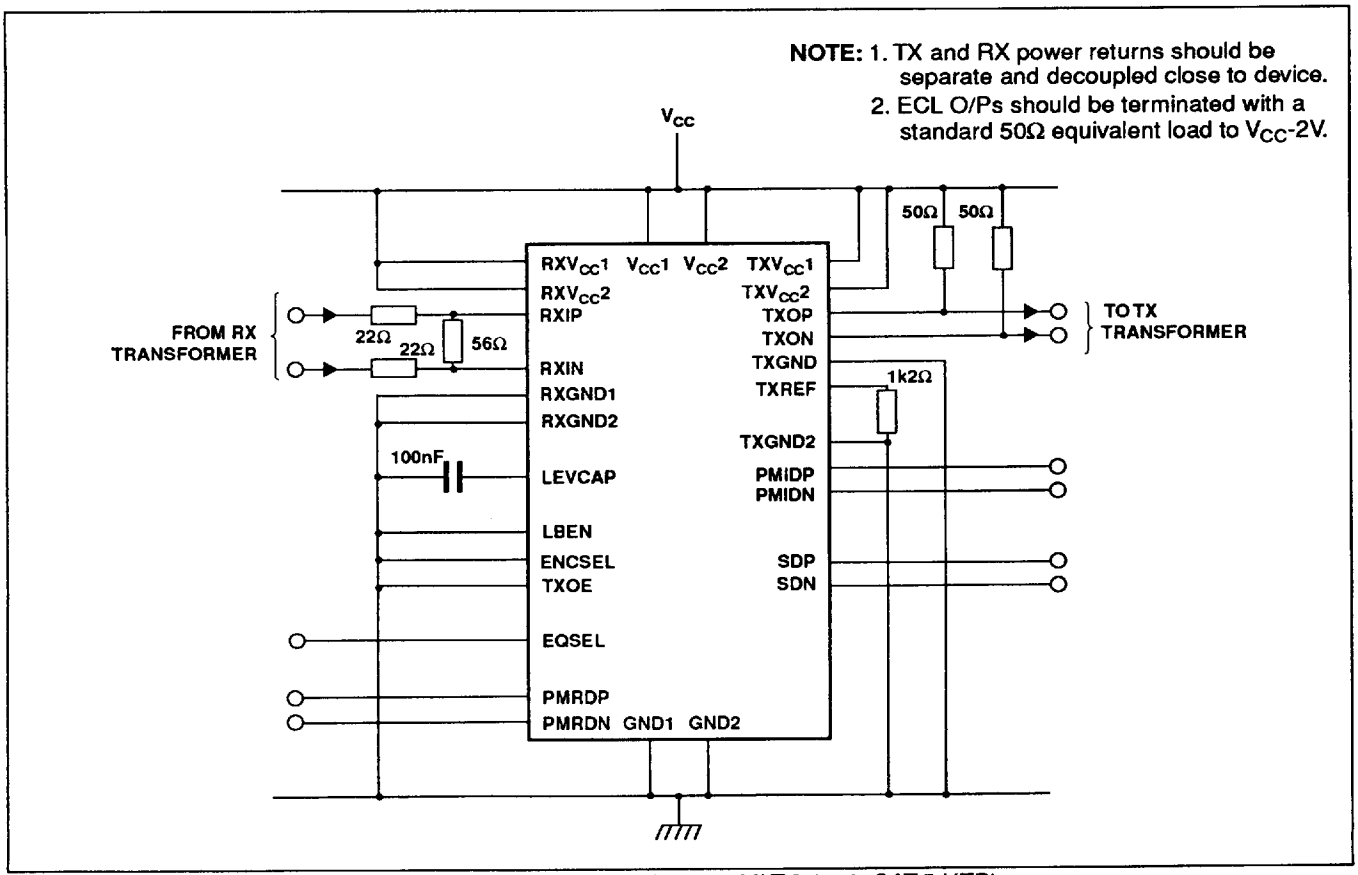


Fig.4 Typical application diagram (MLT-3 100Ω CAT-5 UTP)

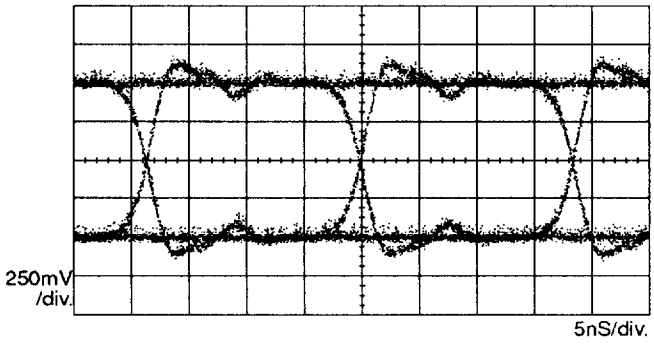


Fig.5 Transmit output NRZI data

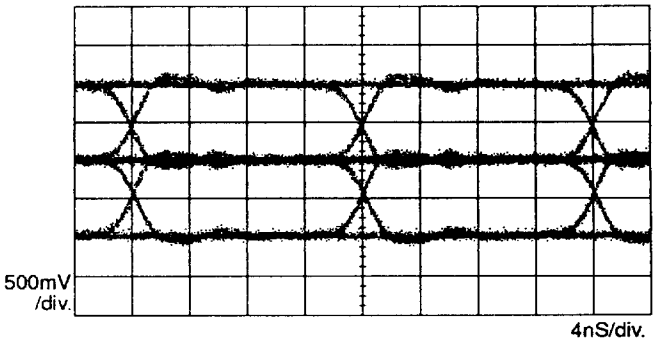


Fig.6 Transmit output MLT-3 data

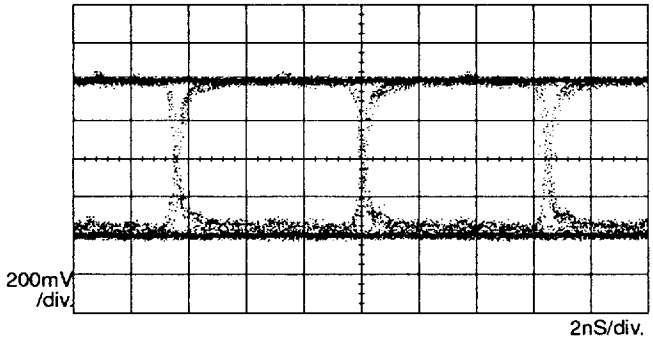


Fig.7 PECL RX data output NRZI mode

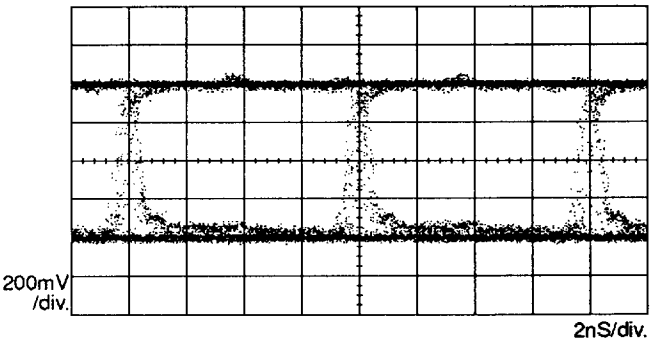


Fig.8 PECL RX data output MLT-3 mode

PIN DESCRIPTIONS

Pin	Name	Type	Description
1	RXIN	input	Differential line receiver inputs
2	RXIP	input	
3	RXGND1	power	Ground to receiver circuits
4	LEVCAP	analog	Level capacitor. This stores the control voltage generated by the quantized feedback circuits
5	$TXV_{CC}1$	power	+5V supply to transmit current reference circuit
6	TXREF	analog	Reference current setting pin for transmit outputs TXOP, TXON
7	TXGND2	power	Ground to current reference circuit
8	TXON	output	Differential current driver outputs (MLT-3 or NRZ) from transmit encoder
9	TXOP	output	
10	TXGND	power	Ground to transmit output driver
11	$TXV_{CC}2$	power	+5V supply to transmit output driver
12	ENCSEL	input	TTL logic input to select encoded state of TXO outputs and RXI inputs (0 = MLT-3, 1 = NRZ)
13	$V_{CC}1$	power	+5V supply to TTL logic inputs
14	GND1	power	Ground to TTL logic inputs
15	PMRDP	input	Differential PECL logic inputs to transmit encoder
16	PMRDN	input	
17	EQSEL	input	3 level input to select receiver equalization mode: 0 = full equalization, 1 = no equalization, float = adaptive equalization
18	TXOE	input	Schmitt input: 0 = normal operation, 1 = inhibit TX outputs
19	LBEN	input	TTL logic input to select loopback mode. LBEN = 1 routes the PMRD inputs to the PMID outputs and forces the TXOP outputs to a static state
20	SDP	output	Differential PECL logic outputs indicating 'signal detect' and loopback mode status
21	SDN	output	
22	GND2	power	Ground to PECL outputs
23	$V_{CC}2$	power	+5V supply to PECL outputs
24	PMIDN	output	Differential PECL compatible logic outputs from receiver circuit
25	PMIDP	output	
26	$RXV_{CC}2$	power	+5V
27	$RXV_{CC}1$	power	+5V supply to receiver circuits
28	RXGND2	power	Ground to receiver circuits

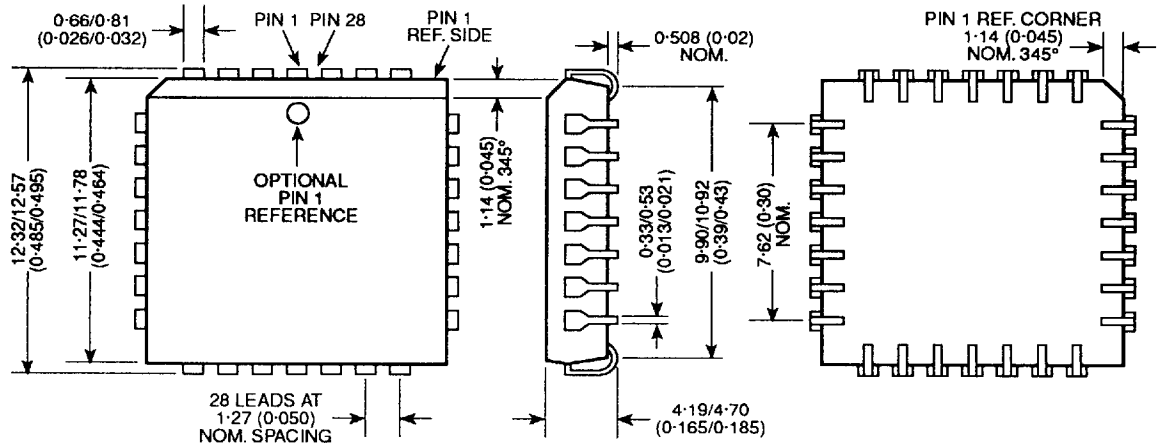
Table.1 Pin descriptions

GLOSSARY OF TERMS AND ABREVIATIONS

UTP	Unshielded Twisted Pair
STP	Shielded Twisted Pair
NRZ	Non Return To Zero
NRZI	Non Return To Zero Inverted on 1s
MLT-3	Multi Level Transmit -3 levels
FDDI	Fiber Distributed Data Interface
PHY	PHYsical Layer
ATM	Asynchronous Transfer Mode
PECL	Pseudo ECL

PACKAGE DETAILS

Dimensions are shown thus: mm (in). For further package information, please contact your local Customer Service Centre.



NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

28-LEAD QUAD PLASTIC J-LEAD – HP28

GEC PLESSEY
SEMICONDUCTORS

HEADQUARTERS OPERATIONS
GEC PLESSEY SEMICONDUCTORS
Cheney Manor, Swindon,
Wiltshire, United Kingdom. SN2 2QW
Tel: (01793) 518000
Fax: (01793) 518411

GEC PLESSEY SEMICONDUCTORS
P.O. Box 660017,
1500 Green Hills Road,
Scotts Valley, California 95067-0017,
United States of America.
Tel (408) 438 2900
Fax: (408) 438 5576

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