Ordering number:ENN*2928A

CMOS IC

# LC66E516

## 4-bit Single Chip Microcontroller with EPROM

**Preliminary**

## Overview

The LC66E516 is a 4-bit single-chip microcontroller with an EPROM on-chip, and can be used for developing and evaluating application programs for the LC665XX series 4-bit single-chip microcontrollers.

The LC66E516 microcontroller is a 4-bit single-chip IC with an EPROM on-chip and brought to you in ceramic DIC64S package with a window and ceramic QFC64 package with a window. This window permits the user to erase EPROM program data as many times as he or she wants. Then, it could be said that this single-chip IC is best suited for developing application programs.

The LC66E516 microcontroller has the same function and the pin assignment as those of the 4-bit single-chip mask programmed ROM-version LC66E516 microcontroller. The on-chip EPROM is 16k bytes in size.

## Features

- Optional functions user-selectable by speciflying EPROM option data.
  The 56 optional functions on the LC665XX series single-chip microcontrollers can be selected by writing appropriate data to the on-chip EPROM. This function specification by the user allows application system to be developed and tested under the same working environment as that of production chip. In other words, the same interface circuit functions as those of production chips can be built up by the user.
  Please note that the above-mentioned optional functions include port output type(open-drain or pull-up), output pin logic level at reset, watchdog timer selection and the like.
- On-chip 16KB EPROM
  The on-chip EPROM enable the user to develop and evaluate application programs which can be run on every LC665XX series microcontroller. Please note that the LC665XX series microcontrollers are LC66506B, LC66508B, LC66512B, LC66516B, LC66556A, LC66558A, LC66562A, LC66566A, LC66556B, LC66558B, LC66562B, LC66566B and that they are listed in the table on page 18 with a few pieces of information.
- Write/Read operation with an EPROM writer
  Used with the dedicated writer board (W66E516DH for DIC, W66E516QH for QFC), an EPROM writer available on your local market permits the user to write or read data to or form the 16KB on-chip EPROM. Please note that the EPROM writer should be an ADVANTEST product or the EVA800/850 accessory writer used for the 27128 type EPROM.
- Pin-compatible with a mask programmed ROM-version single-chip microcontroller (LC66516B, for example)
- Instruction cycle time:0.92μs to 10μs
- Single +5V power supply (Ta=10°C to 40°C)



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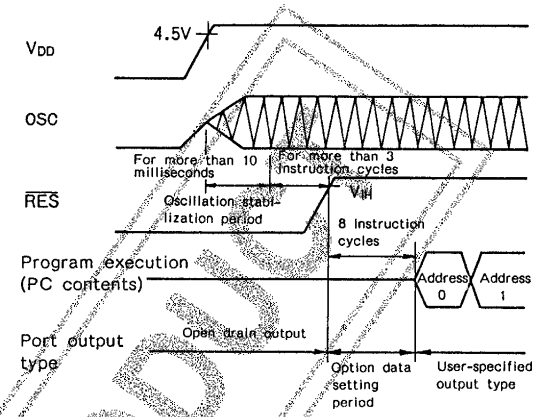
## Usage notes

The LC66E516 single-chip IC is intended for use by those who are in charge of the development and evaluation of application programs for the LC665XX series 4-bit single-chip microcontrollers. please keep in mind the following when the user application developers are to work with this single-chip microcontroller.

- Notes on LC66E516 internal operations after reset

  As the figure shows, the LC66E516 microcontroller starts normal program execution at least 3 instruction cycles later after the oscillation by the OSC function block becomes stable. In other words, the $\overline{RES}$ pin level (active low) must be active for at least 3 instruction cycles after the oscillation becomes stabilized. As the figure also shows, the oscillation stabilization requires more than 10 milliseconds. It is also shown that option data setting requires 8 instruction cycles after the $\overline{RES}$ pin level changes to the inactive level (or to $V_{IH}$ voltage level). After all those operations are carried out, the LC66E516 microcontroller starts program execution normally from address 0 in the EPROM (that is, the content at address 0 is automatically set in the program counter (PC)). At this point, Please note that port output type will be open-drain, not pull-up output type, as long as the $\overline{RES}$ pin stays active.




- Notes on evaluation of user application programs for the LC66506, LC66508, LC66512, LC66556, LC66558, LC66562, microcontrollers

  The above six mask programmed ROM-version microcontrollers are equipped with different ROMs in size from that of the LC66E516 microcontroller. Therefore, the following things should be taken into consideration when you are to make an access to the ROM on the LC66E516 microcontroller.

  First, it should be kept in mind that the last 8 addresses between 3FF8 and 3FFF are used by the user in order to specify functional option data. This 8-byte area is called option specification area. This option specification area must be exclusively used for storing function option data. The option specification will be discussed in detail later in this catalog.

  As far as the cross assembler to be employed is concerned, the user should use the one for the LC66516 microcontroller. In addition, when you write your user application program, you cannot make any access to addresses beyond the area of a mask programmed ROM. Such addresses cannot exist anywhere on mask programmed ROM-version microcontrollers. To avoid such an illegal access to those nonexistent area, it is recommended that jump (or branch) operations with a JMP instruction and so on be used in your user application program. Furthermore, please write "0" to the area beyond that of a mask programmed ROM. In this case, needless to say, the last 8 addresses of the EPROM should be excluded from the "0" padding.

  When evaluating the LC66506, LC66508, LC66556, LC66558, do not use the SB instruction.

- Program protection from exposure to light

  Exposure to light will destroy the precious EPROM data that you have entered with much labor. In order to protect them, it should be strongly recommended that the EPROM window should be covered with an opaque label while you are at work with the EPROM.

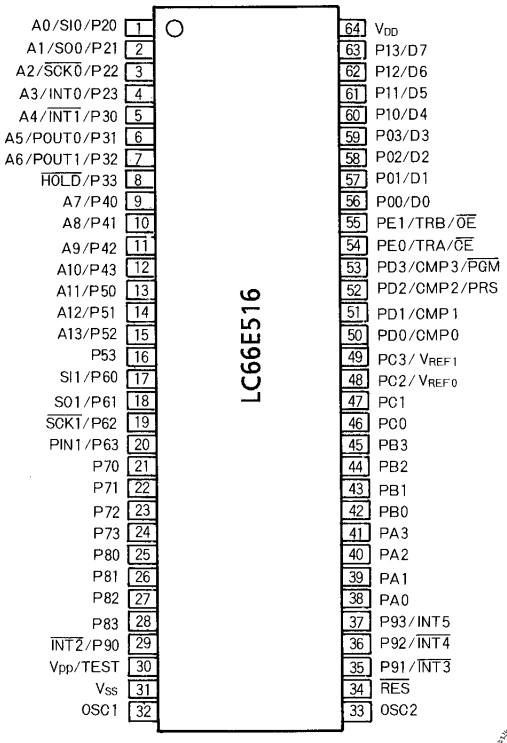
- For the LC66E516/P516, if the $\overline{RES}$ is set to "L" level during the HOLD mode ($\overline{HOLD}$=L), be sure to change the $\overline{HOLD}$ level from "L" to "H" and then change the $\overline{RES}$ level from "L" to "H" when releasing the HOLD mode.

## Comparison of LC66E516 and the masked ROM version(LC665XX)

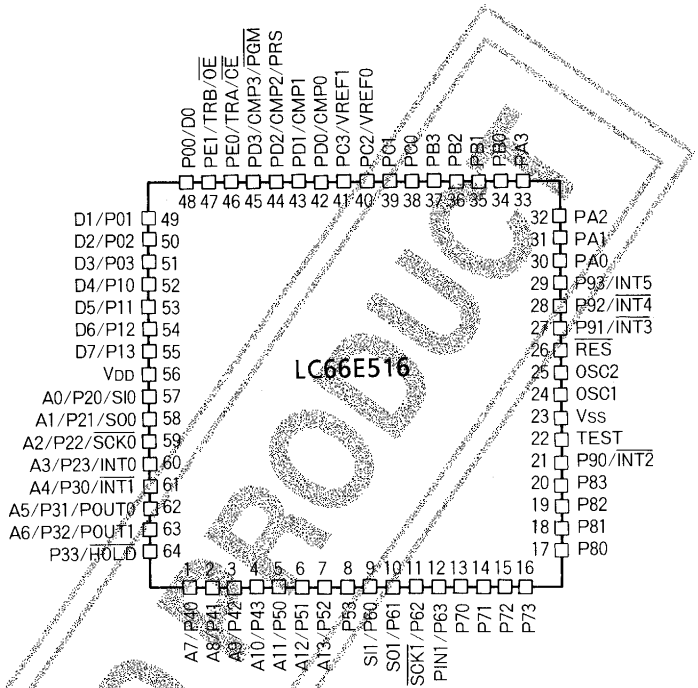
| Item | LC66E516 | LC665XX series(masked ROM version) | |
|---|---|---|---|
| | | LC6650X series(including tool) | LC6655X series |
| Differences in system<br>• Hardware wait time (number of cycles/at HOLD mode released state | 65536 cycles<br>Approx. 64ms at 4MHz (Tcyc=1µs) | 65536 cycles<br>Approx. 64ms at 4MHz (Tcyc=1µs) | 16384 cycles<br>Approx. 32ms at 2MHz (Tcyc=2µs)<br>Approx. 64ms at 1MHz (Tcyc=4µs) |
| • Value(including the value after HOLD mode release)of timer 0 during reset | "$FFO_H$" is set. | "$FFO_H$" is set. | "$FFC_H$" is set. |
| • Port output type during reset | Open-drain output (other than P0, P1) (floating)<br>H/L output (P0, P1)with pull-up | Option-specified output type | Option-specified output type |
| Differences in main characteristics<br>• Operating supply voltage/operating speed | 4.5V to 5.5V/0.92 to 10µs | 4.0V to 6.0V/0.92 to 10µs (tool:5V ±5%) | 2.2V to 5.5V/3.92 to 10µs<br>3.0V to 5.5V/1.96 to 10µs |
| • Operating free-air temperature (Topr) | 10 to 40°C | –30 to +70°C | |
| • Current drain during HALT mode ON ($I_{DD}$ HALT) | 5.0mA max. (4MHz ceramic resonator oscillation)<br>6.0mA max. (4MHz external clock source)<br>5.0mA max. (3MHz typ. RC oscillation) | 2.5mA max.(4MHz ceramic resonator oscillation)<br>3.5mA max.(4MHz external clock source)<br>2.5mA max.(3MHz typ.RC oscillation)<br>(tool:evaluation impossible) | 2.5mA max.(4MHz ceramic resonator oscillation)<br>3.5mA max.(4MHz external clock source) |
| • External constants for RC oscillation | C=100pF<br>R=2.2kΩ | C=100pF<br>R=2.7kΩ(tool:R=2.2kΩ) | Not applicable |
| Case outline (package) | DIC64S with window<br>QFC64 with window | DIP64S<br>QFP64A | DIP64S<br>QFP64E |

## Pin Assignments

DIC64S with window



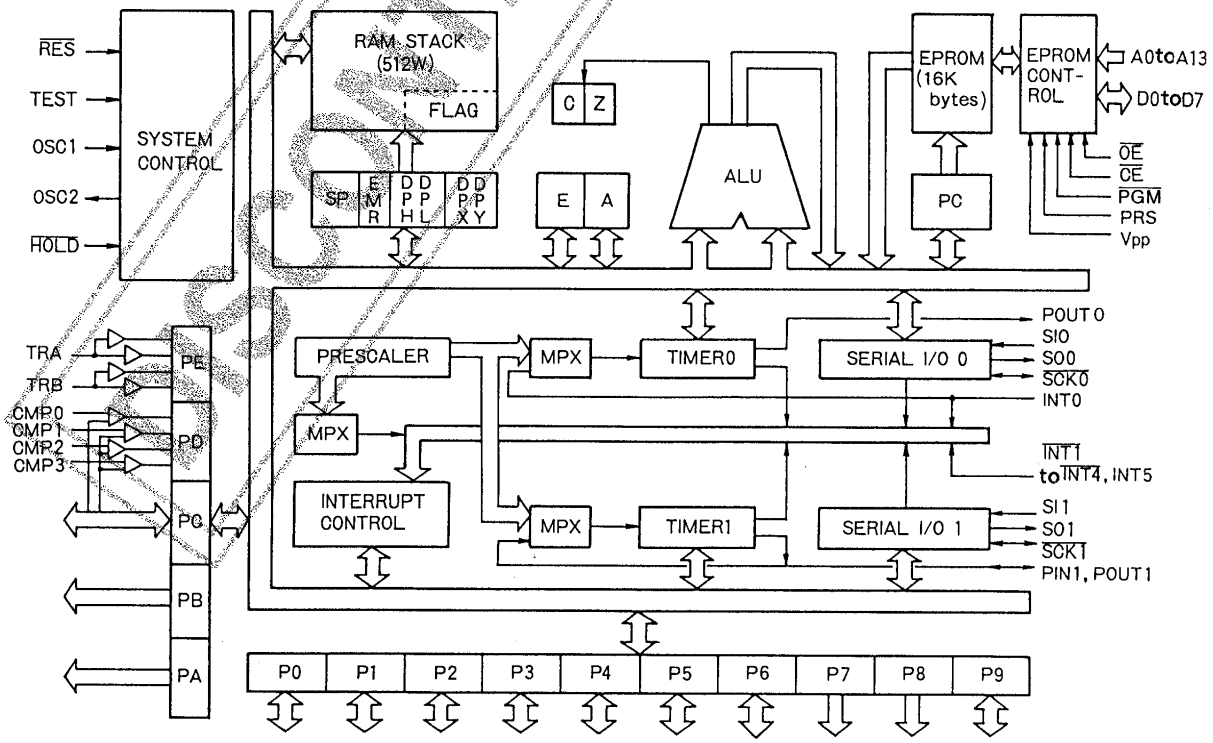

QFC64 with window




Top view



## Block Diagram



## Pin Function

| Pin name | Input/ output | Functional description | Output driver circuit output type | Option | During EPROM mode operation |
|---|---|---|---|---|---|
| P00/D0<br>P01/D1<br>P02/D2<br>P03/D3 | I/O | Input/output port pins P00 to P03<br>· Used for input/output operation in 4-bit units or bit units.<br>· Used for controlling HALT mode operation. | · Pch: Pull-up (Pu) MOS type<br>· Nch: Small sink current output type | · Pull-up (Pu) MOS output type or Nch open-drain (OD) output type<br>· Output pin level at reset | Data input/output pins (D0 to D3) |
| P10/D4<br>P11/D5<br>P12/D6<br>P13/D7 | I/O | Input/output port pins P10 to P13<br>· Used for input/output operation in 4-bit units or bit units. | · Pch: Pull-up (Pu) MOS type<br>· Nch: Small sink current output type | · Pu MOS output type or Nch OD output type<br>· Output pin level at reset | Data input/output pins (D4 to D7) |
| P20/SI0/A0<br>P21/SO0/A1<br>P22/$\overline{SCK0}$/A2<br>P23/INT0/A3 | I/O | Input/output port pins P20 to P23<br>· Used for input/output operation in 4-bit units or bit units.<br>· P20: Common with serial input SI0<br>P21: Common with serial output SO0<br>P22: Common with serial clock $\overline{SCK0}$<br>· P23: Common with INT0 interrupt request input, timer 0-used event count input, pulse width measurement input | · Pch: CMOS type<br>· Nch: Small sink current output type<br>· +15V withstand voltage at Nch open drain (OD) output | · CMOS output type or Nch OD output type | Address input (A0 to A3) |
| P30/$\overline{INT1}$/A4<br>P31/POUT0/A5<br>P32/POUT1/A6 | I/O | Input/output port pins P30 to P32<br>· Used for input/output operation in 3-bit units or bit units and for input operation in 4-bit units (together with the P33 pin) or bit units.<br>· P30 : Common with $\overline{INT1}$ interrupt request input<br>· P31 : Common with burst pulse output from timer 0<br>· P32 : Common with burst pulse output from timer 1 and PWM output | · Pch: CMOS type<br>· Nch: Small sink current output type<br>· +15V withstand voltage for Nch OD output | · CMOS output type or Nch OD output type | Address input (A4 to A6) |
| P33/$\overline{HOLD}$ | I | HOLD mode control signal input<br>· Used for activating HOLD operation mode with $\overline{HOLD}$ = L (active low) by using a HOLD instruction.<br>· Used for restarting the CPU operation from the HOLD mode operation by changing the $\overline{HOLD}$ pin level from L to H.<br>· Used as input port pin P33 to form a 4-bit input port with P30 to P32.<br>· The CPU blocks cannot be reset even if the $\overline{RES}$ (active low) pin level changes from H to L with the $\overline{HOLD}$ pin level = L. This means that you cannot write a user application program requiring the P33/$\overline{HOLD}$ pin to enter the L level state at the moment the system is powered on. | | | |
| P40/A7<br>P41/A8<br>P42/A9<br>P43/A10 | I/O | Input/output port pins P40 to P43<br>· Used for input/output operation in 4-bit units or bit units.<br>· These four pins, combined with port pins P50 to P53, can be used for input/output operation in 8-bit units.<br>· These four pins, together with port pins P50 to P53, can be used for 8-bit ROM data output. | · Pch: Pull-up (Pu) MOS type<br>· Nch: Small sink current output type | · Pu MOS output type or Nch OD output type | Address input (A7 to A10) |
| P50/A11<br>P51/A12<br>P52/A13<br>P53 | I/O | Input/output port pins P50 to P53<br>· Used for input/output operation in 4-bit units or bit units.<br>· These four pins, combined with port pins P40 to P43, can be used for input/output operation in 8-bit units.<br>· These four pins, together with port pins P40 to P43, can be used for 8-bits ROM data output. | · Pch: Pull-up (Pu) MOS type<br>· Nch: Small sink current output type | · Pu MOS output type or Nch OD output type | Address input (A11 to A13) |

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| Pin name | Input/ output | Functional description | Output driver circuit output type | Option | During EPROM mode operation |
|---|---|---|---|---|---|
| P60/SI1<br>P61/SO1<br>P62/$\overline{SCK1}$<br>P63/PIN1 | I/O | Input/output port pins P60 to P63<br>· Used for input/output operation in 4-bit units or bit units.<br>· P60: Common with serial input SI1<br>· P61: Common with serial output $\overline{SO1}$<br>· P62: Common with serial clock $\overline{SCK1}$<br>· P63: Common with timer 1-used event count input | · Pch: CMOS type<br>· Nch: Small sink current output type<br>· +15V withstand voltage for Nch OD output | · CMOS output type or Nch OD output type | |
| P70<br>P71<br>P72<br>P73 | O | Output port pins P70 to P73<br>· Used for output operation in 4-bit units or in bit units.<br>· If you use an input-related instruction in your application program, the content of the output latch will be input. | · Pch: Pull-up (Pu) MOS type<br>· Nch: Medium sink current output type<br>· +15V withstand voltage for Nch OD output type | · Pu MOS output type or Nch output type | |
| P80<br>P81<br>P82<br>P83 | O | Output port pins P80 to P83<br>· Used for output operation in 4-bit units or bit units.<br>· If you use an input-related instruction in your application program,the content of the output latch will be read in.<br>· Pch OD output type optionally available. More about this later. | · Pch: CMOS type<br>· Nch: Small sink current type | · CMOS output type or Pch OD output type<br>· Output pin level at reset | |
| P90/$\overline{INT2}$<br>P91/$\overline{INT3}$<br>P92/$\overline{INT4}$<br>P93/INT5 | I/O | Input/output port pins P90 to P93<br>· Used for input/output operation in 4-bit units or bit units.<br>· P90: Common with $\overline{INT2}$ interrupt request input<br>· P91: Common with $\overline{INT3}$ interrupt request input<br>· P92: Common with $\overline{INT4}$ interrupt request input<br>· P93: Common with INT5 interrupt request input | · Pch: CMOS type<br>· Nch: Small sink current type | · CMOS output type or Nch OD output type | |
| PA0<br>PA1<br>PA2<br>PA3 | O | Output port pins PA0 to PA3<br>· Used for input operation in 4-bit units or bit units.<br>· If you use an input-related instruction in your application program, the content of the output latch will be read in. | · Pch: Pull-up (Pu) MOS type<br>· Nch: Medium sink current type<br>· +15V withstand voltage for Nch OD output type | · Pu MOS output type or Nch OD output type | |
| PB0<br>PB1<br>PB2<br>PB3 | O | Output port pins PB0 to PB3<br>· Used for output operation in 4-bit units or bit units.<br>· If you use an input-related instruction in your application program, the content of the output latch will be read in. | · Pch: Pull-up (Pu) MOS type<br>· Nch: Medium sink current type | · Pu MOS output type or Nch OD output type | |
| PC0<br>PC1<br>PC2/VREF0<br>PC3/VERF1 | I/O | Input/output port pins PC0 to PC3<br>· Used for input/output operation in 4-bit units or bit units.<br>· PC2: Common with VREF0 comparator comparison voltage terminal<br>· PC3: Common with VREF1 comparator comparison voltage terminal | · Pch: CMOS type<br>· Nch: Small sink current type | · CMOS output type or Nch OD output type | |
| PD0/CMP0<br>PD1/CMP1<br>PD2/CMP2/$\overline{PRS}$<br>PD3/CMP3/$\overline{PGM}$ | I | Input port pins PD0 to PD3<br>· These four pins can be programmed for comparator inputs in user application programs. PD0 input will be compared with VREF0. Other inputs will be compared with VREF1. Please note that there are four comparators available in this system and these four comparators are grouped into two (one group: CMP0 and CMP1. the other group: CMP2 and CMP3), and that the comparators must be selected in group units. | | | EPROM control signal inputs ($\overline{PRS}$ and $\overline{PGM}$) |
| PE0/TRA/$\overline{CE}$<br>PE1/TRB/$\overline{OE}$ | I | Input port pins PE0 to PE1<br>· These two tristate input port pins can be controlled in your application programs. | | | EPROM controi signal inputs ($\overline{OE}$ and $\overline{CE}$) |

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| pin name | Input/ output | Functional description | Output driver circuit output type | Option | During EPROM mode operation |
|---|---|---|---|---|---|
| OSC1<br>OSC2 | I<br>O | Pins for connecting system clock oscillator externally. If external clock source mode is to be employed, use the OSC1 pin only for clock input. Leave the other pin open. | | · Ceramic resonator oscillation. RC oscillation or external clock source | |
| $\overline{RES}$ | I | Input port pin for system reset request signal<br>· To initialize the CPU, the $\overline{RES}$ (active low) pin level must be L with the P33/ $\overline{HOLD}$ pin level = H. | | | |
| TEST/$V_{pp}$ | I | Input port pin for CPU test signal<br>This pin should be connected with the VSS pin when this device is in operation. | | | |
| $V_{DD}$<br>Vss | | Power supply pin | | | |

**Remarks:**

Pu MOS type output --- Pch MOS type transistor acts as a pull-up resistor when data is output.
CMOS type output --- Pch MOS type transistor does not act as a pull-up resistor when data is output. Instead, it forms a complementary-symmetry MOS output circuit with an Nch MOS type transistor.
OD output --- Open drain output type

Note:

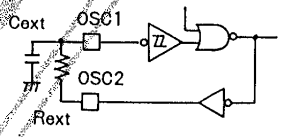
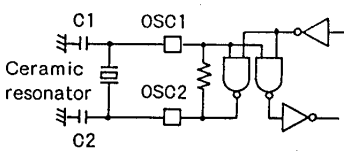
At the system reset, the pin output level of each of input/output and output port pins will be "H" except for such pins as ports 0, 1 and 8. The output level of these exceptions can be specified by the user options. In addition to this system reset operation, the port output type will be set to open drain at the system reset, which is irrespective of user option specification. In this case, there is no exception.

**User options**

1. Option for specifying the output level of ports 0, 1 and 8 at the system reset
   The output level of ports 0, 1 and 8 at the system reset can be selected from the following two optional levels by the user option. In this case, it should be kept in mind that the output levels of all the four bits of each input/output port are specified at the same time.

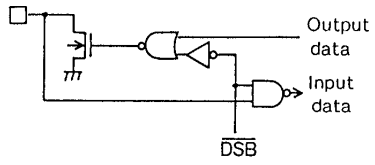
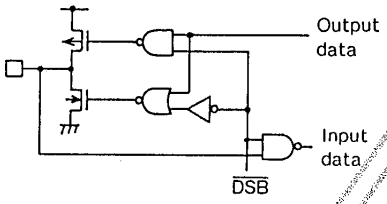
| Option name | Condition |
|---|---|
| 1. "H" output level | In 4-bit units |
| 2. "L" output level | In 4-bit units |

2. Option for selecting oscillation circuit

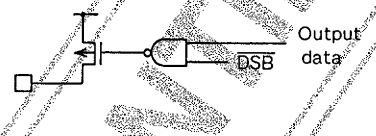
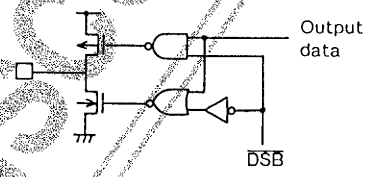
| Option name | Selectable oscillation circuit | Condition |
|---|---|---|
| 1. External clock source |  | · Schmitt trigger input |
| 2. 2-pin (OSC1 and OSC2) RC oscillation circuit |  | · Schmitt trigger input |
| 3. Ceramic resonator oscillation circuit |  | |

3. Option for selecting watchdog timer function
   This option permits the user to select the watchdog timer function. This function could be helpful in detecting a timeout error from your user application program.
4. Option for specifying port output type

i) This option permits the user to select a desired port output type of the following ports from the two output types listed in the table below. Please note that port output types can be specified in bit units.
   Ports: P0, P1, P2, P3 (P33/$\overline{\text{HOLD}}$ not included), P4, P5, P6, P7, P9, PA, PB, and PC

| Option name | Selected output circuit type | Condition |
|---|---|---|
| 1. Open drain output type |  | Ports P7, PA and PB are provided exclusively for output operation.<br>Ports P2, P3, P6 and P9 employ Schmitt trigger input. |
| 2. Pull-up transistor output type |  | Ports P7, PA and PB are provided exclusively for output operation.<br>Ports P2, P3, P6 and P9 employ Schmitt trigger input.<br>The Pch type MOS transistor can act as either a pull-up resistor (for Pu MOS output circuit) or an output transistor (CMOS output circuit), which depends on its driving capability.<br>CMOS output type: P2, P3, P6, P9 and PC.<br>Pu MOS output: P0, P1, P4, P5, P7, PA and PB. |

ii) The output type of P8 can be selected from the following two options. Please note that the output types for the port pins can be specified in bit units.

| Option name | Selected output circuit type | Condition |
|---|---|---|
| 1. Option drain output type (Pch OD) |  | |
| 2. Pull-down resistor output type |  | |

iii) Comparator input of the PD and tristate input of the PE can be specified in your user application program.
   User option specification
   To select desired user options, you must write appropriate data into the user option specification area in the on-chip EPROM. The user option specification will be discussed in detail on the following pages.

How to write data in the user option specification area and the program area in the on-chip EPROM

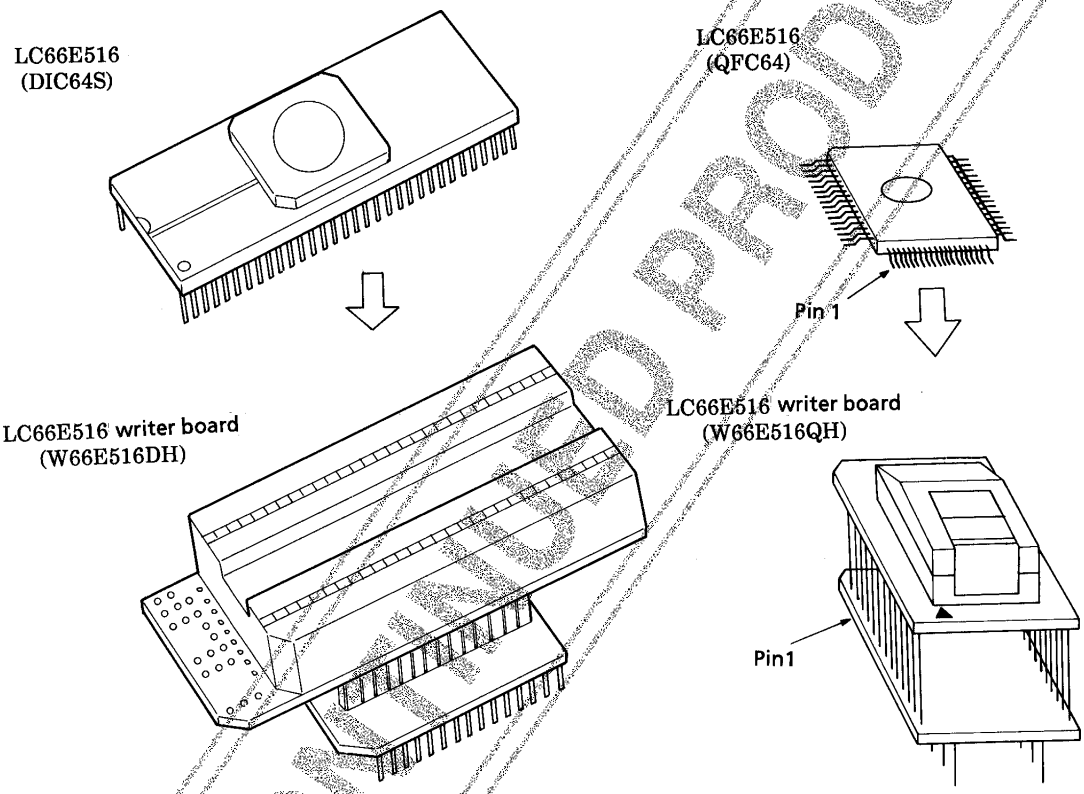
(1) Writing option codes to the user option specification area

Use the cross assembler for the LC66516 mask programmed ROM-version microcontroller when you write option codes in the user specification area. When your source application program is assembled, the option data will be stored in the user option specification area (3FF8 through 3FFF). In addition to the above writing, you are allowed to write option data directly into the user option specification area in the on-chip EPROM. In this case, making references to the option code specification list on the next page will be a "must".

(2) Writing program into the on-chip EPROM program area

An EPROM writer available on your local market can be used to write program into the on-chip EPROM program area. In this case, the EPROM writer (27128 EPROM writer) must be used together with the dedicated writer board because the pin conversion (64 into 28) is required. The dedicated writer board is shown below.

Please note that the EPROM writer must be either an ADVANTEST product or the EVA800/850 accessory writer. Such an EPROM writer enables you to write your application program into the EPROM in Intel high-speed writing method.




This dedicated writer board is inserted into the EPROM writer available on your local market. (Select either an ADVANTEST writer product or the EVA800/850 accessory EPROM writer).

| Manufacturer | Model |
|---|---|
| ADVANTEST | TR4943, R4944A, R4945 or equivalent |
| SANYO | EVA850 or EVA800 accessory EPROM writer |

Notes

1. Intel is a registered trademark of Intel Corporation.
2. ADVANTEST is a registered trademark of ADVANTEST Corporation.

(3) How to erase the contents of the on-chip EPROM

To erase the contents of the on-chip EPROM, you can use an EPROM eraser available on your local market.

## Option code specification list

| ROM address | Bit | Optional item | | Option data and selections |
|---|---|---|---|---|
| 3FF8H | 7 | Unused | | Always set to "0". |
| | 6 | | | |
| | 5 | | | |
| | 4 | Oscillation circuit type | | 1: Ceramic resonator oscillation. 0: RC oscillation or external clock source |
| | 3 | P8 | Output level at the system reset | 1="H"–level, 0="L"–level |
| | 2 | P1 | | |
| | 1 | P0 | | |
| | 0 | Watchdog timer function option | | 1: Selected. 0: Not selected. |
| 3FF9H | 7 | P13 | Output circuit type | 1=PU, 0=OD |
| | 6 | P12 | | |
| | 5 | P11 | | |
| | 4 | P10 | | |
| | 3 | P03 | Output circuit type | 1=PU, 0=OD |
| | 2 | P02 | | |
| | 1 | P01 | | |
| | 0 | P00 | | |
| 3FFAH | 7 | P33 | Unused | Always set to "0". |
| | 6 | P32 | Output circuit type | 1=PU, 0=OD |
| | 5 | P31 | | |
| | 4 | P30 | | |
| | 3 | P23 | Output circuit type | 1=PU, 0=OD |
| | 2 | P22 | | |
| | 1 | P21 | | |
| | 0 | P20 | | |
| 3FFBH | 7 | P53 | Output circuit type | 1=PU, 0=OD |
| | 6 | P52 | | |
| | 5 | P51 | | |
| | 4 | P50 | | |
| | 3 | P43 | Output circuit type | 1=PU, 0=OD |
| | 2 | P42 | | |
| | 1 | P41 | | |
| | 0 | P40 | | |
| 3FFCH | 7 | P73 | Output circuit type | 1=PU, 0=OD |
| | 6 | P72 | | |
| | 5 | P71 | | |
| | 4 | P70 | | |
| | 3 | P63 | Output circuit type | 1=PU, 0=OD |
| | 2 | P62 | | |
| | 1 | P61 | | |
| | 0 | P60 | | |
| 3FFDH | 7 | P93 | Output circuit type | 1=PU, 0=OD |
| | 6 | P92 | | |
| | 5 | P91 | | |
| | 4 | P90 | | |
| | 3 | P83 | Output circuit type | 1=PD, 0=OD |
| | 2 | P82 | | |
| | 1 | P81 | | |
| | 0 | P80 | | |
| 3FFEH | 7 | PB3 | Output circuit type | 1=PU, 0=OD |
| | 6 | PB2 | | |
| | 5 | PB1 | | |
| | 4 | PB0 | | |
| | 3 | PA3 | Output circuit type | 1=PU, 0=OD |
| | 2 | PA2 | | |
| | 1 | PA1 | | |
| | 0 | PA0 | | |
| 3FFFH | 7 | Unused | | Always set to "0". |
| | 6 | | | |
| | 5 | | | |
| | 4 | | | |
| | 3 | PC3 | Output circuit type | 1=PU, 0=OD |
| | 2 | PC2 | | |
| | 1 | PC1 | | |
| | 0 | PC0 | | |



Remarks:

PU --- Pull-up MOS type resistance output

PD --- Pull-down MOS type resistance output

OD --- Open-drain output

Note: The pull-up MOS type resistance output represents the pull-up MOS (Pu MOS) type resistor output circuit and the complementary MOS (CMOS) type output circuit.

# Specifications

## Absolute Maximum Ratings at Ta = 25˚C, $V_{SS}$=0V

| Parameter | Symbol | Pins applicable and related information | Conditions | Ratings | Unit | Note |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | $V_{DD}$ | | –0.3 to +7.0 | V | |
| Input voltage | $V_{IN}$(1) | P2, P3 (except P33/$\overline{HOLD}$) and P6. | | –0.3 to +15.0 | V | 1 |
| | $V_{IN}$(2) | All the pins other than the above | | –0.2 to $V_{DD}$+0.3 | V | 2 |
| Output voltage | $V_{OUT}$(1) | P2,P 3 (except P33/$\overline{HOLD}$), P6, P7 and PA. | | –0.3 to +15.0 | V | 1 |
| | $V_{OUT}$(2) | All the pins other than the above. | | –0.3 to $V_{DD}$+0.3 | V | 2 |
| Output current per pin | $I_{ON}$(1) | P0, P1, P2, P3 ( except P33/$\overline{HOLD}$), P4, P5, P6,P8,P9 and PC. | | 4 | mA | 3 |
| | $I_{ON}$(2) | P7, PA, PB | | 20 | mA | 3 |
| | $-I_{OP}$(1) | P0, P1, P4, P5, P7, PA, PB | | 2 | mA | 4 |
| | $-I_{OP}$(2) | P2, P3 (except P33/$\overline{HOLD}$), P6, P8, P9 and PC. | | 4 | mA | 4 |
| Pin total current | $\Sigma I_{ON}$(1) | P2, P3 (except P33/$\overline{HOLD}$), P4, P5, P6, P7 and P8. | | 75 | mA | 3 |
| | $\Sigma I_{ON}$(2) | P0, P1, P9, PA, PB, PC | | 75 | mA | 3 |
| | $-\Sigma I_{OP}$(1) | P2, P3 (except P33/$\overline{HOLD}$), P4, P5, P6, P7 and P8. | | 25 | mA | 4 |
| | $-\Sigma I_{OP}$(2) | P0, P1, P9, PA, PB, PC | | 25 | mA | 4 |
| Allowable power dissipation | Pd max | Ta=10 to 40°C | DIC-64S | 600 | mW | |
| Operating temperature | Topr | | | 10 to 40 | °C | |
| Storage temperature | Tstg | | | –55 to +125 | °C | |

Note 1: Applicable only to the pins with open drain output circuit. Otherwise, refer to the values listed in the "all the pins other than the above" column.
Note 2: As far as oscillation input and output are concerned, the voltage range can cover the self-oscillating level.
Note 3: Sink current. As far as the P8 is concerned, these parameters can apply only to the CMOS output circuit.
Note 4: Source current. Apply to the both of the pull-up output circuit and the CMOS output circuit except for P8.

## Allowable operating conditions at Ta = –10˚C to 40°C, $V_{SS}$=0V, unless otherwise noted

| Parameter | symbol | Pins applicable | Conditions | | Ratings | | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$(V) | min | typ | max | | |
| Operating supply voltage | $V_{DD}$ | $V_{DD}$ | | | 4.5 | 5.0 | 5.5 | V | |
| Memory backup voltage | $V_{DD}$(H) | $V_{DD}$ | With HOLD mode "ON" | | 1.8 | | 5.5 | V | |
| Input high-level voltage | $V_{IH}$(1) | P2, P3(except P33/$\overline{HOLD}$) and P6. | With output Nch transistor "OFF" | 4.5 to 5.5 | 0.75$V_{DD}$ | | +13.5 | V | 1 |
| | $V_{IH}$(2) | P33/$\overline{HOLD}$, P9 $\overline{RES}$ OSC1 | With output Nch transistor "OFF" | 4.5 to 5.5 | 0.75$V_{DD}$ | | $V_{DD}$ | V | 2 |
| | $V_{IH}$(3) | PO, P1, P4, P5, PC, PD, PE | With output Nch transistor "OFF" | 4.5 to 5.5 | 0.7$V_{DD}$ | | $V_{DD}$ | V | 3 |
| | $V_{IH}$(4) | PE | With tristate input mode selected | 4.5 to 5.5 | 0.8$V_{DD}$ | | $V_{DD}$ | V | |

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| Parameter | | | Symbol | Pins applicable | Conditions | | $V_{DD}$(V) | Ratings min | Ratings typ | Ratings max | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Intermediate level input voltage | | | $V_{IM}$ | PE | With tristate input mode selected. | | 4.5 to 5.5 | $0.4V_{DD}$ | | $0.6V_{DD}$ | V | |
| In-phase input voltage | | | $V_{CMM}$ | PD, PC2, PC3 | With comparator input mode selected | | 4.5 to 5.5 | 1.0 | | $V_{DD}-1.5$ | V | |
| Input low-level voltage | | | $V_{IL}$(1) | P2, P3(except P33/$\overline{HOLD}$), P6, P9 and $\overline{RES}$.<br>OSC1 | With output Nch transistor "OFF" | | 4.5 to 5.5 | Vss | | $0.25V_{DD}$ | V | 2 |
| | | | $V_{IL}$(2) | P33/$\overline{HOLD}$ | | | 1.8 to 5.5 | Vss | | $0.25V_{DD}$ | V | |
| | | | $V_{IL}$(3) | P0, P1, P4, P5, PC, PD, PE, TEST | With output Nch transistor "OFF" | | 4.5 to 5.5 | Vss | | $0.3V_{DD}$ | V | 3 |
| | | | $V_{IL}$(4) | PE | With tristate input mode selected. | | 4.5 to 5.5 | Vss | | $0.2V_{DD}$ | V | |
| Operating frequency (instruction cycle time) | | | fop (TCYC) | | | | 4.5 to 5.5 | 0.4 (10) | | 4.35 (0.92) | MHz (µs) | |
| External clock input mode | Frequency | | fext | OSC1 | Please refer to Figure 1. As it shows, input clocks reach the OSCI pin from an external clock source and the OSC2 pin should be left open. The oscillation circuit option should be "external clock input". | | 4.5 to 5.5 | 0.4 | | 4.35 | MHz | |
| | Pulse width | | textH textL | | Please refer to Figure 1. As it shows, input clocks reach the OSC1 pin from an external clock source and the OSC2 pin should be left open. The oscillation circuit option should be "external clock input". | | 4.5 to 5.5 | 70 | | | ns | |
| | Rise and Fall times | | textR textF | | Please refer to Figure 1. As it shows, input clocks reach the OSC1 pin from an external clock source and the OSC2 pin should be left open. The oscillation circuit option should be "external clock input". | | 4.5 to 5.5 | | | 30 | ns | |
| self oscillation mode | Ceramic resonator oscillation | Oscillation frequency | $f_{CF}$ | OSC1, OSC2 | Refer to Figure 2. | 4MHz | 4.5 to 5.5 | | 4.0 | | MHz | |
| | | Oscillation stabilization time period | $t_{CFS}$ | | Refer to Figure 3 | 4MHz | 4.5 to 5.5 | | | 10 | ms | |
| | External R and C constants | | Cext<br>Rext | OSC1, OSC2 | Refer to Figure 4 | | 4.5 to 5.5 | | 100<br>2.2 | | pF<br>kΩ | |

Note 1: These values apply to the case where the open-drain circuit type has been specified. Note that the P33/$\overline{HOLD}$ pin is not included (refer to the values listed in $V_{IH}$ (2) column and that the pins P2, P3 and P6 cannot be used as the input pins as far as the CMOS output circuit type has been employed.

Note 2: These values apply to the case where the open drain circuit type has been selected. Note that the pin P9 cannot be used as the input pin as far as the CMOS type output circuit has been employed.

Note 3: When the pin PE has been selected as the tristate input pin, the values listed in the $V_{IH}$(4), $V_{IM}$ and $V_{IL}$(4) columns should apply to the pin. Note that the pin PC cannot be used as the input pin as far as the CMOS type output circuit has been employed.

**Electrical characteristics** at Ta = 10˚C to 40°C, $V_{SS}$=0V, unless otherwise noted

| Parameter | Symbol | Pins applicable | Conditions | | Ratings | | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$(V) | min | typ | max | | |
| Input high-level current | $I_{IH}$(1) | P2, P3(except P33/ $\overline{HOLD}$) and P6. | $V_{IN}$ = 13.5V With output Nch transistor "OFF" | 4.5 to 5.5 | | | 5.0 | µA | 1 |
| | $I_{IH}$(2) | P0, P1, P4, P5, P9, PC, OSC1, $\overline{RES}$ and P33/ $\overline{HOLD}$. Note that the PD, PE, PC2, and PC3 are not included. | $V_{IN}$ = $V_{DD}$ With output Nch transistor "OFF" | 4.5 to 5.5 | | | 1.0 | µA | 1 |
| | $I_{IH}$(3) | PD, PE, PC2, PC3 | $V_{IN}$ = $V_{DD}$ With output Nch transistor "OFF" | 4.5 to 5.5 | | | 1.0 | µA | 1 |
| Input low-level current | $I_{IL}$(1) | Input pins otner than PD, PE, PC2 and PC3 | $V_{IN}$ = Vss With output Nch transistor "OFF" | 4.5 to 5.5 | –1.0 | | | µA | 2 |
| | $I_{IL}$(2) | PC2, PC3, PD, PE | $V_{IN}$ = Vss With output Nch transistor "OFF" | 4.5 to 5.5 | –1.0 | | | µA | 2 |
| Output high-level voltage | $V_{OH}$(1) | P2, P3(except P33/ $\overline{HOLD}$), P6, P8, P9, and PC. | $I_{OH}$ = –1mA | 4.5 to 5.5 | $V_{DD}$–1.0 | | | V | 3 |
| | | | $I_{OH}$ = –0.1mA | 4.5 to 5.5 | $V_{DD}$–0.5 | | | V | 3 |
| | $V_{OH}$(2) | P0, P1, P4, P5, P7, PA, PB | IOH = –200µA | 4.5 | 2.4 | | | V | 4 |
| | | | $I_{OH}$ = –130µA | 4.5 to 5.5 | $V_{DD}$–1.35 | | | V | 4 |
| Output pull-up current | $I_{PO}$ | P0, P1, P4, P5, P7, PA, PB | $V_{IN}$ = Vss | 5.5 | –1.6 | | | mA | 4 |
| Output low-level voltage | $V_{OL}$(1) | PO, P1, P2, P3, P4, P5, P6, P8, P9 and PC (except P33/ $\overline{HOLD}$). | $I_{OL}$ = 1.6mA | 4.5 to 5.5 | | | 0.4 | V | 5 |
| | $V_{OL}$(2) | P7, PA, PB | $I_{OL}$ = 10mA | 4.5 to 5.5 | | | 1.5 | V | |
| Output-OFF leakage current | $I_{OFF}$(1) | P2, P3, P6, P7, PA | $V_{IN}$ = 13.5V | 4.5 to 5.5 | | | 5.0 | µA | 6 |
| | $I_{OFF}$(2) | Pins other than P2, P3, P6, P7, P8 and PA | $V_{IN}$ = $V_{DD}$ | 4.5 to 5.5 | | | 1.0 | µA | 6 |
| | $I_{OFF}$(3) | P8 | $V_{IN}$ = Vss | 4.5 to 5.5 | –1.0 | | | µA | 7 |
| Comparator offset current | $V_{OFF}$ | PD | $V_{IN}$ = 1.0V to $V_{DD}$–l.5V | 4.5 to 5.5 | | ±50 | ±300 | mV | |
| Schmitt characteristics: Hysteresis voltage | $V_{HYS}$ | P2, P3, $\overline{RES}$, P6, P9, OSC1 (RC, EXT) | | 4.5 to 5.5 | | 0.1$V_{DD}$ | | V | |
| Schmitt characteristics: High-level threshold voltage | Vt H | | | | 0.5$V_{DD}$ | | 0.75$V_{DD}$ | V | |
| Schmitt characteristics: Low-level threshold voltage | Vt L | | | | 0.25$V_{DD}$ | | 0.5$V_{DD}$ | V | |
| RC oscillation frequency range | $f_{RC}$ | OSC1, OSC2 | Refer to Figure 4. C =100pF ±5% R = 2.2kΩ ±1% | 4.5 to 5.5 | 2.0 | 3.0 | 4.0 | MHz | |

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| Parameter | | | symbol | Pins applicable | | Conditions | $V_{DD}$(V) | Ratings min | Ratings typ | Ratings max | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Serial timing clock | Cycle time | Data input | $t_{CKCY}$ | $\overline{SCK0}$, $\overline{SCK1}$ | | Refer to Figure 5 (timings) and Figure6 (test load). | 4.5 to 5.5 | 0.9 | | | µs | |
| | | Data output | | | | | 4.5 to 5.5 | 2.0 | | | $T_{CYC}$ | |
| | Low-level and high-level pulse width | Data input | $t_{CKL}$ | | | | 4.5 to 5.5 | 0.4 | | | µs | |
| | | Data output | $t_{CKH}$ | | | | 4.5 to 5.5 | 1.0 | | | $T_{CYC}$ | |
| | Rise and fall time | Data output | $t_{CKR}$ $t_{CKF}$ | | | | 4.5 to 5.5 | | | 0.1 | µs | |
| Serial input | Data setup time | | $t_{ICK}$ | SI0, SI1 | | Refer to Figure 5 (timings). Time periods based on the $\overline{SCK0}$ and $\overline{SCK1}$ clock rising edges(↑). | 4.5 to 5.5 | 0.3 | | | µs | |
| | Data HOLD time | | $t_{CKI}$ | | | | 4.5 to 5.5 | 0.3 | | | µs | |
| Serial output | Output delay time | | $t_{CKO}$ | SO0, SO1 | | Refer to Figure 5 (timings) and Figure 6 (test load). Time period based on the $\overline{SCK0}$ and $\overline{SCK1}$ clock falling edges(↓). | 4.5 to 5.5 | | | 0.3 | µs | |
| Pulse input conditions | INT0 high-level and low-level pulse width | | $t_{I0H}$ $t_{I0L}$ | INT0 | Refer to Figure 7.- | · With INTO interrupt request input acceptable · With event counter (timer 0) input or pulse width measuring input acceptable | 4.5 to 5.5 | 2 | | | $T_{CYC}$ | |
| | High-level and low-level pulse width (INTO not included) | | $t_{I1H}$ $t_{I1L}$ | $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT4}$, $\overline{INT5}$ | | · With interrupt request inputs acceptable | | 2 | | | $T_{CYC}$ | |
| | PIN1 high-level and low-level pulse width | | $t_{PINH}$ $t_{PINL}$ | PIN1 | | ·With event counter (timer 1) input acceptable | | 2 | | | $T_{CYC}$ | |
| | $\overline{RES}$ high-level and low-level pulse width | | $t_{RSH}$ $t_{RSL}$ | $\overline{RES}$ | | · With reset request acceptable | | 3 | | | $T_{CYC}$ | |
| Comparator response speed | | | $t_{CRS}$ | PD | Refer to Figure 8. | | 4.5 to 5.5 | | | 30 | µs | |
| Current drain during basis operation mode | | | $I_{DD}$ OP | $V_{DD}$ | | 4 MHz ceramic resonator oscillation | 4.5 to 5.5 | | 4.5 | 8 | mA | 8 |
| | | | | | | 4 MHz external clock source | | | 6.5 | 11 | mA | |
| | | | | | | RC oscillation | | | 4.0 | 8 | mA | |

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| Parameter | symbol | Pin applicable | Conditions | $V_{DD}$(V) | Limits min | Limits typ | Limits max | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| Current drain during HALT operation mode | $I_{DDHALT}$ | $V_{DD}$ | 4 MHz ceramic resonator oscillation | 4.5 to 5.5 | | 2.5 | 4.5 | mA | |
| | | | 4 MHz external clock source | | | 3.5 | 6.0 | mA | |
| | | | RC oscillation | | | 2.5 | 4.5 | mA | |
| Current drain during HOLD operation mode | $I_{DDHOLD}$ | $V_{DD}$ | | 1.8 to 5.5 | | 0.01 | 10 | μA | |

Note 1: Applicable to the case where input/output common ports have been set to open-drain output circuit type and the output Nch transistors have been in OFF state. Note that the input/output common ports cannot be used as the input port if they have been set to the CMOS output circuit type.

Note 2: Applicable to the case where input/output common ports have been set to open-drain output circuit type and the output Nch transistors have been in OFF state. If the pull-up transistor output circuit type has been employed, please refer to the value listed in the output pull-up current column (IPO). Note that input/output common ports cannot be used as the input ports if they have been set to the CMOS output circuit type.

Note 3: Applicable to the case where the ports have been set to the CMOS output circuit type and the output Nch transistors have been in OFF state. Also applicable to the P8 pin as far as it has been set to the Pch open-drain output circuit type.

Note 4: Applicable to the case where the ports have been set to the pull-up resistor output circuit type and the output Nch transistors have been in OFF state.

Note 5: Applicable to the case where the P8 pin has been set to the CMOS output circuit type.

Note 6: Applicable to the case where the ports have been set to the open-drain output circuit type and the output Nch transistors have been in OFF state.

Note 7: Applicable to the case where the port has been set to the open-drain output circuit type and the output Pch transistor has been in OFF state.

Note 8: Reset mode.

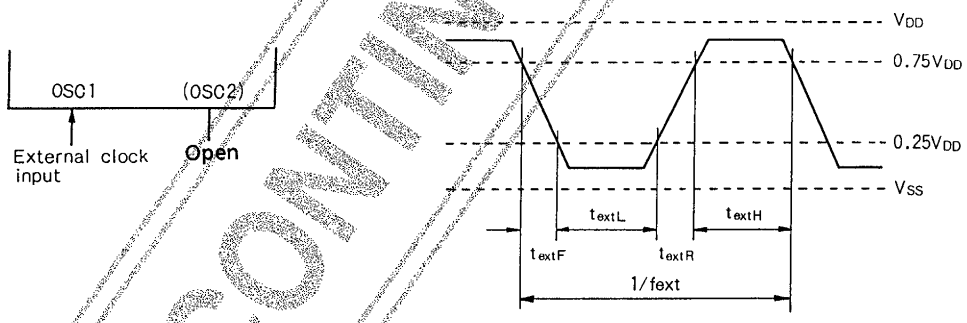


Figure 1. External clock input waveform

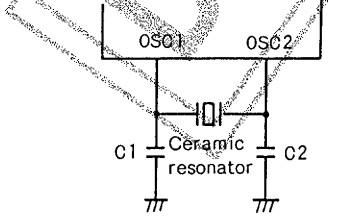


Figure 2. Ceramic resonator oscillation circuit

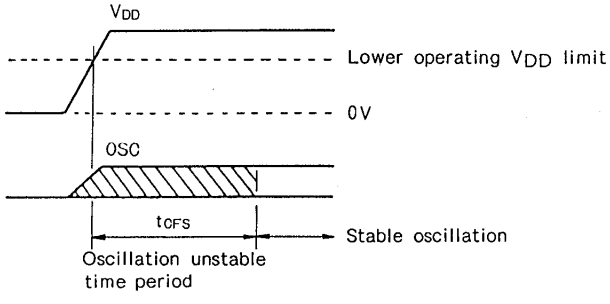


Figure 3. Oscillation stabilization time

| | | | |
|---|---|---|---|
| Capacitance (external) | 4 MHz (Murata) CSA4.00MG | C1 | 33pF±10% |
| | | C2 | 33pF±10% |
| | 4 MHz (Kyocera) KBR4.0MS | C1 | 33pF±10% |
| | | C2 | 33pF±10% |
| Capacitance (internal) | 4 MHz (Murata) CST4.00MG | | |
| | 4 MHz (Kyocera) KBR–4.0MES | | |

Table 1. Ceramic resonator oscillation constants (recommended)

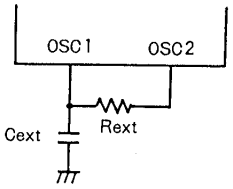


Figure 4. RC oscillation

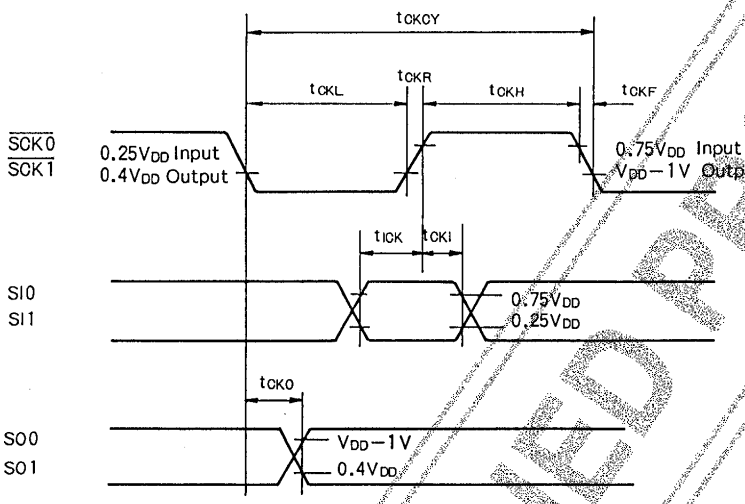


Figure 5. Serial input/output timings

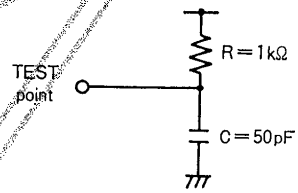


Figure 6. Timing load

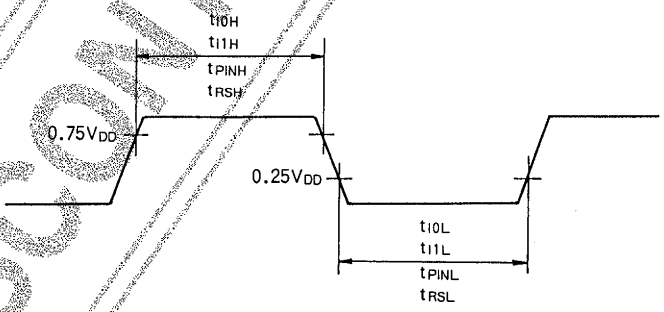


Figure 7. Input timings for INT0, $\overline{\text{INT1}}$, $\overline{\text{INT2}}$, $\overline{\text{INT3}}$, $\overline{\text{INT4}}$, INT5, PIN1 and $\overline{\text{RES}}$

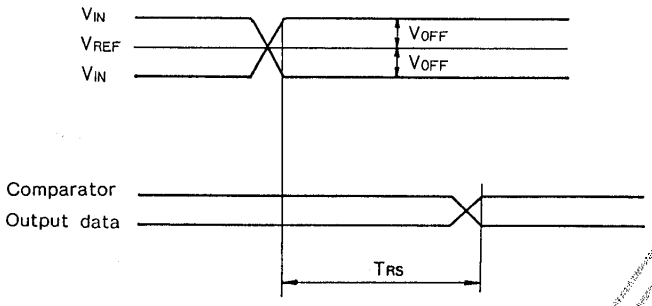


Figure 8. Comparator response speed (TRS) and output timing

### LC66E516 RC oscillation characteristics

Figure 9 shows the RC oscillation characteristics of the LC66E516 microcontroller.
The RC oscillation frequency range that can be guaranteed is shown below with the external constants and other conditions:

2.0MHz ≦ fRC ≦ 4.0MHz

External constants --- Cext = 100pF and Rext = 2.2kΩ
Ta = 10°C to 40°C and $V_{DD}$ = 4.5V to 5.5V

If you are to employ the external constants other than the above, the Rext and the Cext should be within the range between T.B.D kΩ and T.B.D kΩ, and between T.B.D pF and T.B.D pF, respectively. Please take a close look at the figure below.
Note 10: With $V_{DD}$ = 4.5V to 5.5V and Ta = 10°C to 40°C, the oscillation frequency to be selected should meet the requirement that the operating frequencies in the range between 0.4MHz and 4.3MHz must be provided without fail.

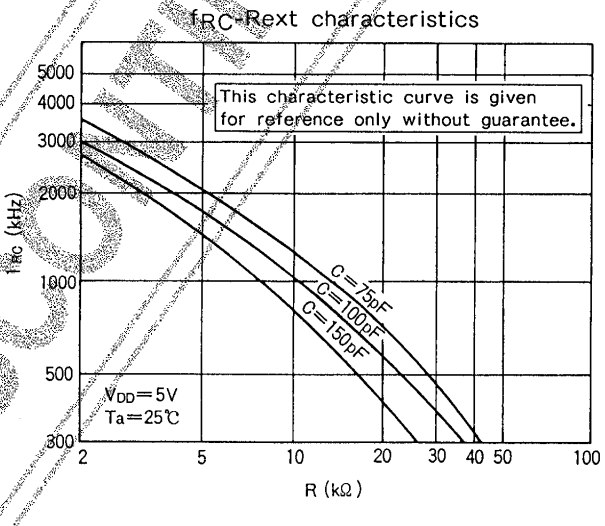


Figure 9. RC oscillation frequency reference values

## Series Lineup

| Type Number | Pins | ROM capacity | RAM cap | Package | Features |
|---|---|---|---|---|---|
| LC66304A/306A/308A | 42 | 4K/6K/8KB | 512W | DIP42S QFP48E | Normal version<br>4.0 to 6.0V/0.92µs |
| LC66404A/406/408A | 42 | 4K/6K/8KB | 512W | DIP42S QFP48E | |
| LC66506B/508B/512B/516B | 64 | 6K/8K/12K/16KB | 512W | DIP64S QFP64A | |
| LC66354A/356A/358A | 42 | 4K/6K/8KB | 512W | DIP42S QFP48E | Low voltage version<br>2.2 to 5.5V/0.92µs |
| LC66354S/356S/358S * | 42 | 4K/6K/8KB | 512W | QFP44M | |
| LC66556A/558A/562A/566A | 64 | 6K/8K/12K/16KB | 512W | DIP64S QFP64E | |
| LC66354B/356B/358B | 42 | 4K/6K/8KB | 512W | DIP42S QFP48E | Low voltage high-speed version*3.0 to 5.5V/0.92µs |
| LC66556B/558B | 64 | 6K/8KB | 512W | DIP64S QFP64E | |
| LC66562B/566B | 64 | 12K/16KB | 512W | DIP64S QFP64E | |
| LC66E308 | 42 | EPROM 8KB | 512W | DIC42S* QFC48* | Evaluation-use windowed version & one-time version<br>4.5 to 5.5V/0.92µs<br><br>*:with window |
| LC66P308 | 42 | OTPROM 8KB | 512W | DIP42S QFP48E | |
| LC66E408 | 42 | EPROM 8KB | 512W | DIC42S* QFC48* | |
| LC66P408 | 42 | OTPROM 8KB | 512W | DIP42S QFP48E | |
| LC66E516 | 64 | EPROM 16KB | 512W | DIC64S* QFC64* | |
| LC66P516 | 64 | OTPROM 16KB | 512W | DIP64S QFP64E | |

*Note : Under develoment