

**EVALUATION KIT
AVAILABLE**

MAXIM

65Msps, 12-Bit, IF Sampling ADC

MAX1211

General Description

The MAX1211 is a 3.3V, 12-bit analog-to-digital converter (ADC) featuring a fully differential wideband track-and-hold (T/H) input, driving the internal quantizer. The MAX1211 is optimized for low power, small size, and high dynamic performance in intermediate frequency (IF) sampling applications. This ADC operates from a single 3.0V to 3.6V supply, consuming only 358mW while delivering a typical signal-to-noise ratio (SNR) performance of 66dB at an input frequency of 175MHz. The T/H driven input stage accepts single-ended or differential inputs. In addition to low operating power, the MAX1211 features a 13mW power-down mode to conserve power during idle periods.

A flexible reference structure allows the MAX1211 to use its internal precision bandgap reference or accept an externally applied reference.

The MAX1211 supports both a single-ended and differential input clock drive. Wide variations in the clock duty cycle are compensated with the ADC's internal duty-cycle equalizer.

The MAX1211 features parallel, CMOS-compatible outputs. The digital output format is pin selectable to be either two's complement or Gray code. A separate power input for the digital outputs accepts a voltage from 1.7V to 3.6V for flexible interfacing with various logic levels. The MAX1211 is available in a 6mm x 6mm x 0.8mm, 40-pin thin QFN package with exposed paddle (EP), and is specified for the extended industrial (-40°C to +85°C) temperature range.

Applications

IF and Baseband Communication Receivers
Cellular, LMDS, Point-to-Point Microwave,
MMDS, HFC, WLAN

Ultrasound and Medical Imaging

Portable Instrumentation

Low-Power Data Acquisition

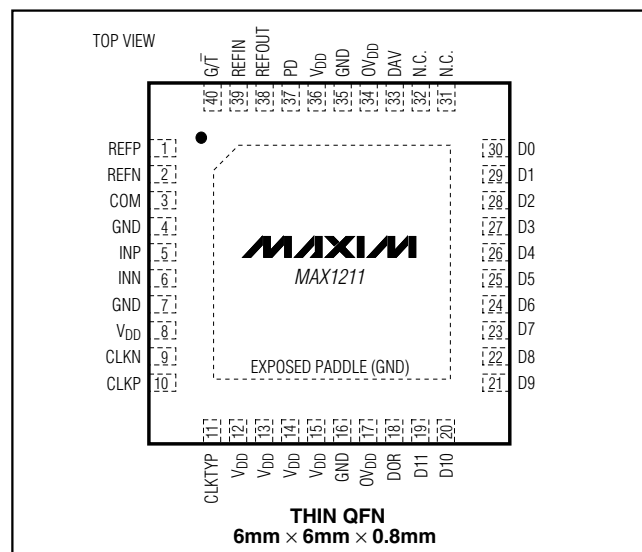
Features

- ◆ Direct IF Sampling Up to 400MHz
- ◆ Excellent Dynamic Performance
 - 66dB SNR at $f_{IN} = 175\text{MHz}$
 - 76dBc SFDR at $f_{IN} = 175\text{MHz}$
- ◆ Differential or Single-Ended Clock
- ◆ 3.3V Low-Power Operation
 - 358mW (Differential Clock Mode)
 - 327mW (Single-Ended Clock Mode)
- ◆ Accepts 20% to 80% Clock Duty Cycle
- ◆ Fully Differential or Single-Ended Analog Input
- ◆ Wide $\pm 1\text{V}_{p-p}$ Differential Analog Input Voltage Range
- ◆ 700MHz Input Bandwidth
- ◆ Power-Down Mode
- ◆ CMOS-Compatible Outputs in Two's Complement or Gray Code
- ◆ Out-of-Range and Data Valid Indicators
- ◆ Small, 40-Pin Thin QFN Package with Exposed Paddle
- ◆ Evaluation Kit Available (Order MAX1211EVKIT)

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1211ETL	-40°C to +85°C	40 Thin QFN 6mm x 6mm

Pin Configuration



MAXIM

Maxim Integrated Products 1

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

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ABSOLUTE MAXIMUM RATINGS

V _{DD} to GND	-0.3V to +3.6V	Continuous Power Dissipation (T _A = +70°C)	
OV _{DD} to GND	-0.3V to the lower of (V _{DD} + 0.3V) and +3.6V	40-Pin Thin QFN 6mm x 6mm x 0.8mm	
INP, INN to GND ...	-0.3V to the lower of (V _{DD} + 0.3V) and +3.6V	(derated 26.3mW/°C above +70°C).....	2105.3mW
REFIN, REFOUT, REFP, REFN,		Operating Temperature Range	-40°C to +85°C
COM to GND	-0.3V to the lower of (V _{DD} + 0.3V) and +3.6V	Junction Temperature	+150°C
CLKP, CLKN, CLKTYP, G/T,		Storage Temperature Range	-65°C to +150°C
PD to GND	-0.3V to the lower of (V _{DD} + 0.3V) and +3.6V	Lead Temperature (soldering 10s)	+300°C
D11–D0, DAV, DOR to GND.....	-0.3V to (OV _{DD} + 0.3V)		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.3V, OV_{DD} = 2.0V, GND = 0, REFIN = REFOUT (internal reference), C_{REFOUT} = 0.1μF, C_L ≈ 5pF at digital outputs, V_{IN} = -0.2dBFS, CLKTYP = high, PD = low, G/T = low, f_{CLK} = 65MHz (50% duty cycle), C_{REFP} = C_{REFN} = 0.1μF to GND, 10μF between REFP and REFN, C_{COM} = 0.1μF in parallel with 2.2μF to GND, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution			12			Bits
Integral Nonlinearity	INL	f _{IN} = 20MHz		±0.8		LSB
Differential Nonlinearity	DNL	f _{IN} = 20MHz, no missing codes over temperature		±0.30	±0.95	LSB
Offset Error		V _{REFIN} = 2.048V		±0.1	±1.2	%FS
Gain Error		V _{REFIN} = 2.048V		±1.0		%FS
ANALOG INPUT (INP, INN)						
Differential Input Voltage Range	V _{DIFF}	Differential or single-ended inputs		±1		V
Common-Mode Input Voltage				V _{DD} / 2		V
Input Resistance	R _{IN}	Switched capacitor load		15		kΩ
Input Capacitance	C _{IN}			4		pF
CONVERSION RATE						
Maximum Clock Frequency	f _{CLK}		65			MHz
Minimum Clock Frequency					5	MHz
Data Latency				8.5		Clock cycles
DYNAMIC CHARACTERISTICS (differential inputs, 4096-point FFT)						
Signal-to-Noise Ratio	SNR	f _{IN} = 32.4MHz at -0.2dBFS		67.2		dB
		f _{IN} = 175MHz at -0.2dBFS		66.1		
		f _{IN} = 250MHz at -0.2dBFS		65.1		
Signal-to-Noise and Distortion	SINAD	f _{IN} = 32.4MHz at -0.2dBFS		67		dB
		f _{IN} = 175MHz at -0.2dBFS		65.3		
		f _{IN} = 250MHz at -0.2dBFS		63.1		
Spurious-Free Dynamic Range	SFDR	f _{IN} = 32.4MHz at -0.2dBFS		81.4		dBc
		f _{IN} = 175MHz at -0.2dBFS		76		
		f _{IN} = 250MHz at -0.2dBFS		68		

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ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = 3.3V$, $OV_{DD} = 2.0V$, $GND = 0$, $REFIN = REFOUT$ (internal reference), $C_{REFOUT} = 0.1\mu F$, $C_L \approx 5pF$ at digital outputs, $V_{IN} = -0.2dBFS$, $CLKTYP = high$, $PD = low$, $G/\bar{T} = low$, $f_{CLK} = 65MHz$ (50% duty cycle), $C_{REFP} = C_{REFN} = 0.1\mu F$ to GND , $10\mu F$ between $REFP$ and $REFN$, $C_{COM} = 0.1\mu F$ in parallel with $2.2\mu F$ to GND , $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Total Harmonic Distortion	THD	$f_{IN} = 32.4MHz$ at $-0.2dBFS$		-79		dBc
		$f_{IN} = 175MHz$ at $-0.2dBFS$		-73		
		$f_{IN} = 250MHz$ at $-0.2dBFS$		-67.3		
Third-Order Intermodulation	IM3	$f_{IN1} = 247.2MHz$ at $-7dBFS$ $f_{IN2} = 253.6MHz$ at $-7dBFS$		-73.3		dBc
Full-Power Bandwidth	FPBW	Input at $-0.2dBFS$, $-3dB$ rolloff		700		MHz
Aperture Delay	t_{AD}			0.9		ns
Aperture Jitter	t_{AJ}			<0.2		psRMS
Output Noise	n_{OUT}	INP = INN = COM		0.6		LSBRMS
Overdrive Recovery Time		$\pm 10\%$ beyond full scale		1		Clock cycles
INTERNAL REFERENCE ($REFIN = REFOUT$; V_{REFP} , V_{REFN} , and V_{COM} are generated internally)						
REFOUT Output Voltage	V_{REFOUT}		1.9	2.048	2.1	V
COM Output Voltage	V_{COM}	$V_{DD} / 2$		1.65		V
Differential Reference Output Voltage	V_{REF}	$V_{REF} = V_{REFP} - V_{REFN}$		1.024		V
REFOUT Load Regulation				35		mV/mA
REFOUT Temperature Coefficient	TC_{REF}			+100		ppm/ $^\circ C$
REFOUT Short-Circuit Current		Short to V_{DD}		0.24		mA
		Short to GND		2.1		
BUFFERED EXTERNAL REFERENCE ($REFIN$ driven externally, $V_{REFIN} = 2.048V$, V_{REFP} , V_{REFN} , and V_{COM} are generated internally)						
REFIN Input Voltage	V_{REFIN}			2.048		V
REFP Output Voltage	V_{REFP}	$(V_{DD} / 2) + (V_{REFIN} / 4)$		2.162		V
REFN Output Voltage	V_{REFN}	$(V_{DD} / 2) - (V_{REFIN} / 4)$		1.138		V
COM Output Voltage	V_{COM}	$V_{DD} / 2$	1.6	1.65	1.7	V
Differential Reference Output Voltage	V_{REF}	$V_{REF} = V_{REFP} - V_{REFN}$		1.024		V
Maximum REFP Current	I_{REFP}	Source		0.4		mA
		Sink		1.4		
Maximum COM Current	I_{REFP}	Source		1.0		mA
		Sink		0.4		
Maximum REFN Current	I_{REFP}	Source		1.0		mA
		Sink		1.0		
REFIN Input Resistance				>50		$M\Omega$

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ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = 3.3V$, $OV_{DD} = 2.0V$, $GND = 0$, $REFIN = REFOUT$ (internal reference), $C_{REFOUT} = 0.1\mu F$, $C_L \approx 5pF$ at digital outputs, $V_{IN} = -0.2dBFS$, $CLKTYP = high$, $PD = low$, $G/\bar{T} = low$, $f_{CLK} = 65MHz$ (50% duty cycle), $C_{REFP} = C_{REFN} = 0.1\mu F$ to GND , $10\mu F$ between $REFP$ and $REFN$, $C_{COM} = 0.1\mu F$ in parallel with $2.2\mu F$ to GND , $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
UNBUFFERED EXTERNAL REFERENCE ($REFIN = GND$, V_{REFP} , V_{REFN} , and V_{COM} are applied externally)						
COM Input Voltage	V_{COM}			$V_{DD} / 2$		V
REFP Input Voltage		$V_{REFP} - V_{COM}$		0.512		V
REFN Input Voltage		$V_{REFN} - V_{COM}$		-0.512		V
Differential Reference Input Voltage	V_{REF}	$V_{REF} = V_{REFP} - V_{REFN}$		1.024		V
REFP Sink Current	I_{REFP}	$V_{REFP} = 2.162V$		1.1		mA
REFN Source Resistance	I_{REFN}	$V_{REFP} = 1.138V$		1.1		mA
REFP, REFN, Capacitance				13		pF
Com Capacitance				6		pF
CLOCK INPUTS ($CLKP$, $CLKN$)						
Single-Ended Input High Threshold	V_{IH}	$CLKTYP = GND$, $CLKN = GND$		$0.8 \times V_{DD}$		V
Single-Ended Input Low Threshold	V_{IL}	$CLKTYP = GND$, $CLKN = GND$			$0.2 \times V_{DD}$	V
Differential Input Voltage Swing		$CLKTYP = high$		0.7		V
Differential Input Common-Mode Voltage		$CLKTYP = high$		$V_{DD} / 2$		V
Clock Duty Cycle				50		%
Clock Duty-Cycle Tolerance				± 30		%
Input Capacitance	C_{IN}			2		pF
DIGITAL INPUTS ($CLKTYP$, G/\bar{T} , PD)						
Input High Threshold	V_{IH}			$0.8 \times OV_{DD}$		V
Input Low Threshold	V_{IL}				$0.2 \times OV_{DD}$	V
Input Leakage Current		$V_{IH} = OV_{DD}$			± 5	μA
		$V_{IL} = 0$			± 5	
Input Capacitance	C_{IN}			2		pF
DIGITAL OUTPUTS ($D0-D11$, DAV , DOR)						
Output-Voltage Low	V_{OL}	$D0-D11$, DOR , $I_{SINK} = 200\mu A$			0.2	V
		DAV , $I_{SINK} = 600\mu A$			0.1	
Output-Voltage High	V_{OH}	$D0-D11$, DOR , $I_{SOURCE} = 200\mu A$		$OV_{DD} - 0.2$		V
		DAV , $I_{SOURCE} = 600\mu A$		$OV_{DD} - 0.1$		
Tri-State Leakage Current	I_{LEAK}	(Note 2)		$< \pm 5$		μA

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ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = 3.3V$, $OV_{DD} = 2.0V$, $GND = 0$, $REFIN = REFOUT$ (internal reference), $C_{REFOUT} = 0.1\mu F$, $C_L \approx 5pF$ at digital outputs, $V_{IN} = -0.2dBFS$, $CLKTYP = high$, $PD = low$, $G/\bar{T} = low$, $f_{CLK} = 65MHz$ (50% duty cycle), $C_{REFP} = C_{REFN} = 0.1\mu F$ to GND , $10\mu F$ between $REFP$ and $REFN$, $C_{COM} = 0.1\mu F$ in parallel with $2.2\mu F$ to GND , $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
D11–D0, DOR Tri-State Output Capacitance	C_{OUT}	(Note 2)		3		pF
DAV Tri-State Output Capacitance	C_{OUT}	(Note 2)		6		pF
POWER REQUIREMENTS						
Analog Supply Voltage	V_{DD}		3.0	3.3	3.6	V
Digital Output Supply Voltage	OV_{DD}		1.7	2.0	$V_{DD} + 0.3V$	V
Analog Supply Current	I_{VDD}	Normal operating mode, $f_{IN} = 32.4MHz$ at $-0.2dBFS$, $CLKTYP = GND$, single-ended clock		99		mA
		Normal operating mode, $f_{IN} = 32.4MHz$ at $-0.2dBFS$, $CLKTYP = OV_{DD}$, differential clock		108	121	
		Power-down mode; clock idle, $PD = OV_{DD}$		4	12	
Analog Power Dissipation	P_{DISS}	Normal operating mode, $f_{IN} = 32.4MHz$ at $-0.2dBFS$, $CLKTYP = GND$, single-ended clock		327		mW
		Normal operating mode, $f_{IN} = 32.4MHz$ at $-0.2dBFS$, $CLKTYP = OV_{DD}$, differential clock		358	400	
		Power-down mode, clock idle, $PD = OV_{DD}$		13	40	
Digital Output Supply Current	I_{OVDD}	Normal operating mode, $f_{IN} = 32.4MHz$ at $-0.2dBFS$, $OV_{DD} = 2.0V$, $C_L \approx 5pF$		10		mA
		Power-down mode; clock idle, $PD = OV_{DD}$		19		μA

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ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = 3.3V$, $OV_{DD} = 2.0V$, $GND = 0$, $REFIN = REFOUT$ (internal reference), $C_{REFOUT} = 0.1\mu F$, $C_L \approx 5pF$ at digital outputs, $V_{IN} = -0.2dBFS$, $CLKTYP = high$, $PD = low$, $G/\bar{T} = low$, $f_{CLK} = 65MHz$ (50% duty cycle), $C_{REFP} = C_{REFN} = 0.1\mu F$ to GND , $10\mu F$ between $REFP$ and $REFN$, $C_{COM} = 0.1\mu F$ in parallel with $2.2\mu F$ to GND , $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS (Figure 5)						
Clock Pulse Width High	t_{CH}			7.7		ns
Clock Pulse Width Low	t_{CL}			7.7		ns
Data Valid Delay	t_{DAV}	$C_L = 5pF$ (Note 3)		6.4		ns
Data Setup Time Before Rising Edge of DAV	t_{SETUP}	$C_L = 5pF$ (Note 3)		8.4		ns
Data Hold Time After Rising Edge of DAV	t_{HOLD}	$C_L = 5pF$ (Note 3)		6.6		ns
Wake-Up Time from Power-Down	t_{WAKE}	$V_{REFIN} = 2.048V$		10		ms

Note 1: Specifications $\geq +25^\circ C$ guaranteed by production test, $< +25^\circ C$ guaranteed by design and characterization.

Note 2: During power-down, D11–D0, DOR, and DAV are high impedance.

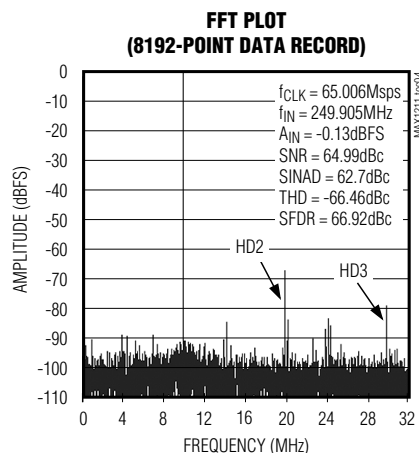
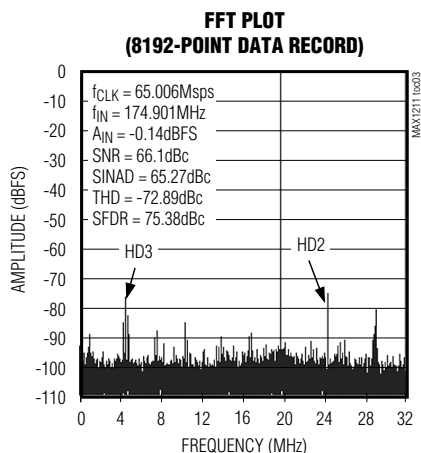
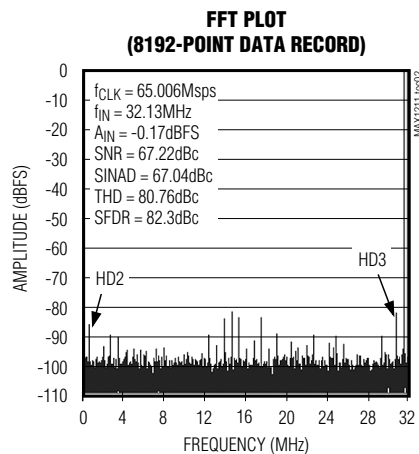
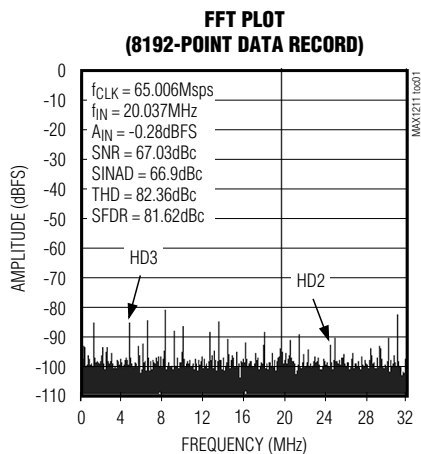
Note 3: Digital outputs settle to V_{IH} or V_{IL} .

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Typical Operating Characteristics

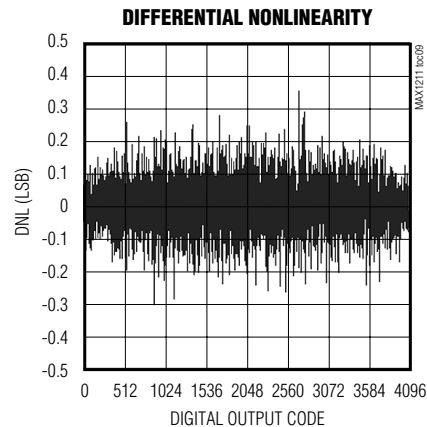
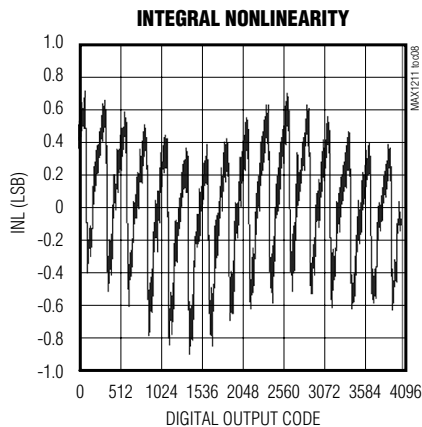
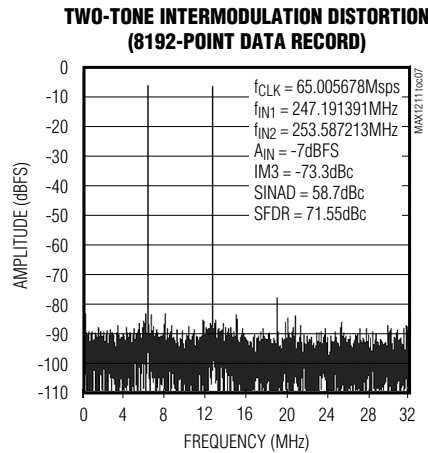
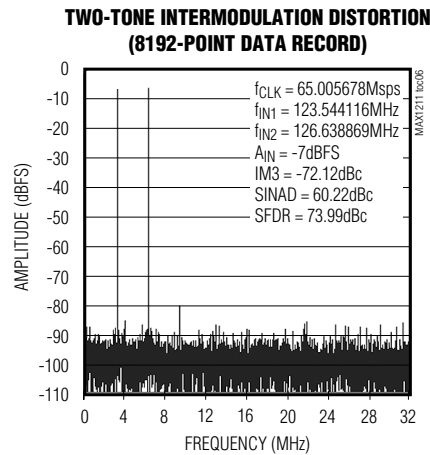
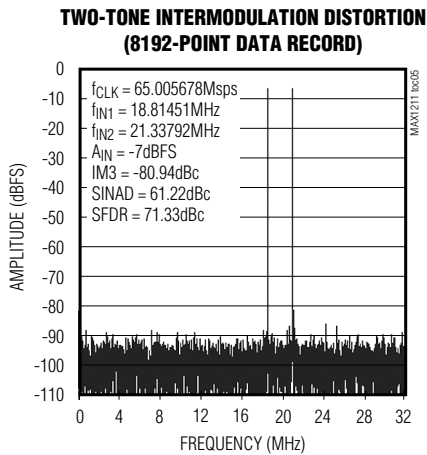
($V_{DD} = 3.3V$, $OV_{DD} = 2.0V$, $GND = 0$, $REF_{IN} = REF_{OUT}$ (internal reference), $C_{REF_{OUT}} = 0.1\mu F$, $C_L \approx 8pF$ at digital outputs, differential input at $-0.2dBFS$, $CLK_{TYP} = high$, $PD = low$, $G/\bar{T} = low$, $f_{CLK} = 65.005678MHz$ (50% duty cycle), $C_{REFP} = C_{REFN} = 0.1\mu F$ in parallel with $10\mu F$ to GND , $10\mu F$ between $REFP$ and $REFN$, $C_{COM} = 0.1\mu F$ in parallel with $2.2\mu F$ to GND , $T_A = +25^\circ C$, unless otherwise noted.)



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Typical Operating Characteristics (continued)

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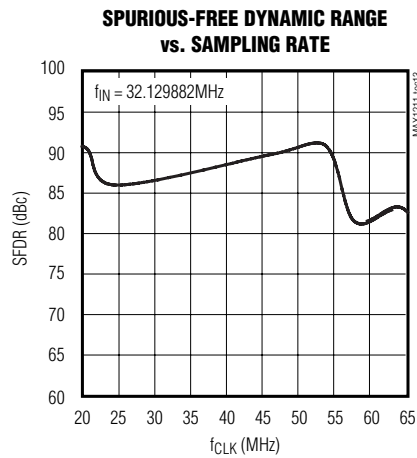
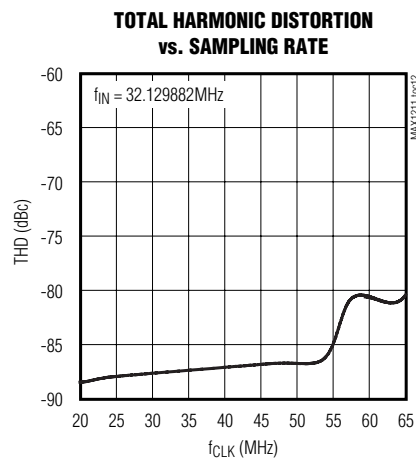
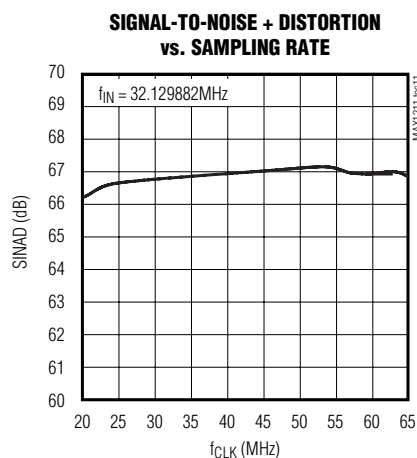
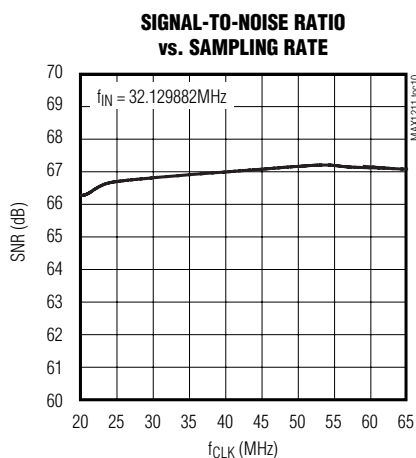


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Typical Operating Characteristics (continued)

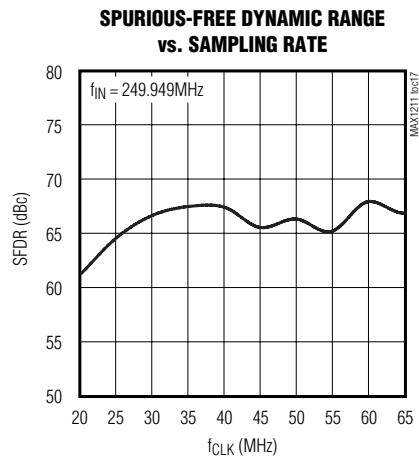
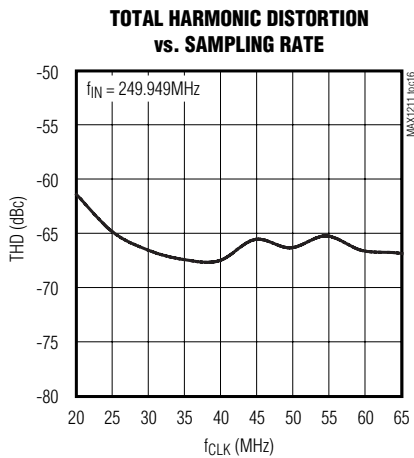
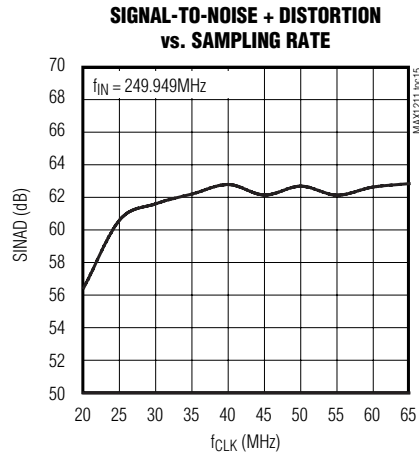
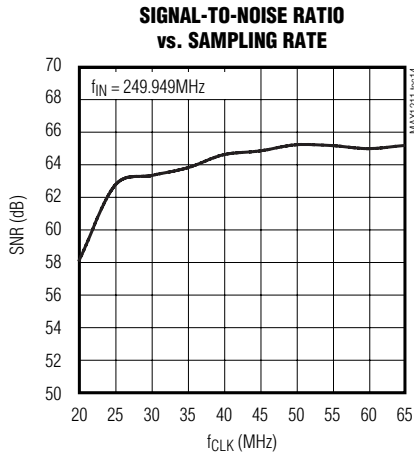
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65Msps, 12-Bit, IF Sampling ADC

Typical Operating Characteristics (continued)

($V_{DD} = 3.3V$, $OV_{DD} = 2.0V$, $GND = 0$, $REF_{IN} = REF_{OUT}$ (internal reference), $C_{REFOUT} = 0.1\mu F$, $C_L \approx 8pF$ at digital outputs, differential input at $-0.2dBFS$, $CLK_{TYP} = high$, $PD = low$, $G/\bar{T} = low$, $f_{CLK} = 65.005678MHz$ (50% duty cycle), $C_{REFP} = C_{REFN} = 0.1\mu F$ in parallel with $10\mu F$ to GND , $10\mu F$ between $REFP$ and $REFN$, $C_{COM} = 0.1\mu F$ in parallel with $2.2\mu F$ to GND , $T_A = +25^\circ C$, unless otherwise noted.)

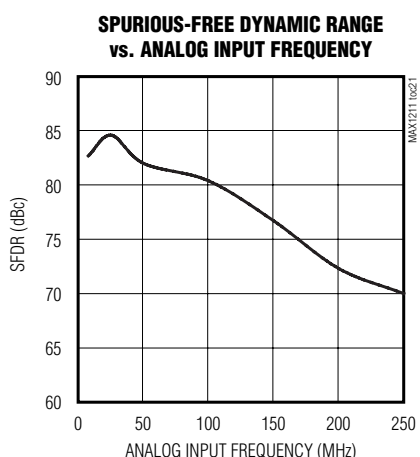
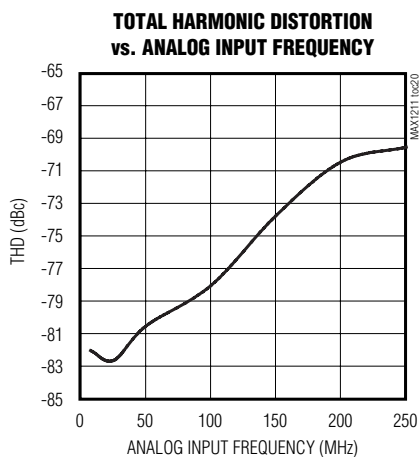
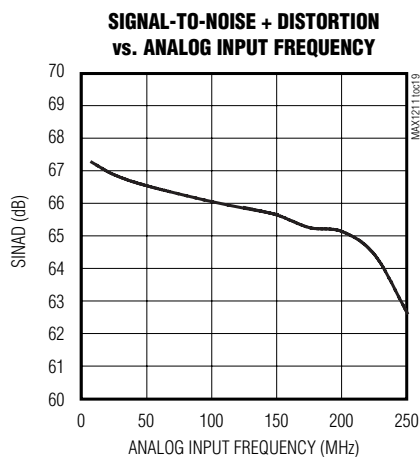
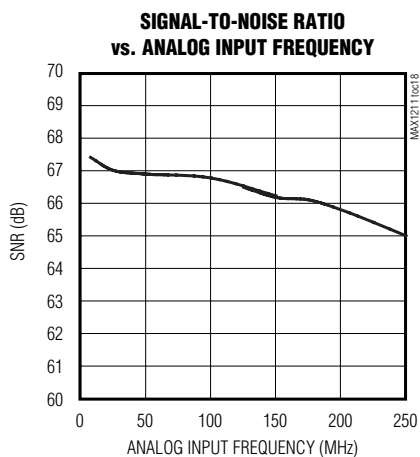


65Msps, 12-Bit, IF Sampling ADC

MAX1211

Typical Operating Characteristics (continued)

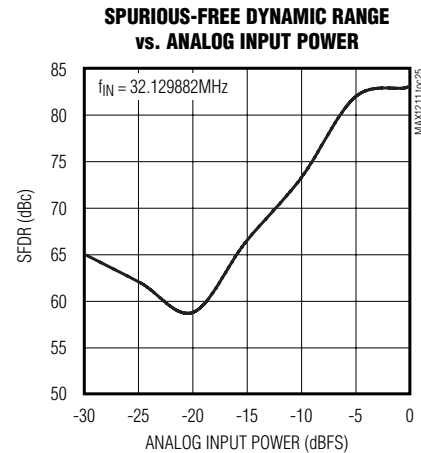
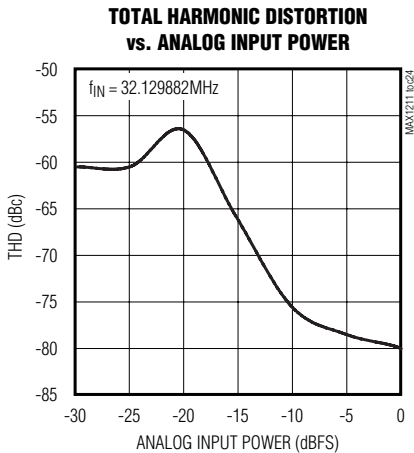
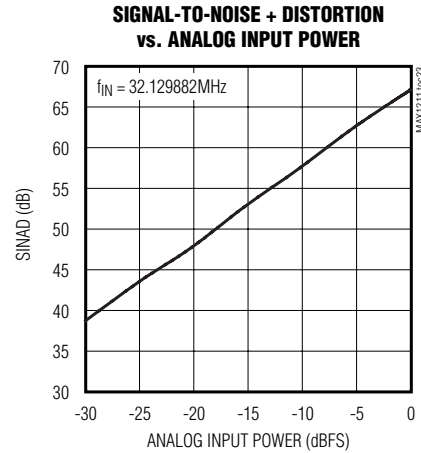
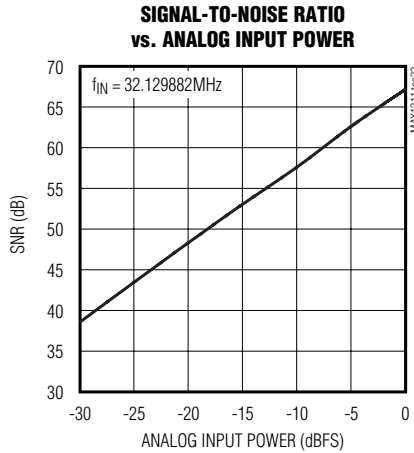
($V_{DD} = 3.3V$, $OV_{DD} = 2.0V$, $GND = 0$, $REFIN = REFOUT$ (internal reference), $C_{REFOUT} = 0.1\mu F$, $C_L \approx 8pF$ at digital outputs, differential input at $-0.2dBFS$, $CLKTYP = high$, $PD = low$, $G/T = low$, $f_{CLK} = 65.005678MHz$ (50% duty cycle), $C_{REFP} = C_{REFN} = 0.1\mu F$ in parallel with $10\mu F$ to GND , $10\mu F$ between $REFP$ and $REFN$, $C_{COM} = 0.1\mu F$ in parallel with $2.2\mu F$ to GND , $T_A = +25^\circ C$, unless otherwise noted.)



65Msps, 12-Bit, 1/2 Sampling ADC

Typical Operating Characteristics (continued)

($V_{DD} = 3.3V$, $OV_{DD} = 2.0V$, $GND = 0$, $REFIN = REFOUT$ (internal reference), $C_{REFOUT} = 0.1\mu F$, $C_L \approx 8pF$ at digital outputs, differential input at $-0.2dBFS$, $CLKTYP = high$, $PD = low$, $G/T = low$, $f_{CLK} = 65.005678MHz$ (50% duty cycle), $C_{REFP} = C_{REFN} = 0.1\mu F$ in parallel with $10\mu F$ to GND , $10\mu F$ between $REFP$ and $REFN$, $C_{COM} = 0.1\mu F$ in parallel with $2.2\mu F$ to GND , $T_A = +25^\circ C$, unless otherwise noted.)

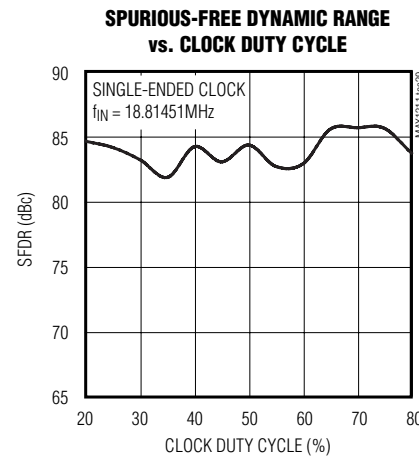
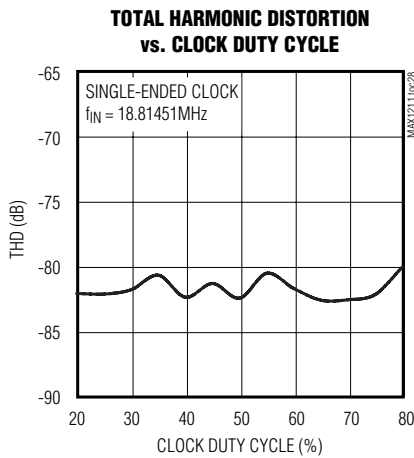
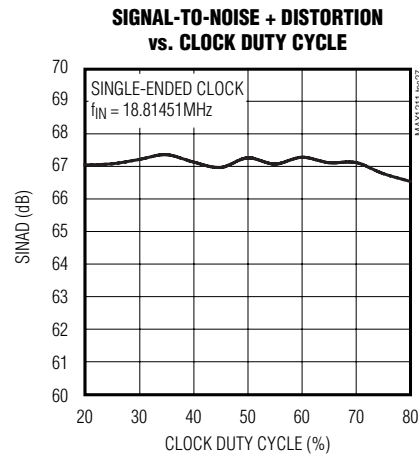
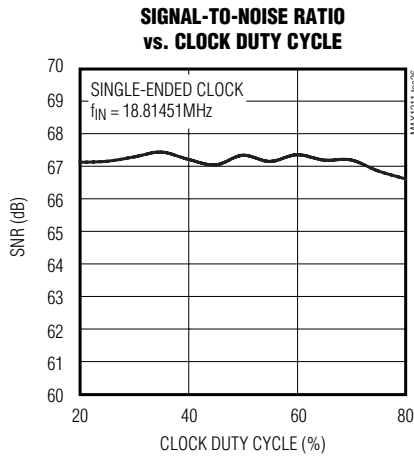


65Msps, 12-Bit, IF Sampling ADC

MAX1211

Typical Operating Characteristics (continued)

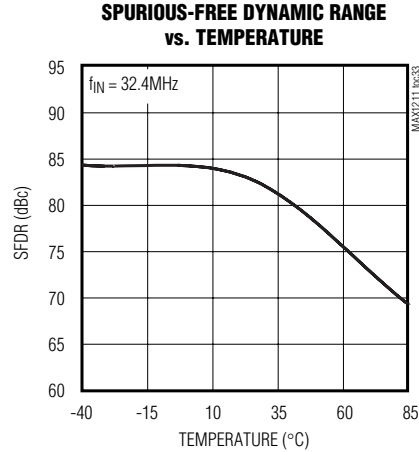
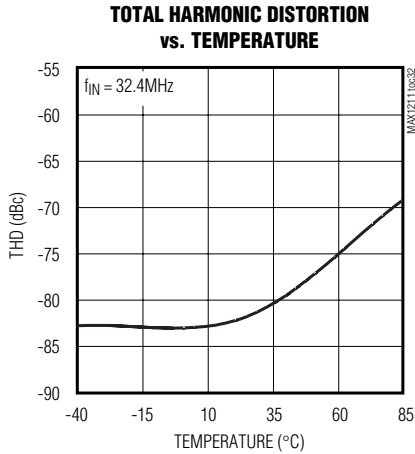
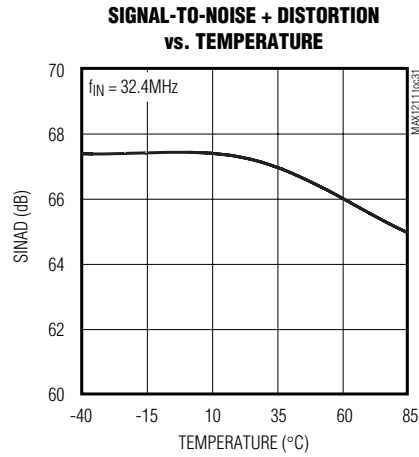
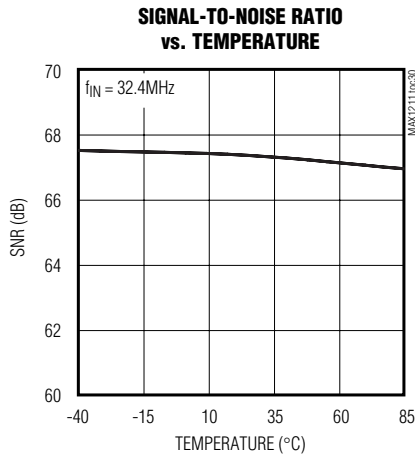
($V_{DD} = 3.3V$, $OV_{DD} = 2.0V$, $GND = 0$, $REFIN = REFOUT$ (internal reference), $C_{REFOUT} = 0.1\mu F$, $C_L \approx 8pF$ at digital outputs, differential input at $-0.2dBFS$, $CLKTYP = high$, $PD = low$, $G/\bar{T} = low$, $f_{CLK} = 65.005678MHz$ (50% duty cycle), $C_{REFP} = C_{REFN} = 0.1\mu F$ in parallel with $10\mu F$ to GND , $10\mu F$ between $REFP$ and $REFN$, $C_{COM} = 0.1\mu F$ in parallel with $2.2\mu F$ to GND , $T_A = +25^\circ C$, unless otherwise noted.)



65Msps, 12-Bit, 1F Sampling ADC

Typical Operating Characteristics (continued)

($V_{DD} = 3.3V$, $OV_{DD} = 2.0V$, $GND = 0$, $REFIN = REFOUT$ (internal reference), $C_{REFOUT} = 0.1\mu F$, $C_L \approx 8pF$ at digital outputs, differential input at $-0.2dBFS$, $CLKTYP = high$, $PD = low$, $G/T = low$, $f_{CLK} = 65.005678MHz$ (50% duty cycle), $C_{REFP} = C_{REFN} = 0.1\mu F$ in parallel with $10\mu F$ to GND , $10\mu F$ between $REFP$ and $REFN$, $C_{COM} = 0.1\mu F$ in parallel with $2.2\mu F$ to GND , $T_A = +25^\circ C$, unless otherwise noted.)

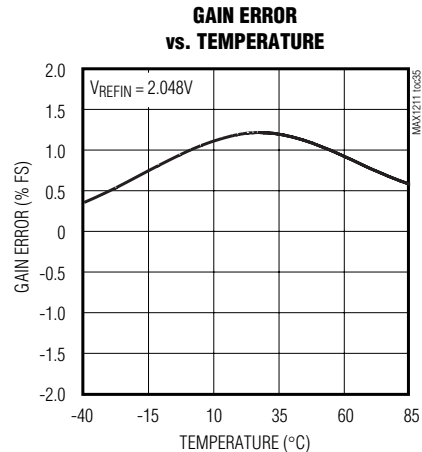
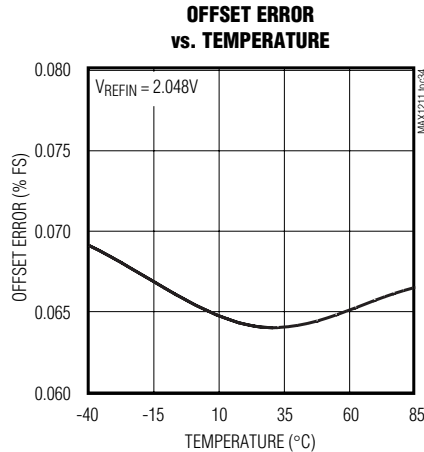


65Msps, 12-Bit, 1F Sampling ADC

MAX1211

Typical Operating Characteristics (continued)

($V_{DD} = 3.3V$, $OV_{DD} = 2.0V$, $GND = 0$, $REFIN = REFOUT$ (internal reference), $C_{REFOUT} = 0.1\mu F$, $C_L \approx 8pF$ at digital outputs, differential input at $-0.2dBFS$, $CLKTYP = high$, $PD = low$, $G/\bar{T} = low$, $f_{CLK} = 65.005678MHz$ (50% duty cycle), $C_{REFP} = C_{REFN} = 0.1\mu F$ in parallel with $10\mu F$ to GND , $10\mu F$ between $REFP$ and $REFN$, $C_{COM} = 0.1\mu F$ in parallel with $2.2\mu F$ to GND , $T_A = +25^\circ C$, unless otherwise noted.)



Pin Description

PIN	NAME	FUNCTION
1	REFP	Positive Reference I/O. Conversion range is $\pm(V_{REFP} - V_{REFN})$. Bypass REFP to GND with a $\geq 2.2\mu F$ capacitor in parallel with a $0.1\mu F$ capacitor. Connect a $10\mu F$ bypass capacitor between REFP and REFN.
2	REFN	Negative Reference I/O. Conversion range is $\pm(V_{REFP} - V_{REFN})$. Bypass REFN to GND with a $\geq 2.2\mu F$ capacitor in parallel with a $0.1\mu F$ capacitor. Connect a $10\mu F$ bypass capacitor between REFP and REFN.
3	COM	Common-Mode Voltage I/O. Bypass COM to GND with a $\geq 2.2\mu F$ capacitor in parallel with a $0.1\mu F$ capacitor.
4, 7, 16, 35	GND	Ground. Connect all ground pins and the EP together.
5	INP	Positive Analog Input. For single-ended input operation, connect signal source to INP and connect INN to COM. For differential operation, connect the input signal between INP and INN.
6	INN	Negative Analog Input. For single-ended input operation, connect INN to COM. For differential operation, connect the input signal between INP and INN.
8, 12–15, 36	V_{DD}	Analog Power Input. Connect V_{DD} to a 3.0V to 3.6V power supply. Bypass V_{DD} to GND with a parallel capacitor combination of $\geq 2.2\mu F$ and $0.1\mu F$. Connect all V_{DD} pins to the same potential.
9	CLKN	Negative Clock Input. In differential clock input mode ($CLKTYP = OV_{DD}$ or V_{DD}), connect the clock signal between CLKP and CLKN. In single-ended clock mode ($CLKTYP = GND$), apply the clock signal to CLKP and tie CLKN to GND.
10	CLKP	Positive Clock Input. In differential clock input mode ($CLKTYP = OV_{DD}$ or V_{DD}), connect the differential clock signal between CLKP and CLKN. In single-ended clock mode ($CLKTYP = GND$), apply the single-ended clock signal to CLKP and connect CLKN to GND.

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Pin Description (continued)

PIN	NAME	FUNCTION
11	CLKTYP	Clock Type Definition Input. Connect CLKTYP to GND to define the single-ended clock input. Connect CLKTYP to OV _{DD} or V _{DD} to define the differential clock input.
17, 34	OV _{DD}	Output Driver Power Input. Connect OV _{DD} to a 1.7V to V _{DD} power supply. Bypass OV _{DD} to GND with a parallel capacitor combination of $\geq 2.2\mu\text{F}$ and $0.1\mu\text{F}$.
18	DOR	Data Out-of-Range Indicator. The DOR digital output indicates when the analog input voltage is out of range. When DOR is high, the analog input is beyond its full-scale range. When DOR is low, the analog input is within its full-scale range.
19	D11	CMOS Digital Output, Bit 11 (MSB)
20	D10	CMOS Digital Output, Bit 10
21	D9	CMOS Digital Output, Bit 9
22	D8	CMOS Digital Output, Bit 8
23	D7	CMOS Digital Output, Bit 7
24	D6	CMOS Digital Output, Bit 6
25	D5	CMOS Digital Output, Bit 5
26	D4	CMOS Digital Output, Bit 4
27	D3	CMOS Digital Output, Bit 3
28	D2	CMOS Digital Output, Bit 2
29	D1	CMOS Digital Output, Bit 1
30	D0	CMOS Digital Output, Bit 0 (LSB)
31, 32	N.C.	No Connect. Leave N.C. unconnected.
33	DAV	Data Valid Output. The DAV is a single-ended version of the input clock that is compensated to correct for any input clock duty-cycle variations. DAV is typically used to latch the MAX1211 output data into an external back-end digital circuit.
37	PD	Power-Down Input. Force PD high for power-down mode. Force PD low for normal operation.
38	REFOUT	Internal Reference Voltage Output. For internal reference operation, connect REFOUT directly to REFIN or use a resistive divider from REFOUT to set the voltage at REFIN. Bypass REFOUT to GND with a $\geq 0.1\mu\text{F}$ capacitor.
39	REFIN	Reference Input. $V_{\text{REFIN}} = 2 \times (V_{\text{REFP}} - V_{\text{REFN}})$. Bypass REFIN to GND with a $\geq 0.1\mu\text{F}$ capacitor.
40	G/ \bar{T}	Output Format Select Input. Connect G/ \bar{T} to GND for the two's complement digital output format. Connect G/ \bar{T} to OV _{DD} or V _{DD} for the Gray code digital output format.
—	EP	Exposed Paddle. EP is internally connected to GND. Externally connect EP to GND to achieve specified performance.

65Msps, 12-Bit, 1F Sampling ADC

MAX1211

Detailed Description

The MAX1211 uses a 10-stage, fully differential, pipelined architecture (Figure 1) that allows for high-speed conversion while minimizing power consumption. Samples taken at the inputs move progressively through the pipeline stages every half-clock cycle. From input to output, the total clock-cycle latency is 8.5 clock cycles.

Each pipeline converter stage converts its input voltage into a digital output code. At every stage, except the last, the error between the input voltage and the digital output code is multiplied and passed along to the next pipeline stage. Digital error correction compensates for ADC comparator offsets in each pipeline stage and ensures no missing codes. Figure 2 shows the MAX1211 functional diagram.

Input Track-and-Hold (T/H) Circuit

Figure 3 displays a simplified functional diagram of the input T/H circuits. In track mode, switches S1, S2a, S2b, S4a, S4b, S5a, and S5b are closed. The fully differential circuits sample the input signals onto the two capacitors (C2a and C2b) through switches S4a and S4b. S2a and S2b set the common mode for the operational transconductance amplifier (OTA), and open simultaneously with S1, sampling the input waveform. Switches S4a, S4b, S5a, and S5b are then opened before switches S3a and S3b connect capacitors C1a and C1b to the output of the amplifier and switch S4c is closed. The resulting differential voltages are held on capacitors C2a and C2b. The amplifiers charge capacitors C1a and C1b to the same values originally held on C2a and C2b. These values are then presented to the first-stage quantizers and isolate the pipelines from the fast-changing inputs. The wide input-bandwidth T/H amplifier allows the MAX1211 to track and sample/hold analog inputs of high frequencies well beyond Nyquist. Analog input INP to INN can be driven either differentially or single ended. For differential inputs, balance the input impedance of INP and INN and set the common-mode voltage to midsupply ($V_{DD}/2$) for optimum performance.

Reference Output (REFOUT)

An internal bandgap reference is the basis for all the internal voltages and bias currents used in the MAX1211. The power-down logic input (PD) enables and disables the reference circuit. REFOUT has approximately $17k\Omega$ to GND when the MAX1211 is in power-down. The reference circuit requires 10ms to power up and settle when power is applied to the MAX1211 or when PD transitions from high to low.

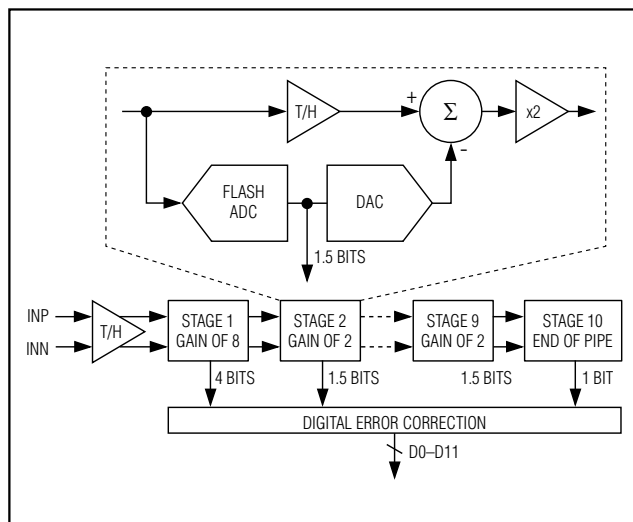


Figure 1. Pipeline Architecture—Stage Blocks

The internal bandgap reference and buffer generate REFOUT to be 2.048V with a $+100\text{ppm}/^\circ\text{C}$ temperature coefficient. Connect an external $\geq 0.1\mu\text{F}$ bypass capacitor from REFOUT to GND for stability. REFOUT sources up to 1.4mA and sinks up to $100\mu\text{A}$ for external circuits with a load regulation of $35\text{mV}/\text{mA}$. Short-circuit protection limits IREFOUT to a 2.1mA source current when shorted to GND and a $240\mu\text{A}$ sink current when shorted to V_{DD} .

Analog Inputs and Reference Configurations

The MAX1211 full-scale analog input range is $\pm V_{REF}$ with a common-mode input range of $V_{DD} / 2 \pm 0.5V$. V_{REF} is the difference between V_{REFP} and V_{REFN} . The MAX1211 provides three modes of reference operation. The voltage at REFIN (V_{REFIN}) sets the reference operation mode (Table 1).

Connect REFOUT to REFIN either with a direct short or through a resistive divider to enter internal reference mode. COM, REFP, and REFN are low-impedance outputs with $V_{COM} = V_{DD} / 2$, $V_{REFP} = V_{DD} / 2 + V_{REFIN} / 4$, and $V_{REFN} = V_{DD} / 2 - V_{REFIN} / 4$. Bypass REFP, REFN, and COM each with a $0.1\mu\text{F}$ capacitor in parallel with a $\geq 2.2\mu\text{F}$ capacitor to GND. Bypass REFP to REFN with a $10\mu\text{F}$ capacitor. Bypass REFIN and REFOUT to GND with a $0.1\mu\text{F}$ capacitor. The REFIN input impedance is very large ($>50M\Omega$). When driving REFIN through a resistive divider, use resistances $\geq 10k\Omega$ to avoid loading REFOUT.

Buffered external reference mode is virtually identical to internal reference mode except that the reference source is derived from an external reference and not

65Msps, 12-Bit, 1F Sampling ADC

drive CLKP and CLKN with the external differential clock signal. Consider the clock input as an analog input and route it away from any other analog inputs and digital signal lines.

CLKP and CLKN are high impedance when the MAX1211 is powered down (Figure 4).

Low clock jitter is required for the specified SNR performance of the MAX1211. Analog input sampling occurs on the falling edge of the clock signal, requiring this edge to have the lowest possible jitter. Jitter limits the maximum SNR performance of any ADC according to the following relationship:

$$SNR = 20 \times \log \left(\frac{1}{2 \times \pi \times f_{IN} \times t_J} \right)$$

where f_{IN} represents the analog input frequency and t_J is the total system clock jitter. Clock jitter is especially critical for undersampling applications. For example, assuming that clock jitter is the only noise source, to obtain the specified 65.1dB of SNR with an input frequency of 250MHz, the system must have less than 0.35ps of clock jitter. In actuality, there are other noise sources such as thermal noise and quantization noise that contribute to the system noise requiring the clock jitter to be less than 0.22ps to obtain the specified 65.1dB of SNR at 250MHz.

System Timing Requirements

Figure 5 shows the relationship between the clock, analog inputs, DAV indicator, DOR indicator, and the resulting output data. The analog input is sampled on the falling edge of the clock signal and the resulting data appears at the digital outputs 8.5 clock cycles later.

The DAV indicator is synchronized with the digital output and optimized for use in latching data into digital back-end circuitry. Alternatively, digital back-end circuitry may be latched with the falling edge of the clock.

Data Valid Output (DAV)

DAV is a single-ended version of the input clock that is compensated to correct for any input clock duty-cycle variations. The output data changes on the falling edge of DAV, and DAV rises once the output data is valid. The falling edge of DAV is synchronized to have a 6.4ns delay from the falling edge of the input clock. Output data at D0–D11 and DOR are valid from 8.4ns before the rising edge of DAV to 6.6ns after the rising edge of DAV.

DAV is high impedance when the MAX1211 is in power-down (PD = high). DAV is capable of sinking and sourcing 600µA and has three times the drive strength of

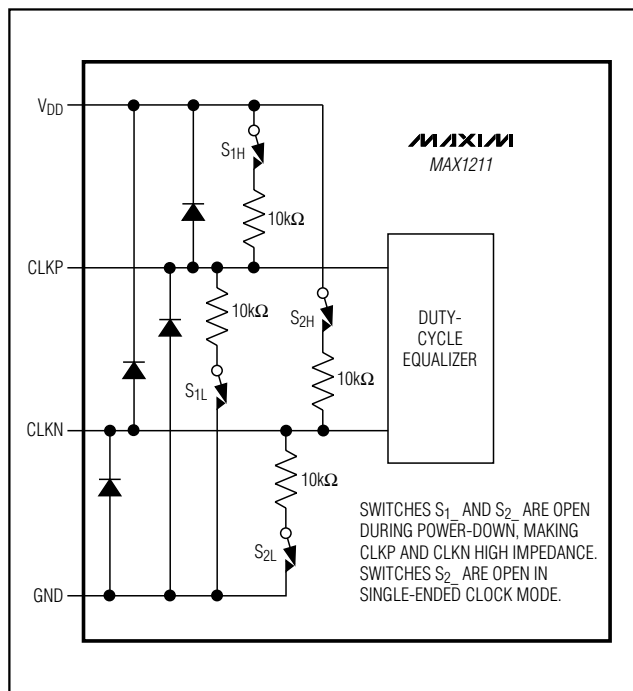


Figure 4. Simplified Clock Input Circuit

D0–D11 and DOR. It is typically used to latch the MAX1211 output data into an external back-end digital circuit.

Keep the capacitive load on DAV as low as possible (<25pF) to avoid large digital currents feeding back into the analog portion of the MAX1211 and degrading its dynamic performance. An external buffer on DAV isolates it from heavy capacitive loads. Refer to the MAX1211 EV kit schematic for an example of DAV driving back-end digital circuitry through an external buffer.

Data Out-of-Range Indicator (DOR)

The DOR digital output indicates when the analog input voltage is out of range. When DOR is high, the analog input is out of range. When DOR is low, the analog input is within range. The valid differential input range is from (VREFP - VREFN) to (VREFN - VREFP). Signals outside this valid differential range cause DOR to assert high as shown in Table 2.

DOR is synchronized with DAV and transitions along with output data D0–D11. There is an 8.5 clock-cycle latency in the DOR function just as with the output data (Figure 5).

DOR is high impedance when the MAX1211 is in power-down (PD = high). DOR enters a high-imped-

65Msps, 12-Bit, IF Sampling ADC

Table 2. Output Codes vs. Input Voltage

GRAY CODE OUTPUT CODE (G \bar{T} = 1)				TWO'S COMPLEMENT OUTPUT CODE (G \bar{T} = 0)				V _{INP} - V _{INN} (V _{REFP} = 2.162V) (V _{REFN} = 1.138V)
BINARY D11 → D0	DOR	HEXADECIMAL EQUIVALENT OF D11 → D0	DECIMAL EQUIVALENT OF D11 → D0 (CODE ₁₀)	BINARY D11 → D0	DOR	HEXADECIMAL EQUIVALENT OF D11 → D0	DECIMAL EQUIVALENT OF D11 → D0 (CODE ₁₀)	
1000 0000 0000	1	0x800	+4095	0111 1111 1111	1	0x7FF	+2047	>+1.0235V (DATA OUT OF RANGE)
1000 0000 0000	0	0x800	+4095	0111 1111 1111	0	0x7FF	+2047	+1.0235V
1000 0000 0001	0	0x801	+4094	0111 1111 1110	0	0x7FE	+2046	+1.0230V
1100 0000 0011	0	0xC03	+2050	0000 0000 0010	0	0x002	+2	+0.0010V
1100 0000 0001	0	0xC01	+2049	0000 0000 0001	0	0x001	+1	+0.0005V
1100 0000 0000	0	0xC00	+2048	0000 0000 0000	0	0x000	0	+0.0000V
0100 0000 0000	0	0x400	+2047	1111 1111 1111	0	0xFFF	-1	-0.0005V
0100 0000 0001	0	0x401	+2046	1111 1111 1110	0	0xFFE	-2	-0.0010V
0000 0000 0001	0	0x001	+1	1000 0000 0001	0	0x801	-2047	-1.0235V
0000 0000 0000	0	0x000	0	1000 0000 0000	0	0x800	-2048	-1.0240V
0000 0000 0000	1	0x000	0	1000 0000 0000	1	0x800	-2048	<-1.0240V (DATA OUT OF RANGE)

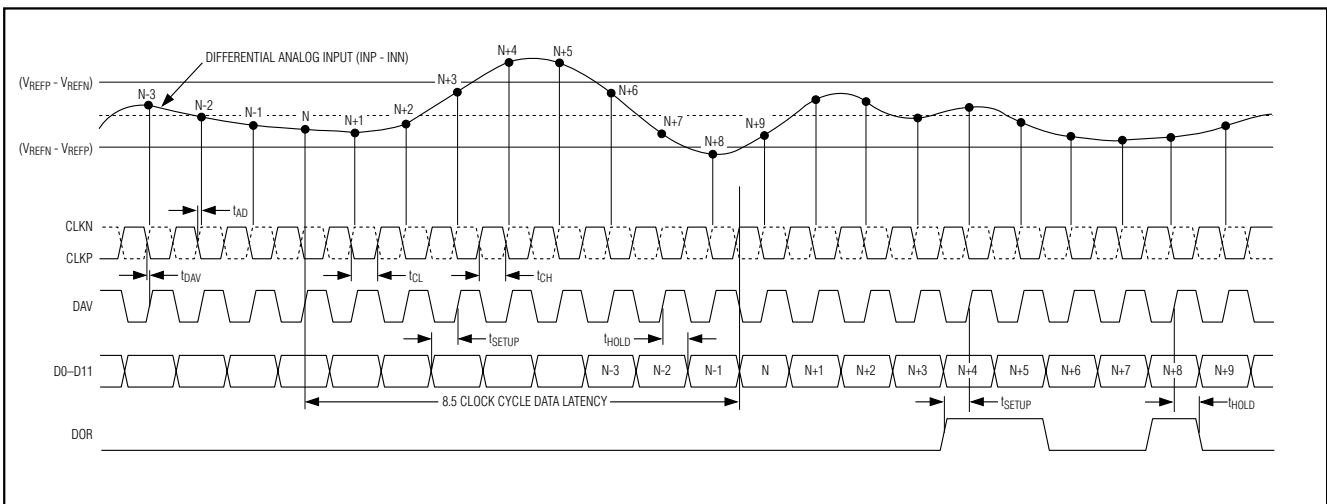


Figure 5. System Timing Diagram

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MAX1211

ance state within 10ns of the rising edge of PD and becomes active within 10ns of PD's falling edge.

Digital Output Data (D0–D11), Output Format (G/T)

The MAX1211 provides a 12-bit, parallel, tri-state output bus. D0–D11 and DOR update on the falling edge of DAV and are valid on the rising edge of DAV.

The MAX1211 output data format is either Gray code or two's complement, depending on the logic input G/T. With G/T high, the output data format is Gray code. With G/T low, the output data format is two's complement. See Figure 8 for a binary-to-Gray and Gray-to-binary code-conversion example.

The following equations, Table 2, Figure 6, and Figure 8 define the relationship between the digital output and the analog input:

$$V_{INP} - V_{INN} = (V_{REFP} - V_{REFN}) \times 2 \times \frac{CODE_{10} - 2048}{4096}$$

for Gray code (G/T = 1).

$$V_{INP} - V_{INN} = (V_{REFP} - V_{REFN}) \times 2 \times \frac{CODE_{10}}{4096}$$

for two's complement (G/T = 0).

where CODE₁₀ is the decimal equivalent of the digital output code as shown in Table 2.

The digital outputs D0–D11 are high impedance when the MAX1211 is in power-down (PD = high). D0–D11 go high impedance within 10ns of the rising edge of PD and become active within 10ns of PD's falling edge.

Keep the capacitive load on the MAX1211 digital outputs D0–D11 as low as possible (<15pF) to avoid large digital currents feeding back into the analog portion of the MAX1211 and degrading its dynamic performance. The addition of external digital buffers on the digital outputs isolate the MAX1211 from heavy capacitive loads. To improve the dynamic performance of the MAX1211, add 220Ω resistors in series with the digital outputs close to the MAX1211. Refer to the MAX1211 EV kit schematic for an example of the digital outputs driving a digital buffer through 220Ω series resistors.

Power-Down Input (PD)

The MAX1211 has two power modes that are controlled with power-down digital input (PD). With PD low, the MAX1211 is in its normal operating mode. With PD high, the MAX1211 is in power-down mode.

The power-down mode allows the MAX1211 to efficiently use power by transitioning to a low-power state when conversions are not required. Additionally, the MAX1211 parallel output bus goes high impedance in

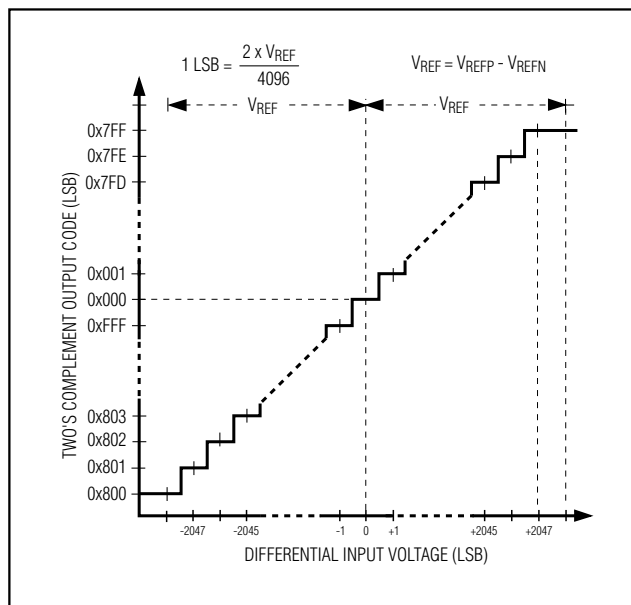


Figure 6. Two's Complement Transfer Function (G/T = 0)

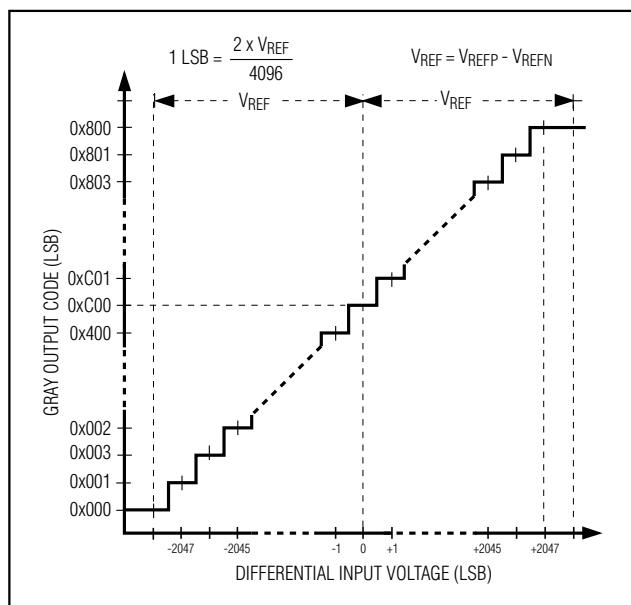


Figure 7. Gray Code Transfer Function (G/T = 1)

power-down mode, allowing other devices on the bus to be accessed.

In power-down mode, all internal circuits are off, the analog supply current reduces to 4mA, and the digital supply current reduces to 19μA. The following list

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BINARY-TO-GRAY CODE CONVERSION

1) THE MOST SIGNIFICANT GRAY CODE BIT IS THE SAME AS THE MOST SIGNIFICANT BINARY BIT.

D11 → D7 → D3 → D0	BIT POSITION
0 1 1 1 0 1 0 0 1 1 0 0	BINARY
↓	
0	GRAY CODE

2) SUBSEQUENT GRAY CODE BITS ARE FOUND ACCORDING TO THE FOLLOWING EQUATION:

$$\text{GRAY}_X = \text{BINARY}_X \oplus \text{BINARY}_{X+1}$$

WHERE \oplus IS THE EXCLUSIVE OR FUNCTION (SEE TRUTH TABLE BELOW) AND X IS THE BIT POSITION.

$$\text{GRAY}_{10} = \text{BINARY}_{10} \oplus \text{BINARY}_{11}$$

$$\text{GRAY}_{10} = 1 \oplus 0$$

$$\text{GRAY}_{10} = 1$$

D11 → D7 → D3 → D0	BIT POSITION
0 \oplus 1 1 1 0 1 0 0 1 1 0 0	BINARY
↓	
0 1	GRAY CODE

3) REPEAT STEP 2 UNTIL COMPLETE

$$\text{GRAY}_9 = \text{BINARY}_9 \oplus \text{BINARY}_{10}$$

$$\text{GRAY}_9 = 1 \oplus 1$$

$$\text{GRAY}_9 = 0$$

D11 → D7 → D3 → D0	BIT POSITION
0 1 \oplus 1 1 0 1 0 0 1 1 0 0	BINARY
↓	
0 1 0	GRAY CODE

4) THE FINAL GRAY CODE CONVERSION IS:

D11 → D7 → D3 → D0	BIT POSITION
0 1 1 1 0 1 0 0 1 1 0 0	BINARY
0 1 0 0 1 1 1 0 1 0 1 0	GRAY CODE

GRAY-TO-BINARY CODE CONVERSION

1) THE MOST SIGNIFICANT BINARY BIT IS THE SAME AS THE MOST SIGNIFICANT GRAY CODE BIT.

D11 → D7 → D3 → D0	BIT POSITION
0 1 0 0 1 1 1 0 1 0 1 0	GRAY CODE
↓	
0	BINARY

2) SUBSEQUENT BINARY BITS ARE FOUND ACCORDING TO THE FOLLOWING EQUATION:

$$\text{BINARY}_X = \text{BINARY}_{X+1} \oplus \text{GRAY}_X$$

WHERE \oplus IS THE EXCLUSIVE OR FUNCTION (SEE TRUTH TABLE BELOW) AND X IS THE BIT POSITION.

$$\text{BINARY}_{10} = \text{BINARY}_{11} \oplus \text{GRAY}_{10}$$

$$\text{BINARY}_{10} = 0 \oplus 1$$

$$\text{BINARY}_{10} = 1$$

D11 → D7 → D3 → D0	BIT POSITION
0 \oplus 0 0 1 1 1 0 1 0 1 0	GRAY CODE
↓	
0 1	BINARY

3) REPEAT STEP 2 UNTIL COMPLETE

$$\text{BINARY}_9 = \text{BINARY}_{10} \oplus \text{GRAY}_9$$

$$\text{BINARY}_9 = 1 \oplus 0$$

$$\text{BINARY}_9 = 1$$

D11 → D7 → D3 → D0	BIT POSITION
0 1 \oplus 0 0 1 1 1 0 1 0 1 0	GRAY CODE
↓	
0 1 1	BINARY

4) THE FINAL BINARY CONVERSION IS:

D11 → D7 → D3 → D0	BIT POSITION
0 1 0 0 1 1 1 0 1 0 1 0	GRAY CODE
0 1 1 1 0 1 0 0 1 1 0 0	BINARY

EXCLUSIVE OR TRUTH TABLE

A	B	Y = A \oplus B
0	0	0
0	1	1
1	0	1
1	1	0

Figure 8. Binary-to-Gray and Gray-to-Binary Code Conversion

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shows the state of the analog inputs and digital outputs in power-down mode:

- INP, INN analog inputs are disconnected from the internal input amplifier (Figure 3).
- REFOUT has approximately 17kΩ to GND.
- REFP, COM, REFN go high impedance with respect to V_{DD} and GND, but there is an internal 4kΩ resistor between REFP and COM, as well as an internal 4kΩ resistor between REFN and COM.
- D0–D11, DOR, and DAV go high impedance.
- CLKP, CLKN clock inputs go high impedance (Figure 4).

The wake-up time from power-down mode is dominated by the time required to charge the capacitors at REFP, REFN, and COM. In internal reference mode and buffered external reference mode, the wake-up time is typically 10ms. When operating in the unbuffered external reference mode, the wake-up time is dependent on the external reference drivers.

Applications Information

Using Transformer Coupling

In general, the MAX1211 provides better SFDR and THD with fully differential input signals than single-ended input drive, especially for input frequencies above 125MHz. In differential input mode, even-order harmonics are lower as both inputs are balanced, and each of the ADC inputs only requires half the signal swing compared to single-ended input mode.

An RF transformer (Figure 9) provides an excellent solution to convert a single-ended input source signal to a fully differential signal, required by the MAX1211 for optimum performance. Connecting the center tap of the transformer to COM provides a V_{DD} / 2 DC level shift to the input. Although a 1:1 transformer is shown, a step-up transformer can be selected to reduce the drive requirements. A reduced signal swing from the input driver, such as an op amp, can also improve the overall distortion. The configuration of Figure 9 is good for input frequencies up to Nyquist ($f_{CLK} / 2$).

The circuit of Figure 10 converts a single-ended input signal to fully differential just as in Figure 9. However, Figure 10 utilizes an additional transformer to improve the common-mode rejection, allowing high-frequency signals beyond the Nyquist frequency. The two sets of 49.9Ω termination resistors provide an equivalent 50Ω termination to the signal source. The second set of termination resistors connects to COM, providing the correct input common-mode voltage. A pair of 0.1μF and 4.7μF decoupling capacitors on COM allows a fully

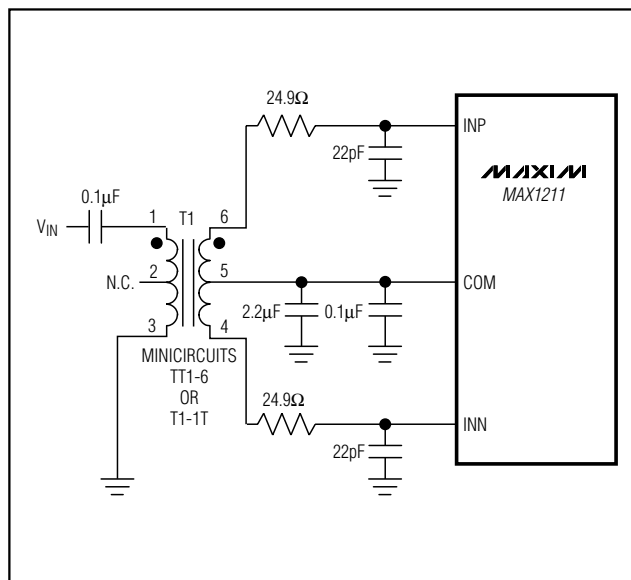


Figure 9. Transformer-Coupled Input Drive for Input Frequencies Up to Nyquist

symmetric PC board layout. Two 0Ω resistors in series with the analog inputs allow high IF input frequencies. These 0Ω resistors may be replaced with low-value resistors to limit the input bandwidth.

Single-Ended AC-Coupled Input Signal

Figure 11 shows an AC-coupled, single-ended input application. The MAX4108 provides high speed, high bandwidth, low noise, and low distortion to maintain the input signal integrity.

Buffered External Reference Drives Multiple ADCs

The buffered external reference mode allows for more control over the MAX1211 reference voltage and allows multiple converters to use a common reference. The REFIN input impedance is >50MΩ.

Figure 12 shows the MAX6062 precision bandgap reference used as a common reference for multiple converters. The 2.048V output of the MAX6062 passes through a one-pole 10Hz lowpass filter to the MAX4250. The MAX4250 buffers the 2.048V reference before its output is applied to the REFIN input of the MAX1211. The MAX4250 provides a low offset voltage (for high gain accuracy) and a low noise level.

Unbuffered External Reference Drives Multiple ADCs

The unbuffered external reference mode allows for precise control over the MAX1211 reference and allows

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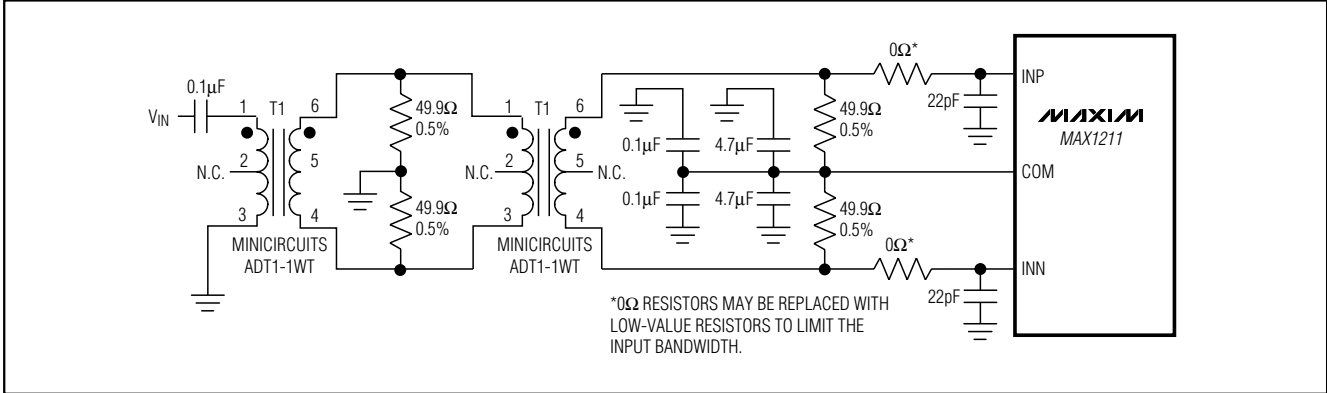


Figure 10. Transformer-Coupled Input Drive for Input Frequencies Beyond Nyquist

multiple converters to use a common reference. Connecting REFIN to GND disables the internal reference, allowing REFP, REFN, and COM to be driven directly by a set of external reference sources.

Figure 13 shows the MAX6066 precision bandgap reference used as a common reference for multiple converters. The 2.500V output of the MAX6066 is followed by a 10Hz lowpass filter and precision voltage-divider. The MAX4254 buffers the taps of this divider to provide the +2.000V, +1.500V, and +1.000V sources to drive REFP, REFN, and COM. The MAX4254 provides a low offset voltage and low noise level. The individual voltage followers are connected to 10Hz lowpass filters, which filter both the reference voltage and amplifier noise to a level of 3nV/√Hz. The 2.000V and 1.000V reference voltages set the differential full-scale range of the associated ADCs at ±1.000V.

The common power supply for all active components removes any concern regarding power-supply sequencing when powering up or down.

With the outputs of the MAX4252 matching better than 0.1%, the buffers and subsequent lowpass support as many as 8 ADCs.

Grounding, Bypassing, and Board Layout

The MAX1211 requires high-speed board layout design techniques. Refer to the MAX1211 EV kit data sheet for a board layout reference. Locate all bypass capacitors as close to the device as possible, preferably on the same side as the ADC, using surface-mount devices for minimum inductance. Bypass V_{DD} to GND with a 0.1μF ceramic capacitor in parallel with a 2.2μF ceramic capacitor. Bypass OV_{DD} to GND with a 0.1μF ceramic capacitor in parallel with a 2.2μF ceramic capacitor.

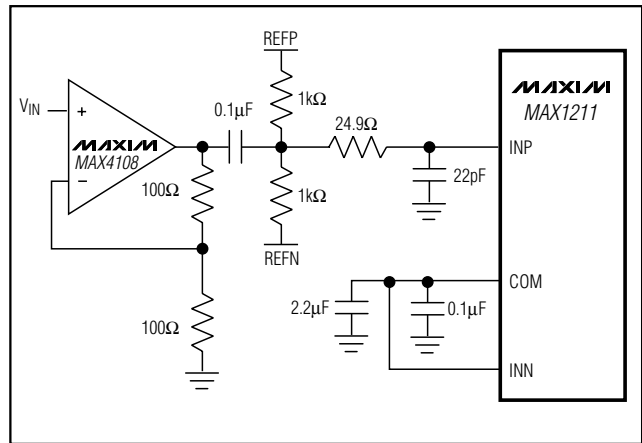


Figure 11. Single-Ended, AC-Coupled Input Drive

Multilayer boards with ample ground and power planes produce the highest level of signal integrity. All MAX1211 GNDs and the exposed backside paddle must be connected to the same ground plane. The MAX1211 relies on the exposed backside paddle connection for a low-inductance ground connection. Isolate the ground plane from any noisy digital system ground planes such as a DSP or output buffer ground.

Route high-speed digital signal traces away from the sensitive analog traces. Keep all signal lines short and free of 90° turns.

Ensure that the differential analog input network layout is symmetric and that all parasitics are balanced equally. Refer to the MAX1211 EV kit data sheet for an example of symmetric input layout.

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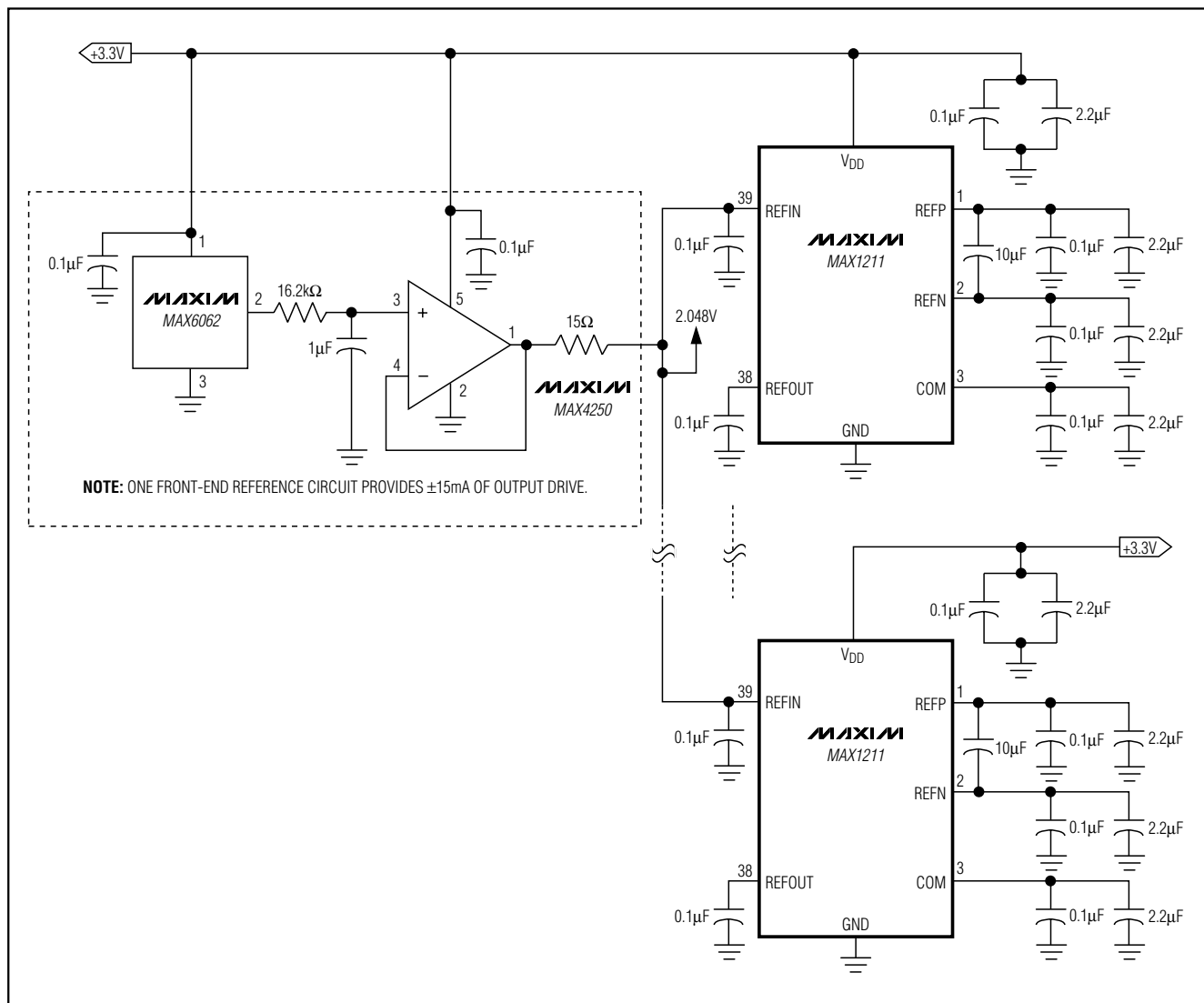


Figure 12. External Buffered (MAX4250) Reference Drive Using a MAX6062 Bandgap Reference

Parameter Definitions

Integral Nonlinearity (INL)

Integral nonlinearity is the deviation of the values on an actual transfer function from a straight line. This straight line is either a best-straight-line fit or a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. The static linearity parameters for the MAX1211 are measured using the end-point method.

Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between an actual step width and the ideal value of 1 LSB. A DNL error specification of less than 1 LSB guarantees no missing codes and a monotonic transfer function.

Offset Error

Ideally, the midscale MAX1211 transition occurs at 0.5 LSB above midscale. The offset error is the amount of deviation between the measured transition point and the ideal transition point.

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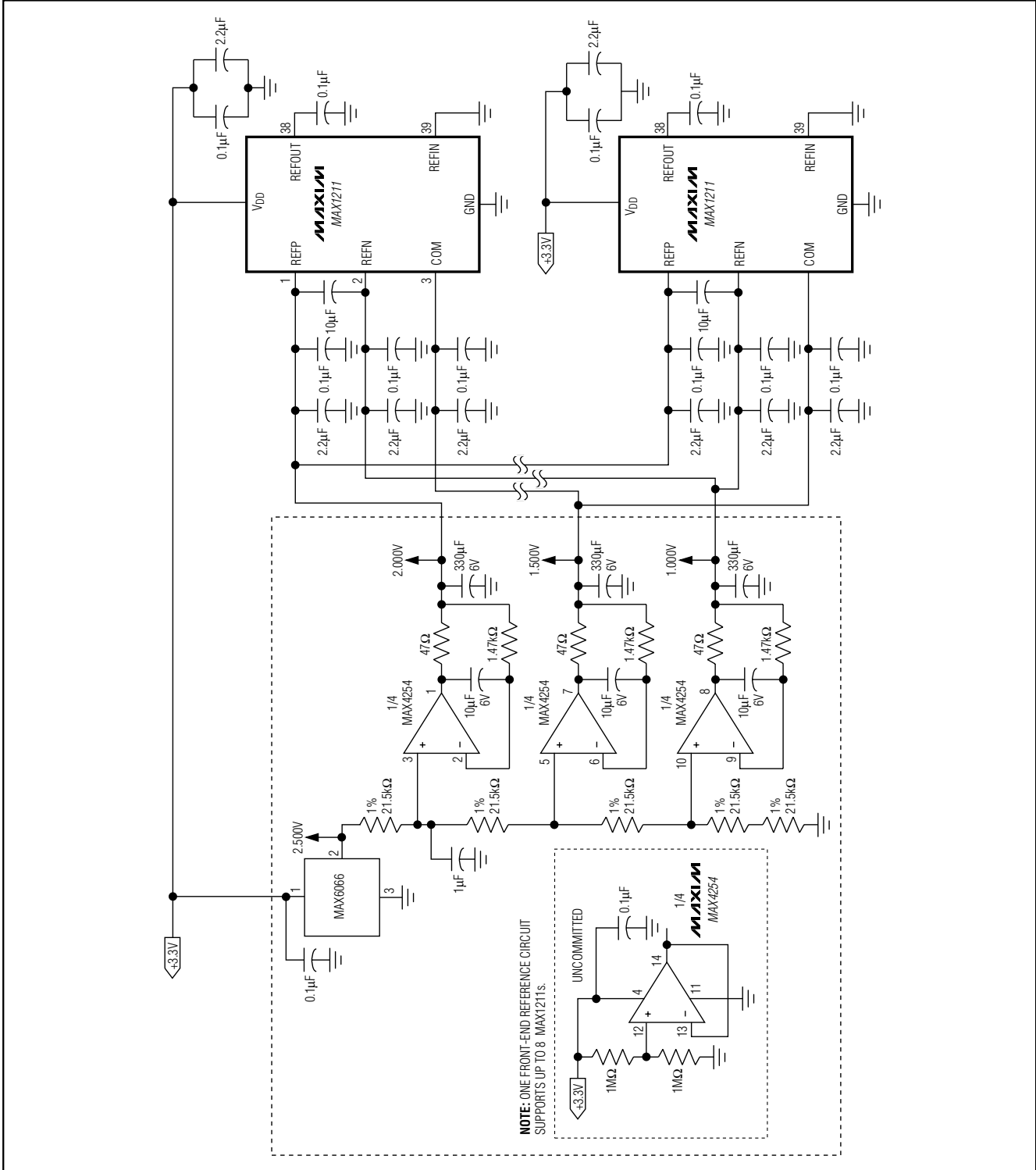


Figure 13. External Unbuffered Reference Driving 8 ADCs with MAX4254 and MAX6066

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Gain Error

Ideally, the positive full-scale MAX1211 transition occurs at 1.5 LSB below positive full scale, and the negative full-scale transition occurs at 0.5 LSB above negative full scale. The gain error is the difference of the measured transition points minus the difference of the ideal transition points.

Aperture Jitter

Figure 14 depicts the aperture jitter (t_{AJ}), which is the sample-to-sample variation in the aperture delay.

Aperture Delay

Aperture delay (t_{AD}) is the time defined between the rising edge of the sampling clock and the instant when an actual sample is taken (Figure 14).

Overdrive Recovery Time

Overdrive recovery time is the time required for the ADC to recover from an input transient that exceeds the full-scale limits. The MAX1211 specifies overdrive recovery time using an input transient that exceeds the full-scale limits by $\pm 10\%$.

Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$\text{SNR}_{\text{dB}[\text{max}]} = 6.02_{\text{dB}} \times N + 1.76_{\text{dB}}$$

In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc. SNR is computed by taking the ratio of the RMS signal to the RMS noise. RMS noise includes all spectral components to the Nyquist frequency excluding the fundamental, the first six harmonics (HD2–HD7), and the DC offset.

Signal-to-Noise Plus Distortion (SINAD)

SINAD is computed by taking the ratio of the RMS signal to the RMS noise plus distortion. RMS noise plus distortion includes all spectral components to the Nyquist frequency, excluding the fundamental and the DC offset.

Effective Number of Bits (ENOB)

ENOB specifies the dynamic performance of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. ENOB for a full-scale sinusoidal input waveform is computed from:

$$\text{ENOB} = \left(\frac{\text{SINAD} - 1.76}{6.02} \right)$$

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first six harmonics of the input signal to the fundamental itself. This is expressed as:

$$\text{THD} = 20 \times \log \left(\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2 + V_7^2}}{V_1} \right)$$

where V_1 is the fundamental amplitude, and V_2 through V_7 are the amplitudes of the 2nd- through 7th-order harmonics (HD2–HD7).

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio expressed in decibels of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next-largest spurious component, excluding DC offset.

Intermodulation Distortion (IMD)

IMD is the total power of the IM2 to IM5 intermodulation products to the Nyquist frequency relative to the total input power of the two input tones f_1 and f_2 . The individual input tone levels are at $-dBFS$. The intermodulation products are as follows:

- 2nd-order intermodulation products (IM2): $f_1 + f_2$, $f_2 - f_1$
- 3rd-order intermodulation products (IM3): $2 \times f_1 - f_2$, $2 \times f_2 - f_1$, $2 \times f_1 + f_2$, $2 \times f_2 + f_1$
- 4th-order intermodulation products (IM4): $3 \times f_1 - f_2$, $3 \times f_2 - f_1$, $3 \times f_1 + f_2$, $3 \times f_2 + f_1$
- 5th-order intermodulation products (IM5): $3 \times f_1 - 2 \times f_2$, $3 \times f_2 - 2 \times f_1$, $3 \times f_1 + 2 \times f_2$, $3 \times f_2 + 2 \times f_1$

3rd-Order Intermodulation (IM3)

IM3 is the total power of the 3rd-order intermodulation product to the Nyquist frequency relative to the total input power of the two input tones f_1 and f_2 . The individual input tone levels are at $-7dBFS$. The 3rd-order intermodulation products are $2 \times f_1 - f_2$, $2 \times f_2 - f_1$, $2 \times f_1 + f_2$, $2 \times f_2 + f_1$.

Full-Power Bandwidth

A large $-0.5dBFS$ analog input signal is applied to an ADC, and the input frequency is swept up to the point where the amplitude of the digitized conversion result has decreased by $-3dB$. This point is defined as full-power input bandwidth frequency.

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Chip Information

TRANSISTOR COUNT: 18,700

PROCESS: CMOS

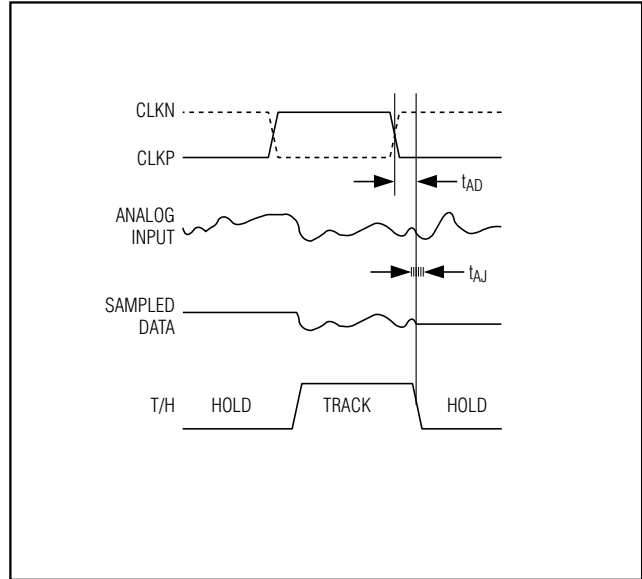


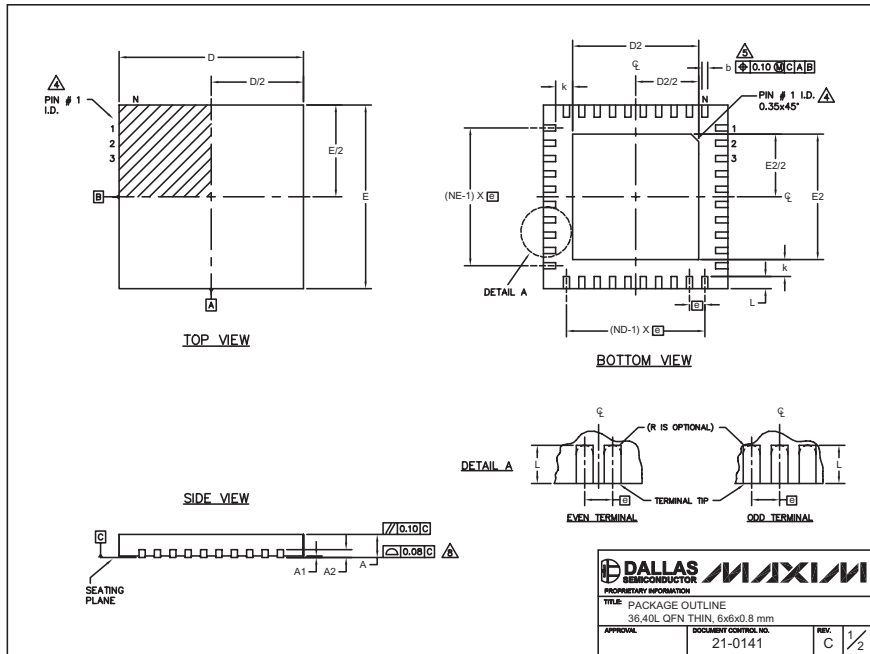
Figure 14. T/H Aperture Timing

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Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



COMMON DIMENSIONS						
PKG.	36L 6x6			40L 6x6		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF.			0.20 REF.		
b	0.20	0.25	0.30	0.20	0.25	0.30
D	5.90	6.00	6.10	5.90	6.00	6.10
E	5.90	6.00	6.10	5.90	6.00	6.10
e	0.50 BSC.			0.50 BSC.		
k	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.30	0.40	0.50
N	36			40		
ND	9			10		
NE	9			10		
JEDEC	WJJD-1			WJJD-2		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T3666-1	3.60	3.70	3.80	3.60	3.70	3.80
T4066-1	4.00	4.10	4.20	4.00	4.10	4.20

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.

△ THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.

△ DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.

△ ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.

7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.

△ COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

9. DRAWING CONFORMS TO JEDEC MO220.

10. WARPAGE SHALL NOT EXCEED 0.10 mm.

DALLAS SEMICONDUCTOR	
MAXIM	
PROPRIETARY INFORMATION	
TITLE: PACKAGE OUTLINE	
36, 40L QFN THIN, 6x6x0.8 mm	
APPROVAL	DOCUMENT CONTROL NO. 21-0141
REV. C	1/2

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